DESIGN AND SIMULATION OF A CIRCUIT TO PREDICT AND COMPENSATE PERFORMANCE VARIABILITY IN SUBMICRON CIRCUIT

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ABSTRACT

We present a technique for compensating process, voltage and temperature variations due to manufacturing and environmental variability in submicron circuits using canary flip-flop. This canary flip flop predicts the timing error before it actually occurs and compensate the performance so that the system performance does not get affected. I am going to design a 16-bit Brent-Kung adder in 45-nm CMOS technology , whose performance will be controlled by supply voltage scaling. I will show that this technique can compensate process, supply voltage, and temperature variations and improve the energy efficiency of submicron circuits. I also discuss how to determine design parameters, such as the inserted location and the buffer delay of the canary FF.

key words – Manufacturing variability, Timing error prediction, Brent-Kung adder, Speed control unit, Canary flip-flop.

I. INTRODUCTION

Manufacturing processes necessary to make an integrated circuit (IC) are among the most sophisticated processes ever invented, since they are inherently sensitive to all kinds of disturbances and, as a result, the manufactured IC components exhibit large variations of their electrical parameters [1]. Process-related variability of semiconductor device characteristics has always been a hardest task for IC process engineers and circuit designers. In nanometer scale devices variability approaches the limits determined by the discrete nature of the solid matter and cannot be reduced by means of improvements in manufacturing processes and equipment.

A good example is the doping concentration. The electrical characteristics of MOS transistors are controlled by introducing dopant atoms into the electrically active regions of these devices. The number of dopant atoms in the channel region of a deep submicron devices is of the order of tens or even single atoms, e.g. the estimated average number of boron atoms in a 32 nm device is 3.5. This means that we will have 3 atoms in one device and 4 in another – a 25% variation of the dopant dose.

As CMOS transistors are scaled to nanometer feature sizes, variations in transistor performance and leakage has become a critical challenge. There are three main sources of variations Process variation , supply voltage variation and Operating temperature variation. These variations cannot be avoided or reduced in any way and lead to unavoidable variations of the device parameters. Therefore it is crucial to estimate these variations and to account for them in the circuit design process.

II. CANARY FLIP-FLOP

Canary FF is augmented with a delay element and a redundant FF named shadow FF, as shown in Figure1. Each FF (main FF) is augmented with a delay buffer and a redundant FF (shadow FF). The shadow FF is used as a canary in a coal mine to help detect whether a timing error is about to occur [2]. Timing errors are predicted by comparing the main FF value with that of the shadow FF, which runs into the timing error a little bit before the main FF. Alert signal triggers voltage or frequency control.

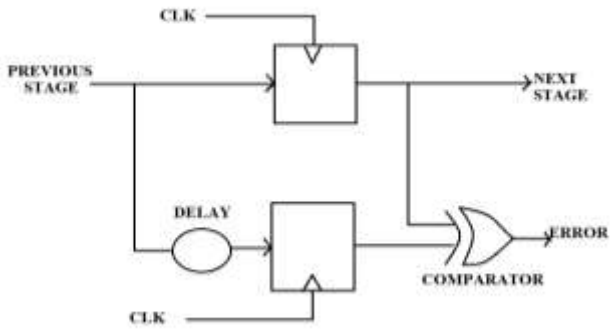

Figure 1. Block diagram of Canary flip-flop

Utilizing canary FFs has the following three advantages.

1. **Elimination of the delayed clock:** Using single phase clock simplifies clock tree design. It also eliminates the short path problem [3] in Razor FF, and hence its minimum-path length constraint should not be considered.

2. **Protection offered against timing errors**: As explained above, in Canary, the shadow FF protects the main FF against timing errors. This freedom from timing errors eliminates any complex recovery mechanism. Hence, Canary is applicable to the common LSIs as well as modern microprocessors that have the recovery mechanism for branch miss-predictions. If Canary FF predicts a timing error, the supply voltage is increased to satisfy timing constraints.

3. **Robustness for variations**: Canary FF is variation resilient. The delay buffer always has a positive delay, even though parameter variations affect it. Hence, the shadow FF always encounters a timing error before the main FF [5].

Fig 2 shows configurable canary flip-flop where canary flip-flop is agumented with delay buffers. The buffer delay is calculated by:

F1 = 1/(Dc+Dd)

F2 = 1/Dc .

Delay = F1 - F2

Where Dc = circuit delay, Dd = Buffer delay.

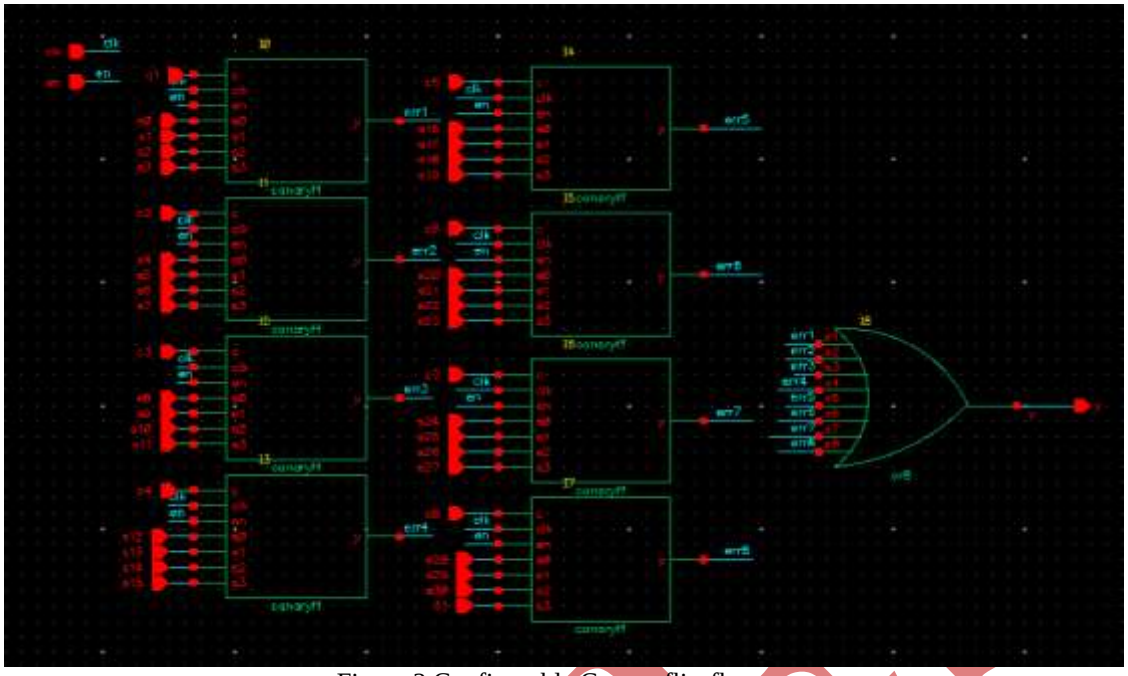

Figure 2 Configurable Canary flip-flop

III. SPEED CONTROL UNIT

Speed control unit alters speed of the Brent-Kung adder whenever warning signal goes high. Figure. 3 shows a schematic of the speed control unit. Four speed levels can be provided by applying four different voltage.

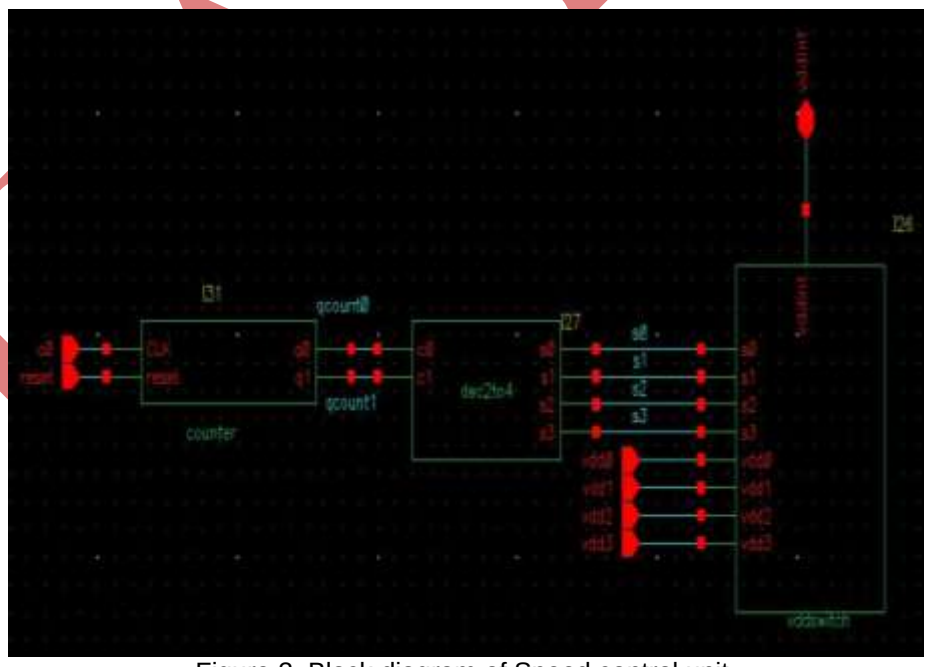

Figure 3. Block diagram of Speed control unit.

VDD1, VDD2, VDD3, and VDD4 are selected according to the speed level stored in a two-bit register, that is, when the stored value in the speed level register is three, for instance,VDD3 is selected. Circuit operation starts at the maximum speed level. When the timer signal is asserted, the speed control unit decrements the speed level

by one and the circuit is slowed down. In contrast, when the warning signal is asserted, the speed control unit immediately increments the speed level by one.

IV. BRENT-KUNG ADDER

The Brent-Kung adder is a parallel prefix adder. Parallel prefix adders are special class of adders that are based on the use of generate and propagate signals. Simpler Brent-Kung adders was been proposed to solve the disadvantages of Kogge-Stone adders. The cost and wiring complexity is greatly reduced. But the logic depth of Brent-Kung adders increases to 2log (2n-1), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Figure 4. In order to achieve a high speed circuit with less complex design, a Brent kung adder is a good candidate and suitable for parallel adder designs with high bit input numbers. Propagate (Exclusive OR) and generate (AND gate) functions.

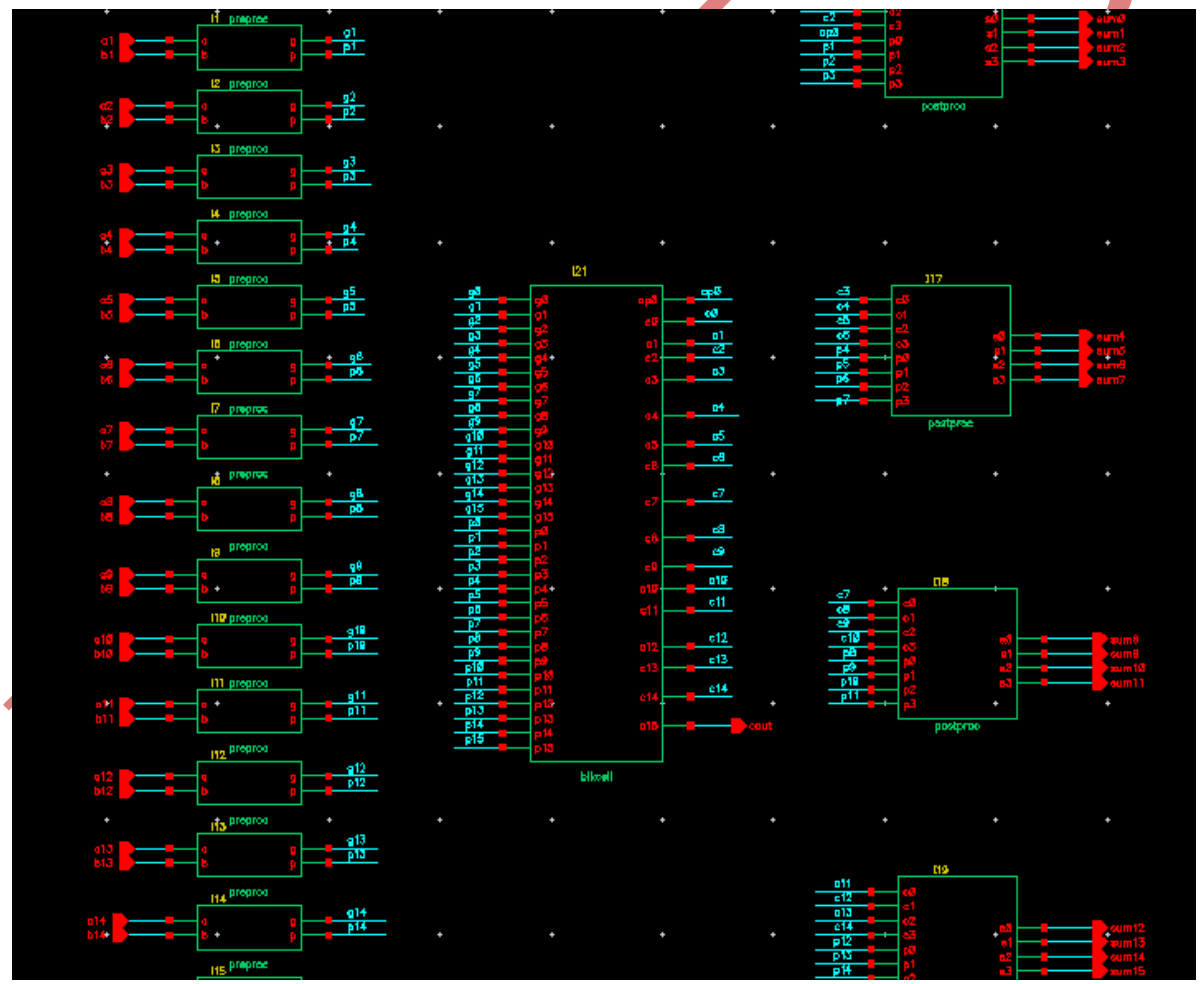

Figure 4. Brent-Kung adder

V. PROPOSED BLOCK DIAGRAM

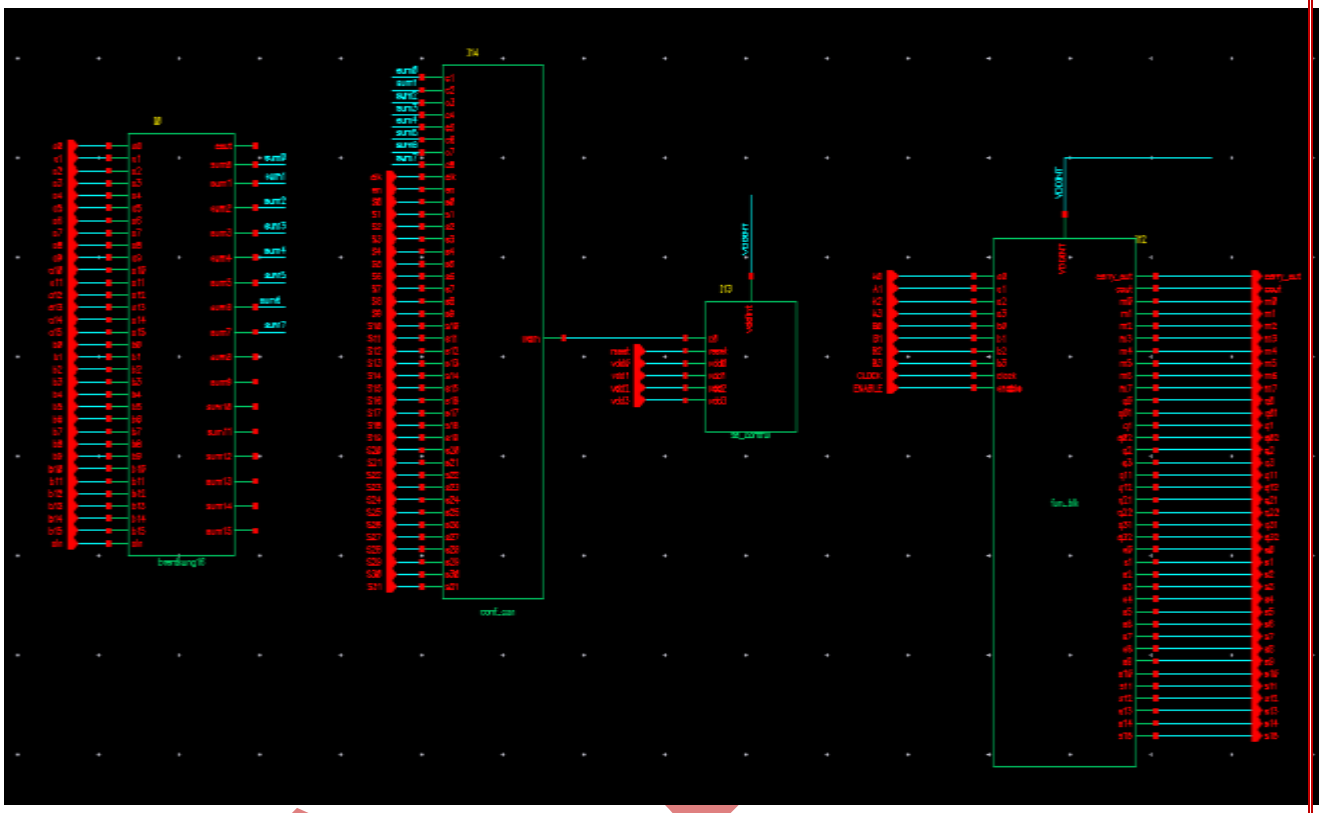

Figure 5. Block diagram of test circuit.16 bit Brent-Kung adder speed is control unit with canary flip-flop.

The structure of the circuit is as depicted in Figure 5. It consists of Configurable canary flip-flop, Speed control unit, brent-kung adder. A 16-bit Brent-hung adder is adopted as a circuit whose performance is controlled by using speed control unit. The circuit speed is controlled digitally and the term "speed level" is used to describe how fast or slow the circuit is controlled. A higher speed level means the circuit is controlled for faster operation.

The output of Brent-kung adder consists of sum bits as S[0] to S[15], from which only S[0] to s[7] is connected to Configurable canary flip-flop. This uses technique that pads the data-path with a delay element and samples the delayed data-path signal in another flip-flop, called the canary flip-flop, which is as shown in figure 5. Each flip-flop (main flip-flop) is augmented with a delay buffer and a redundant flip-flop (shadow flip-flop). Timing errors are predicted by comparing the main flip-flop value with that of the shadow FF, which runs into the timing error a little bit before the main flip-flop. Alert signal triggers voltage control.

The warning signal is monitored during a specified period. Once the warning signal is detected, which is generated by canary flip-flop , the circuit is controlled to speed up. That means speed gets increased by one level. If no warning signals are observed during the monitoring period, the circuit is slowed down by one level for power reduction. Here each speed level has a difference of 0.1 volt. The speed control unit as in the fig consists of a decoder, 4-bit Counter and a voltage switch. If the warning signal from the configurable canary flip-flop is high and the timer signal is high, then these two bits are given to

decoder. Then this output is given to counter which increases the value of decoder by one, that means the speed is increased by one level. Then this value is given to vltage switch, which consists of four pmos each connected to different vdd as in vdd0, vdd1, vdd2, vdd3. Depending upon the output of counter , one out of the four vdd is selected.

VI. MEASUREMENT RESULTS AND WAVEFORM

The Block diagram as in Figure.5 is designed using Cadence Virtuoso tool and simulated by Synopsys Hspice. Figure.6 shows the operation example with 5 sec as monitoring period, where the circuit is operated at 2 MHz with 1v as supply voltage. Speed level for speed control unit corresponds to 0.1 volt. Measurement purpose Three spice models for slow, fast and nominal speeds, which are available in hspice are used.

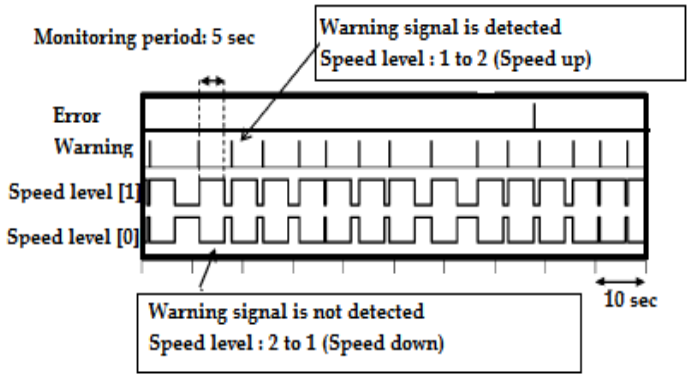

Figure6. Measurement of timing error with monitoring period of 5 sec

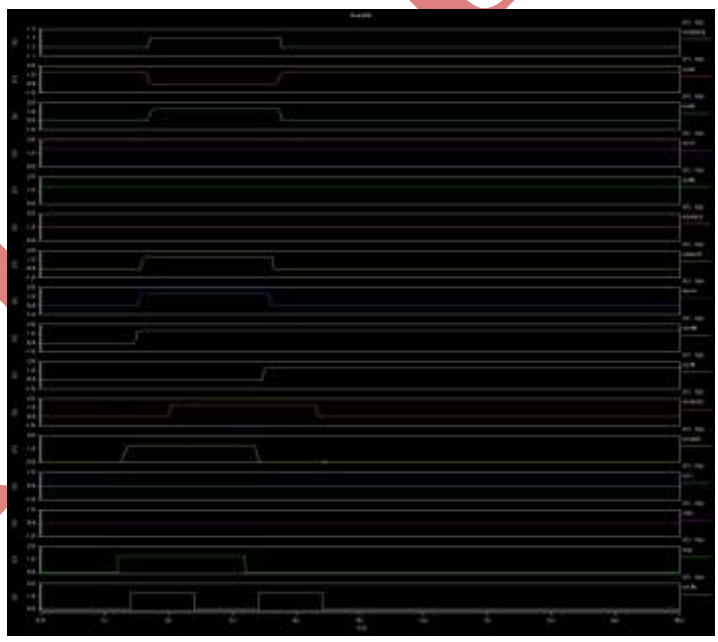

Figure 7. Waveforms of Configurable canary flip-flop with Speed control unit

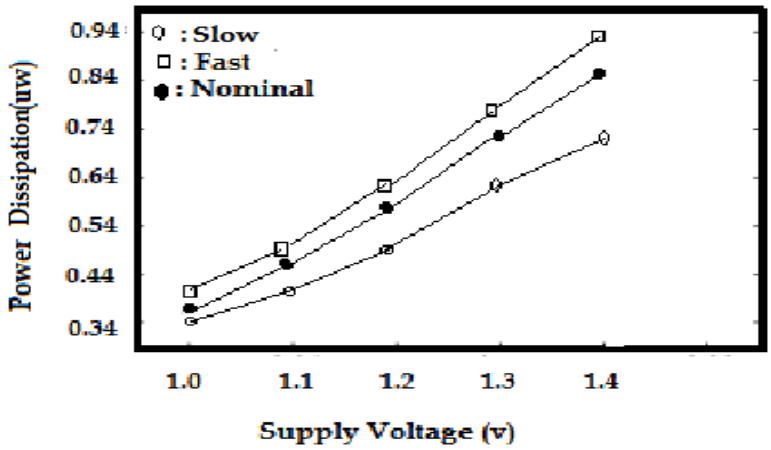

Figure 8.Measurement of power dissipation at various supply voltages at 2 MHz frequency.

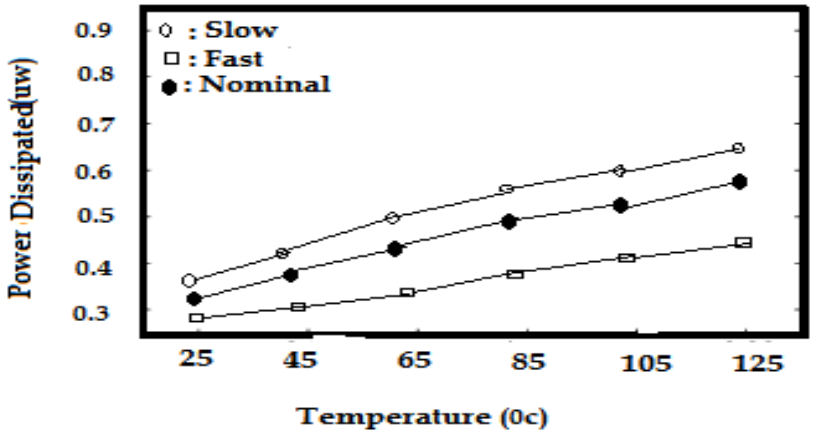

Figure 9. Measurement of Power dissipation at various Temperature conditions at 2 MHz frequency

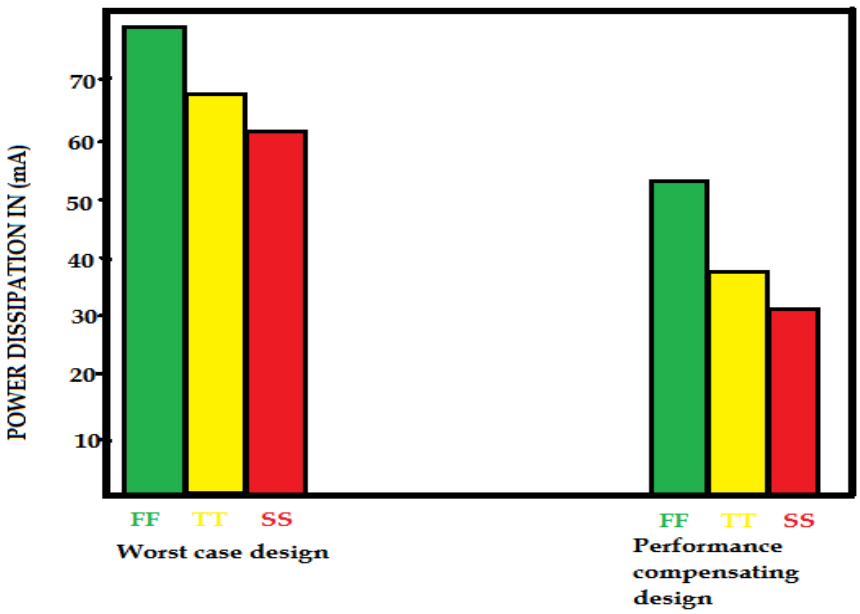

Figure 10 comparisons of worst case and performance compensating designs

Figure 8 and 9 shows the variation of Power dissipation for different supply voltage and temperature respectively. Here three Spice models are taken they are slow, fast and nominal.

VII. CONCLUSION

We presented a performance compensation technique using canary flip-flop for submicron circuits. Canary flip-flop, Configurable canary flip-flop and speed conrol unit is designed in 45nm technology. A 16-bit Brent-Kung adder, whose performance was controlled by speed control unit, was designed in a 45-nm CMOS process using cadence virtuoso tool. Three spice models namely FF, TT and SS are used as design corners to show fast, Nominal and slow chips respectively. Measurement results showed that the adaptive control compensated manufacturing and environmental variability and reduced power dissipation compared to traditional worst-case design. Simulation results indicated that it is appropriate to adjust the buffer delay to attain higher mean time between failures, canary FF insertion with the sufficient buffer delay to cover a wider manufacturing variability space is the most practical.

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