

INVESTIGATION OF FREQUENCY DEPENDENT PARAMETER OF GEWE-SiNW MOSFET FOR MICROWAVE AND RF APPLICATIONS

Neha Gupta¹, Ajay Kumar² and Rishu Chaujar³

¹Department of Engineering Physics, DTU, Delhi (India)

²Department of Engineering Physics, DTU, Delhi (India)

³Assistant Professor, Department of Engineering Physics, DTU, Delhi (India)

ABSTRACT

This paper presents the RF and high frequency performance of Gate Electrode Workfunction Engineered-Silicon Nanowire (GEWE-SiNW) MOSFET and the results so obtained are compared with Silicon Nanowire (SiNW) and Conventional MOSFET by using DEVEDIT-3D and ATLAS device simulator. The simulation results unfold the reduction in parasitic capacitances and lowering of intrinsic delay in GEWE-SiNW MOSFET. Furthermore, significant improvement in stern stability factor (K) has also been observed for GEWE-SiNW MOSFET as compared to conventional and SiNW MOSFETs, thus, reinforcing its use for high frequency wireless applications.

Keywords: Cut-Off Frequency (F_t), GEWE, Maximum Frequency (F_{max}), RF, Stability.

I. INTRODUCTION

The rapid growth of the mobile telecommunication markets emphasizes the need for reliable analog IC design at high frequencies. The RF performance of the Silicon MOSFET has been improved considerably during the late 1990s and early 2000s due to scaling of MOSFET. The reduction of the channel length in CMOS technologies has significantly improved the high frequency properties of the MOSFETs, making CMOS technology suitable for wireless communications and other RF applications [1-2]. Although, scaled technologies leads to undesirable effects such as short channel effects, leakage current, hot carrier effects (HCE), parasitic capacitances which results in degradation of device characteristics such as transconductance, voltage gains, subthreshold slope etc., which is unsuitable for RF/wireless applications [3]. GAA SiNW MOSFET [4] is getting more attention for its advantages of small DIBL, small subthreshold swing etc. Also, it has found that their cut-off frequency can be much larger than that of planar Si-MOSFET [5]. Further, to enhance the carrier efficiency of a device, Zhou and Long [6] in 1999 proposed the concept of GEWE. With this scheme there is appreciable reduction in short channel effects and improvement in on-current due to step potential profile at the interface of metal gates owing to difference in metal workfunctions which results in enhanced lateral electric field allowing the carriers to travel faster hence improving the gate transport efficiency. Moreover, integration of GEWE scheme onto SiNW MOSFET ameliorates device efficiency, enhanced driving capability, minimizes short channel effects etc. [7-8]. Also, due to the increased demand for high-speed electronics products, the accurate analysis of the MOSFET at high frequencies (HF) is requisite to represent the behavior of device in microwave circuits and systems [9]. In

this work, TCAD simulation tool is used to evaluate RF figure of merits of GEWE-SiNW MOSFET in terms of enhanced digital and RF performance of scaled devices in comparison to its conventional counterparts.

II. DEVICE STRUCTURE AND SIMULATION

Fig.1 shows a schematic cross-sectional view of GEWE-SiNW MOSFET where L_1 and L_2 are lengths of two different gate materials with workfunction $\Phi_{M1}=4.8\text{eV}$ and $\Phi_{M2}=4.4\text{eV}$ respectively. For n-channel MOSFET, we select two gate materials in such a way that the gate material having highest work function is placed near the source end and the gate material having lowest workfunction is placed near the drain end.

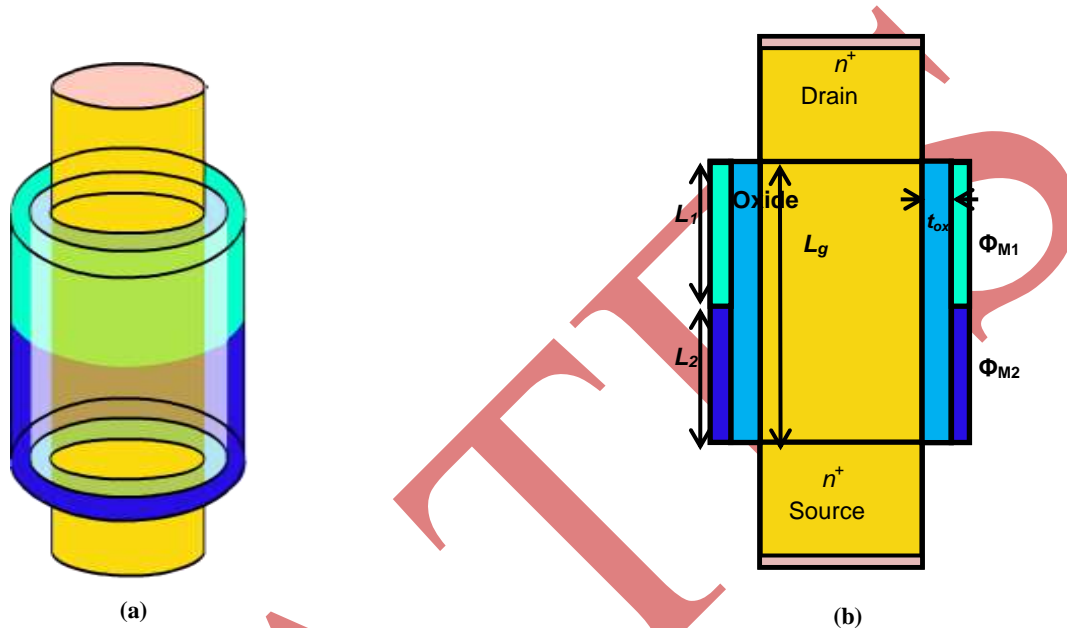


Fig. 1(a-b): Simulated structure and cross section of GEWE-SiNW MOSFET respectively

All the simulations have been performed using physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping dependent carrier lifetime, inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model are all included [10]. In our simulation, we have adopted the hydrodynamic energy transport model which includes all nonlocal effects and is more accurate than the drift-diffusion method.

III. RESULTS AND DISCUSSION

In this paper, we compare GEWE-SiNW MOSFET with its conventional counterparts. The present analysis is carried out for a channel length, $L_g=30\text{ nm}$, radius of NW, $R=5\text{ nm}$ and thickness of oxide, $t_{ox}=1.5\text{ nm}$, substrate doping concentration is $1\times 10^{16}\text{ cm}^{-3}$. It is evident from Fig. 2(a-c) that GEWE-SiNW exhibits smaller C_{SG} , C_{DG} and C_{DS} in comparison to its conventional MOSFET at 240 GHz due to metal gate workfunction difference which results in improved screening of conducting channel from drain variations. In addition, due to Silicon nanowire carrier mobility across the channel is enhanced [11-12], thereby reducing the parasitic capacitances. The higher value of these capacitances acts as an obstruction in device switching performance due to increase in the turn-on delay time.

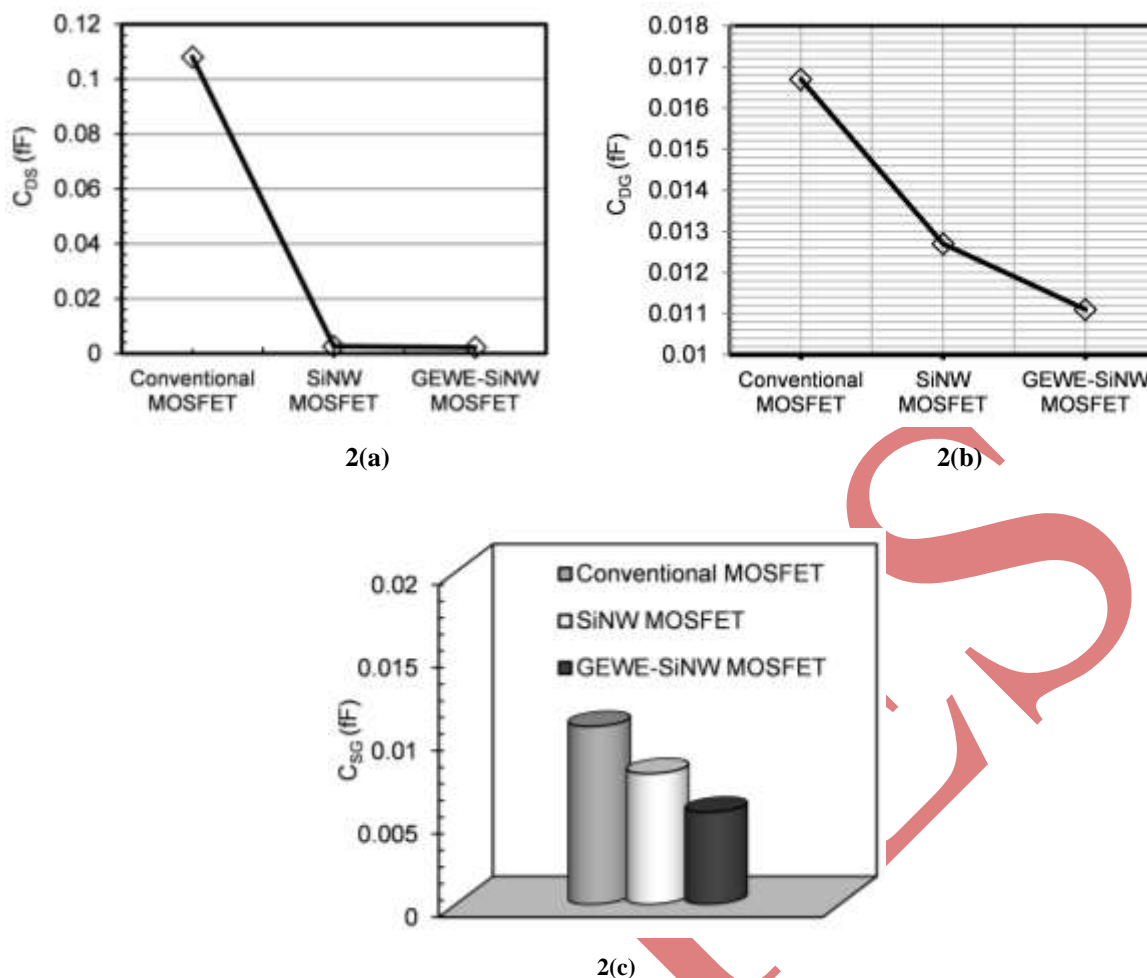


Fig. 2 (a-c): Parasitic capacitance (femto farad) of Drain to source, Drain to Gate and Source to gate for Conventional, SiNW and GEWE-SiNW MOSFET respectively at 240 GHz.

The stern stability factor (K) determines the stability of a device. This factor estimates whether the device is conditionally/unconditionally stable. It must satisfy the condition $K > 1$ for a device to be unconditionally stable [13-15].

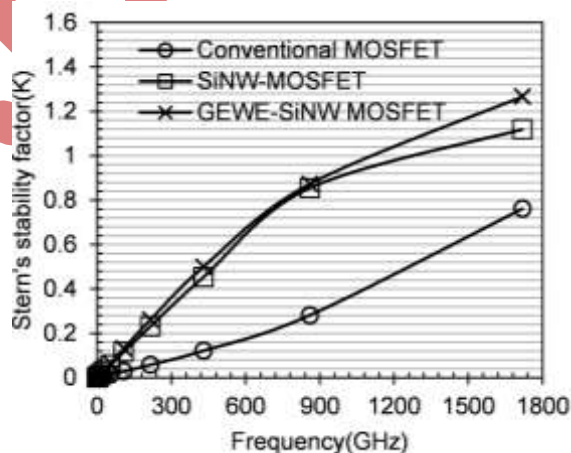


Fig. 3: Variation of Stern's stability (K) factor for Conventional, SiNW and GEWE-SiNW MOSFET

Fig. 3 shows the variation of stern’s stability factor at higher frequencies. As is clear from the figure, K is significantly larger (greater than 1) as frequency increases, for GEWE-SiNW MOSFET in comparison to its counterpart where K is approaching 1.1 in SiNW MOSFET and 0.76 in conventional MOSFET. This is due to increased control of gate, which causes maximum power transfer from source to load. Hence, GEWE-SiNW is suitable for Low noise amplifier and RF applications.

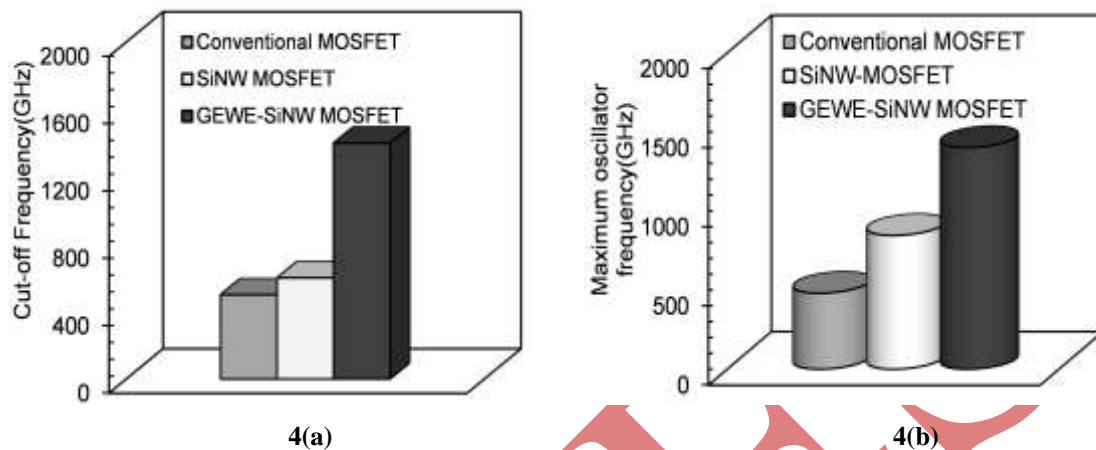


Fig. 4: (a-b) Maximum oscillator frequency and Cut-off frequency for Conventional, SiNW and GEWE-SiNW MOSFET respectively

Further, the cut-off frequency f_T is the frequency when the current gain is unity, whereas f_{MAX} is the frequency when the power gain is unity [16-17]. f_T is a specification for high-speed digital applications (speed and high swing) while f_{MAX} analogous to the transit frequency of the maximum available power gain that is a realistic parameter of the optimization of microwave amplifiers. The f_{MAX} , as is seen from Fig.4 (a), for GEWE-SiNW MOSFET, is higher than for SiNW and Conventional MOSFET, which shows large parasitic capacitance in the conventional and SiNW MOSFET, thereby giving the GEWE-SiNW design a new strength for switching applications and wireless communication. Also, the use of metal gates results in reduced gate resistance, and hence increases in f_{MAX} . Fig. 4(b) shows the cut-off frequency of GEWE-SiNW MOSFET is greater than the cut-off frequency for bulk MOSFET. Due to the enhanced gate control over channel and screening of potential from drain side, it reduces the short channel effects and enhances the transconductance, leading to increase the cut-off frequency and packing density, thereby making the device suitable for CMOS wireless applications.

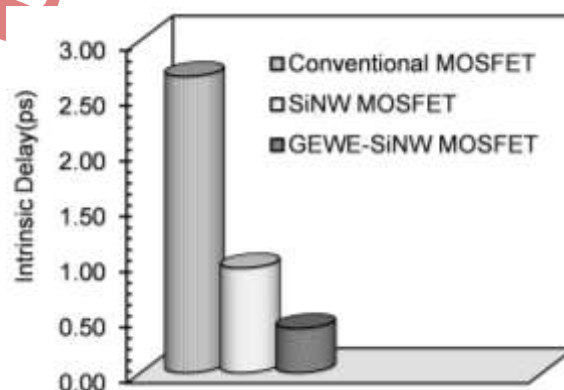


Fig. 5: Intrinsic Delay for Conventional, SiNW and GEWE-SiNW MOSFET

The increasing capacitance between the gate and the overlapped S/D region degrades the intrinsic gate delay. Fig. 5 shows the comparison of GEWE-SiNW with SiNW and conventional MOSFET in terms of intrinsic delay parameter. As is evident from the figure, there is notable reduction in intrinsic delay of GEWE-SiNW MOSFET than its conventional counterparts due to cylindrical gate which increases on-current, reduces parasitic capacitances and incorporation of two dissimilar metal gates, which leads to considerable reduction of intrinsic delay by 55.5%.

IV. CONCLUSION

In this work, we have investigated the improved RF performance of GEWE-SiNW MOSFET and compared it with conventional and SiNW MOSFET, it has been scrutinized that GEWE SiNW MOSFET exhibit lower parasitic capacitances, enhanced cut-off and maximum frequency with an appreciably low intrinsic delay, hence suitable for RF/wireless applications. Furthermore, GEWE-SiNW is found to be more stable than its conventional counterparts, thereby providing its efficacy for high-performance RF applications.

V. ACKNOWLEDGMENT

The authors would like to thank the Microelectronics Research Lab, Department of Engineering Physics, Delhi Technological University (formerly DCE) and one of the authors (Neha Gupta) is grateful to the University Grant Commission (UGC) for providing the necessary financial assistance to carry out this research work.

REFERENCES

- [1] Larson, L. E., "Silicon technology tradeoffs for radio-frequency/mixed-signal system-on-a-chip", IEEE Trans Electron Devices 50(3), 2003, 683–99.
- [2] Saijets. J., Andersson. M. and Berg. M. A., "A Comparative Study of Various MOSFET Models at Radio Frequencies", Analog Integrated Circuits and Signal Processing 33(1), 2002, 5–17
- [3] Chen. Q., "Compact Modeling of Multi-Gate MOSFETs for RF Designs", IEEE International Wireless Symposium, Beijing, 2013, 1-4
- [4] Kim. D. W., Yeo. K. H., Suk. S. D., Li. M., Yeoh. Y. Y., Kyun. S. D. and Chung. C., "Fabrication and electrical characteristics of self-aligned (SA) gate-all-around (GAA) Si nanowire MOSFETs (SNWFET)", IC Design and Technology (ICICDT), IEEE International Conference, 2010, Grenoble, 63-66.
- [5] Wang. C., Zhuge. C., Huang. R., Tian. Y., Xiao. H., Zhang. L., Li. C., Zhang. X. and Wang. Y., "Analog/RF performance of Si nanowire MOSFETs and the impact of process variation", IEEE Trans. Electron Devices 54(6), 2007, 1288–1294.
- [6] Long. W. and Chin. K. K., "Dual Material Gate Field Effect Transistor (DMGFET)", Electron Devices Meeting Tech Dig., 1999, Washington, DC, USA, 549-552.
- [7] Gupta. N and Chaujar. R, "Implications of Transport models on the analog performance of gate electrode workfunction engineered (GEWE) SiNW MOSFET", IEEE Second International conference on Devices, Circuits and Systems (ICDCS'2014), 2014, Coimbatore, India, 278-282.

- [8] Gupta. N, Chaujar. R and Kumar. A, “Simulation analysis of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET for hot carrier reliability”, IEEE 1st International conference on Microelectronics, Circuits and Systems, 2014, Kolkata, India, 150-153
- [9] Doan. C.H., Emami. S., Niknejad. A.M. and Brodersen. R.W., “Millimeter-wave CMOS design”, IEEE J. Solid-State Circuits 40(1), 2005, 144–155.
- [10] ATLAS User’s Manual, SILVACO Int., Santa Clara, 2011, CA.
- [11] Frey. M., Esposito. A. and Schenk. A., “Computational comparison of conductivity and mobility models for silicon nanowire devices”, J. Appl. Phys. 109(8), 2011, 083707 - 083707-6
- [12] Ramayya. E. B., Vasileska. D., Goodnick. R.W. and Knezevic. I., “Electron Mobility in Silicon Nanowires”, IEEE Transactions on Nanotechnology, 6(1), 2008, 113-116.
- [13] Voldman. S. H., (ESD: RF technology and circuits, Wiley, 2006)
- [14] Cho. S., Kim. K. R., Park. B. G. and Kang. I. M., “RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs”, IEEE Trans. Electron Devices 58(5), 2011, 1388–1396.
- [15] Oh. Y. and Rieh. J. S., “Effect of Device Layout on the Stability of RF MOSFETs”, IEEE Transactions on Microwave Theory and Techniques 61(5), 2013, 1861-1869.
- [16] Nae. B., Lazaro. A. and Iniguez. B., “High Frequency and Noise Model of Gate-All-Around MOSFETs, Spanish Conference on Electron Devices”, 2009, Santiago de Compostela, 112-115.
- [17] Sarkar. A., De. S., Dey. A. and Sarkar. C. K., “Analog and RF performance investigation of cylindrical surrounding-gate MOSFET with an analytical pseudo-2D model”, Journal of Computational Electronics, 2012, 11(2), 182-185.

Biographical Notes

Mrs. Neha Gupta is presently working as a Ph. D Research Scholar in Engineering Physics Department from Delhi Technological University (DTU), Delhi, India.

Mr. Ajay Kumar is presently working as Ph. D Research Scholar in Engineering Physics Department from Delhi Technological University (DTU), Delhi, India.

Dr. Rishu Chaujar is working as an Assistant Professor in Engineering Physics Department from Delhi Technological University (DTU), Delhi, India.