A SURVEY ON FINFETS: TECHNOLOGY, PROS, CONS AND IMPROVEMENT PROSPECTS

Revathy. G[1], Dr. Abdul Rajak[2]

[1, 2] *Department of Electrical Engineering, Birla Institute of Technology and Science-Pilani (Dubai Campus), United Arab Emirates*

ABSTRACT

Electronics manufacturing markets are focusing in miniaturization of existing devices and are into delivering products in smaller sizes with higher speeds and power efficiencies. The current transistor technology uses planar CMOS transistors which are used for many analog and digital applications. According to Moore's law, the no. of transistors in an area should double every 18 months. For this to happen, transistors should shrink in size to accommodate double the number per same unit area. Unfortunately, CMOS have short channel effects and leakage coming into picture when its gate length is reduced and so cannot be put into use beyond 22nm reduction. To replace nano-scale CMOS, a trigate device called FINFETs are used. FINFETs proved to be efficient in performance than CMOS, but its only disadvantage being parasitic capacitance is more than that of CMOS' parasitic capacitance. Because of this, the speed of switching might reduce. Current nano-electronics research on FINFETs focus on ways to reduce the parasitic capacitance associated with it. This paper will focus on the issues and the challenges faced so far, their advantages, and prospects of improvement to make it a universal alternative for CMOS in IC applications, aiming towards optimizations in speed, size and power.

Keywords: Analog Applications, Finfets, Nano Electronics, Parasitics, Short Channel Effects

I. INTRODUCTION

FINFETs are non planar structures unlike planar CMOS structures built on a Silicon on Insulator(SOI). CMOS brings noise and other adverse factors because of short channel effects and leakage when the length of gate beyond 22nm. There is also a swing in threshold voltage because of this. To replace this, a multigate device is used for a very precise control over the current across the channel. FINFET as shown in the Fig.1 has gate on three sides, unlike a CMOS which has gate only on one side. Hence, these FETs are called multigate FINFETs. Intel FINFETs have a triangular structure as they increase switching speed. FINFETs operate in two modes Independent Gate (IG) mode and Shorted Gate (SG) mode as shown in Fig.2. These modes decide upon how many gates can control the channel. If its an IG mode, there are two gates to control the channel, and each gate terminals are separate. In the SG mode, both the gate Just as CMOS has its own parasitic capacitance by virtue, due to gate-source and gate-drain overlap, even a FINFET has its parasitic capacitance more than that of CMOS as the gate is covered all 3 sides as shown in Fig. 1. It also illustrates how source and drain is embossed on the insulator substrate and the gate covering the channel in all three sides. This parasitic capacitance brings in more noise to the device, making it disadvantageous to be used in analog and mixed signal circuits.

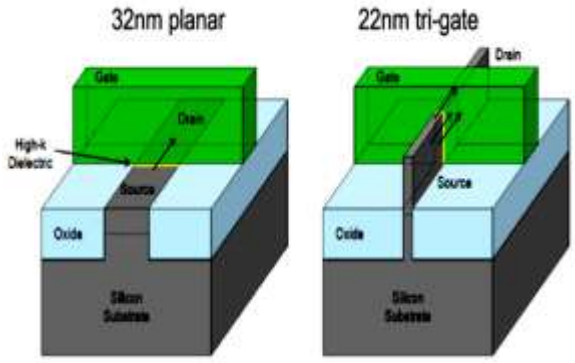


Figure 1 CMOS Vs FINFET

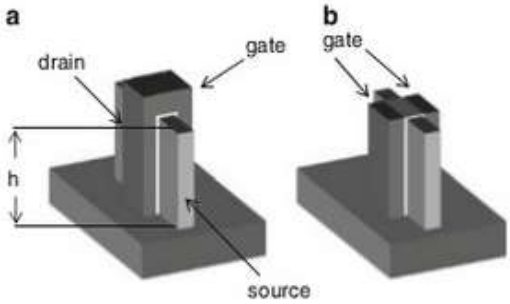


Figure 2. (A) Shorted Gate FINFET (B) Independent Gate FINFET

This paper discusses on the pros and cons of FINFET as it demands more improvisation, how their performance is limited in few applications and their scope for improvement in Section 2. Data and diagrams are presented from the literature to give a better understanding of the problem and ways it can be improved and Section 3 draws conclusions from existing literatures, and scope of future work.

II. PROS, CONS AND IMPROVEMENT PROSPECTS

Many surveys have been made as to whether analog or digital circuits find better applications with FINFETs. Most papers prefer digital applications over analog due to increased parasitic effects in analog. [1] focused on the fact that FINFETs offered more speed but gave a degraded analog performance. CMOS proved to be better alternative for 45nm technology for increased speed and RF performance. But, for low energy and high gain applications, former was better. FINFETs showed increased I_{on}/I_{off} ratio than CMOS, as showed in Table 1 taken from [1]

Table 1 I_{on} and I_{off} values of CMOS and FINFET

Architecture	*Planar CMOS*	*FINFET*
I_{on}	1100 uA/um	550 uA/um
I_{off}	$2.00E^{-8}$ A/um	$1E^{-9}$ A/um
Vt Sat	.034 V	0.22 V

Hence, they conclude that for high gain baseband analog circuits, under 45nm CMOS is difficult to realize, but whereas with FINFET, both can be done. To increase speed and mobility, decrease large series resistances and capacitance between gate and drain. Chenyue Et al [2] lists asymmetric issues of FINET due to hot carrier injection(HCI) and its impact. HCI said to be more prominent from Ids-Vds graph than that of Igs-Vgs graph as shown in Fig. 3.

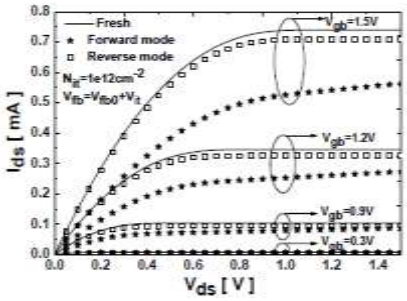


Figure 3 IV Curve Due To HCI Effect

Ashutosh Et al [3] figures out means of enhancing low temperature analog performance of FINFET. A 16 nm FINFET has high mobility. But, a high-k dielectric gate is not a right option. At lower temperature, the percentage of Figure of Merit(FOM) increases, for dual k FINFET. Hence, this is a possible solution at low temperatures. High k dielectric is bad for performance of short channel effects resulting in deterioration of analog figure of merit. Hence, dual k dielectric is attractive for high FOM applications because of improvement in mobility and threshold voltage as enhanced volume inversion, sub-band splitting, velocity overdrive effect, low photon scattering and high in fermi potential and low leakage current. As discussed by Parvais Et al [4] FINFET technologies' about prospects in analog and RF circuits, due to parasitic effects, their behaviour is affected. But, their advantages are good matching performance and reasonable RF characteristics. The problem arises due to series resistance and extrinsic capacitance. Technological solutions and geometrical optimizations are also investigated in the paper. Random telegraph noise impairs FINFET performance, and more emphasis is given about it in [5]. They also impact transconductance, output resistance, cut off frequency, etc. Trigate FINFETs have more diversion than double gate FINFETs. Jagar Et al [6] describes device challenges dealing with analog and RF devices again, but with 14nm technology. Diodes and BJTs are mostly used in RF. Diodes have poor ideality, high leakage and low breakdown voltage where as BJTs have everything discussed and also, weak re-surface action and also low drain current. Hence, FINFET can be a good option, but , it is not very efficient for analog and many papers concentrate on improving performance. In this paper, FINFETs are optimized by changing its geometrical characteristics as shown in Fig. 4.

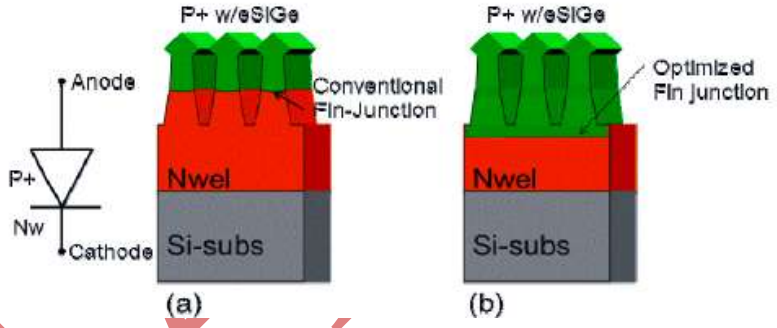


Figure 4 (A) Conventional FINFET (B) Optimized FINFET [6].

And thus, stabilizations in IV are shown in Fig. 5.

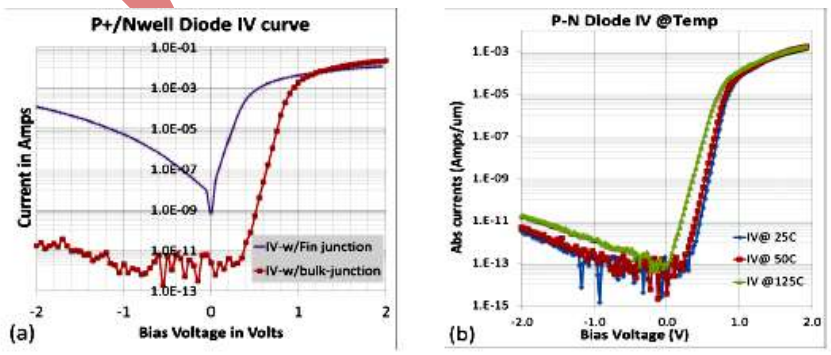


Figure 5 (A) IV Behaviour Of Conventional Vs Optimized FINFET (B) Temperature Dependent IV Characteristics.

From the newly optimized device, re-surface degradation and high leakage current due to 3D effect was able to overcome. Also, it showed increased drain current and decreased transconductance.

But, the disadvantage was that, it dint focus on internal parasitic issues. Instead, they did improvements on geometrics only. [7] tried to compare op-amp operation using 10 nm FINFETs and Planar bulk 28 nm CMOS, and the improvements they sought is shown in Table 2.

Table 2 Challenges in designing analog devices and its improvements from [7].

Devices	*Challenges*	*Improvements[7]*
Diodes	Higher Leakage low BV. Poor ideality	Near perfect ideality and lower leakage
BJT	High leakage, low beta and poor ideality	η= 1.01, low leakage and high beta
Core analog, RF FET	RF performance and poor 1/f noise mismatch	New design under investigation and improved mismatch
Metal resistor	Poor mismatch	Mismatch is improved by 12%

Lithography and processing complications are higher, and also parasitics. As the gate length increases, CMOS is better in performance than FINFETs. In CMOS, intrinsic gain is lesser as gate length increases. The paper concludes that, for OPAMP, FINFET is better because of lower gain bandwidth product of OPAMP. But, for higher specifications, it is not a good option. As current density increases, parasitic resistance worsens and from certain gain bandwidth product onwards, planar CMOS proves better. As a whole, FINFET delivers more gain using less current, but again, its parasitic effects are bad. [8] is also a comparative analysis of double gate FINFET's configurations. They also compare on transconductance, output resistance, gain and cut off frequency. FINFETs have high on off ratio which is a good quality for digital applications, but not for analog. In this paper, three configurations of FINFET operation are compared which are Shorted Gate, Independent Gate and Low power modes and different values of performance parameters are sought. [9] studied on performance of FINFET in a digital circuit, which uses FINFET pass transistor based XOR and XNOR circuits and this is at 45nm. The study of this work is enumerated in Table 3.

Table 3 Comparison Of Delay, Power Delay, Energy Delay Product And Average Power Consumption.

Performance Parameters	*Proposed FINFET XOR[9]*	*Existing CMOS XOR*	*Proposed FINFET OR[9]*	*Existing CMOS OR*
Delay (s)	20.67E-9	0.068E-9	663.7E-9	0.0906E-9
Average Dynamic Power Consumption (W)	6.08E-6	0.053E-3	505.5E-9	0.0987
Power Delay Product (J)	1.25E-15	4.075E-15	3.35E-15	8.93E-15
Energy Delay Product (J)	2.66	0.283	2.226	0.808

This comparison proved FINFET based XNOR; XOR circuits were better in performance and also had lowest power dissipation due to lower power supply and high speed. Julio Et al [11] shows the impact of extrinsic capacitances shown in Fig. 6 and 7 on FINFET high frequency performance. This resistance and capacitance can be reduced by reduction in fin spacing, changing fin height and width and also with suitable optimizations.

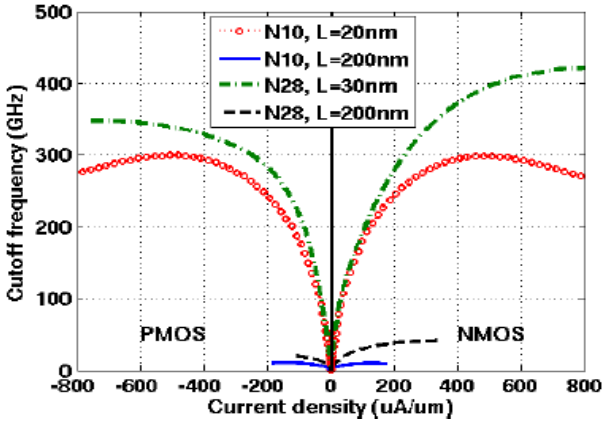


Fig. 6 Effect Of Parasitic Capacitance With FINFET Performance

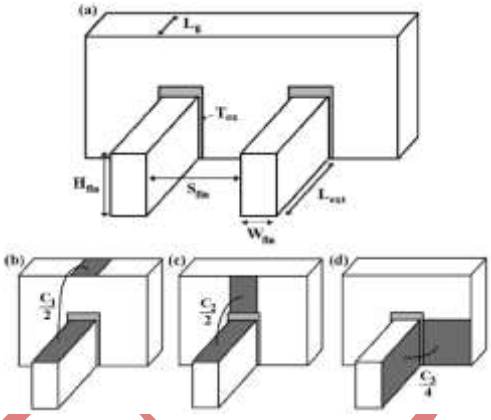


Figure 7 (A) Representation Of 2 Finfets (B), (C), (D) Are Different Capacitances Withing The 3D Structure Walls.

On reducing spacing and adjusting ratio of fin height and width, better performances are observed.

The literature in [12] gives an overview of FINFET being functional as a nano-sensor, as they consume very little power. Cheyue et al [13] again deals with asymmetric issues of FINFET device after HCI and its impact on digital and analog circuits, and the results obtained are more or less the same, as depicted earlier. There are many fluctuations in electrical characteristics of FINFETs and they are given in detail in [14]. These fluctuations arise due to variations in characteristics, manufacturing processes and also due to varied electrical characteristics. Variations due to manufacturing processes turn out as roughness and they are termed as Line edge roughness and line width roughness. Fig. 8 shows the small signal model of FINFET to indicate the capacitances associated within it

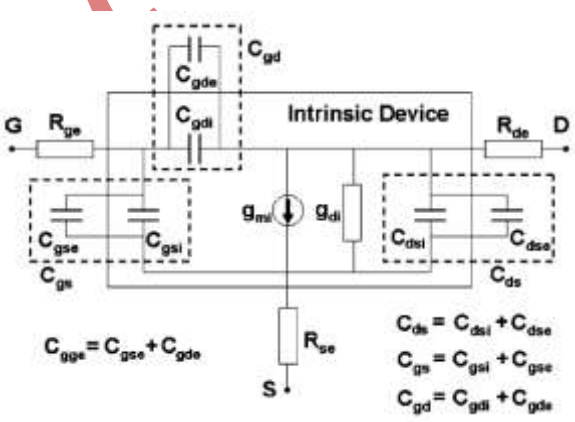
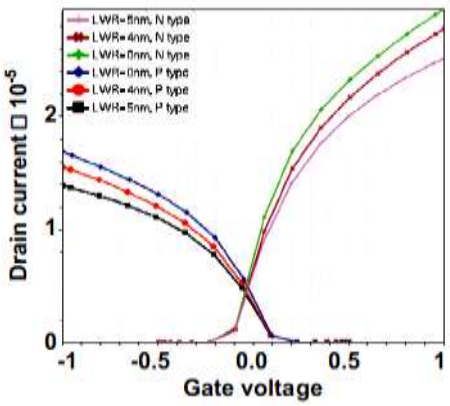


Figure 8 Small Signal Model Of FINFET

Fig. 9 depicts the variation in Id-Vgs due to Line width roughness and Fig. 10 shows the variation of gm-Vgs due to the same.



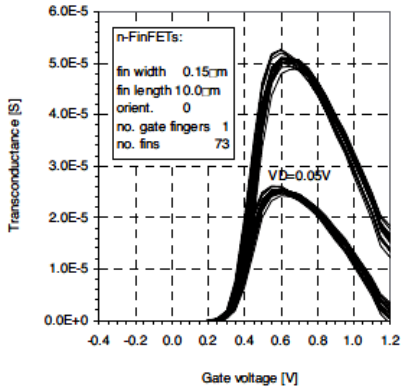


Figure 9 Id-Vg Curves for different width roughness. **Figure 10 gm-Vgs curves for different channels in a FINFET.**

The challenges of FINFETs over planar CMOS are discussed in [15] and is concluded that FINFETs have better matching than CMOS, in spite of its asymmetric properties. For mixed signal scope, [17] focused on a 10 bit digital to analog converter using FINFETs and it proved to reduce the footprint area compared to planar designs, but irregularities in analog performance still existed. Piet Et al in [18] designed analog circuits like varactors, oscillators, resistors, comparators, mixers etc to know more about potential of FINFETs in analog and RF applications. FINFETs were used in better electro static discharge (ESD) protection. Fig. 10 shows a SEM image of the optimized FINFET in [18].

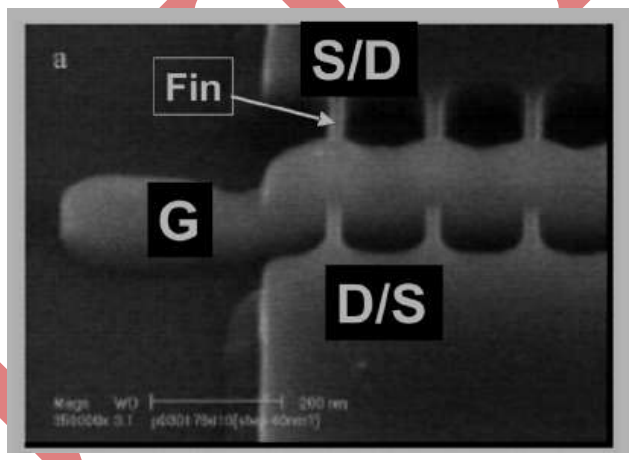


Figure 2 SEM Image of FINFET

The paper concludes that FINFETs are better devices for low power applications. But for high speed or RF, they show inferior performance due to low mobility at sidewalls of fins and high series resistance. The RF/analog perspective of FINFETs were again discussed in [19] where variations on gate length lead to variation in threshold voltage, as shown in fig. 10. FINFETs have a straighter slope when compared to CMOS, and this is also one of the advantages, as they are deciding factor for current leakage in gates. The graph is shown in fig. 12. Gain is also shown as a function of gate length in fig. 13. The off current will be reduced due to reduced junction and sub threshold leakage due to increased series resistance, drive current is degraded and also is the same with transconductance. The improved transconductance amplifier's performance is hence enumerated in Table 4.

Table 4 Performance Of Transconductance Amplifier With FINFET And CMOS.

	90 nm node bulk	*45 nm Bulk*	*45 nm FINFET*
Ao	60 dB	46 dB	73 dB
DC Current	1.12 mA	7.16 uA	863 uA

The dependence of gate length with respect to sub threshold voltage, slope and gain is shown in Fig. 12,13 and 14. This was the main inference from [18]

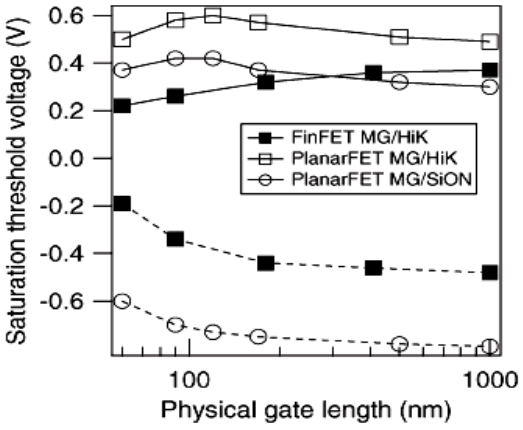


Figure 12 Threshold Voltage Vs Physical Gate Length

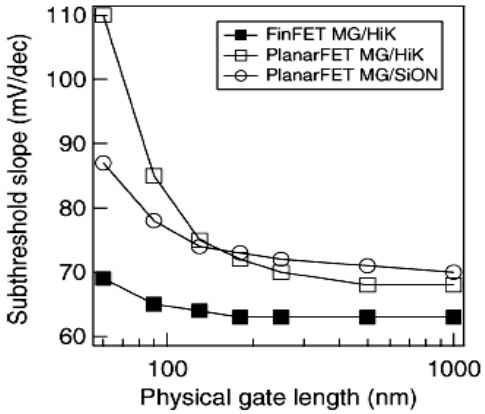


Figure 3 Subthreshold slope Vs gate length.

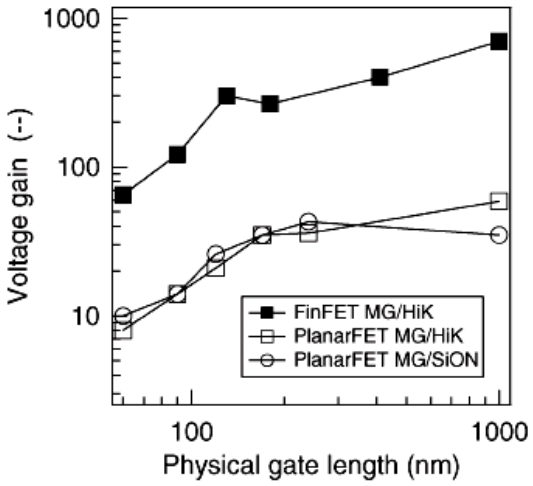


Figure 4 Gain Vs Gate Length.

From all the literature discussed above, we come to a conclusion that though FINFETS pose advantages over CMOS in many aspects, the capacitance associated with it is imposing great parasitic effect, and this needs to be curbed. Because of this, the speed of the circuit designed using FINFET is limited and also is seen as a serious draw back in high speed and RF applications.. Decreasing parasitic effects increase device performance in analog and RF applications. As shown in Fig. 15, on introduction of spacer, the gate to source/drain capacitance decreases due to no direct impact caused by a dielectric.

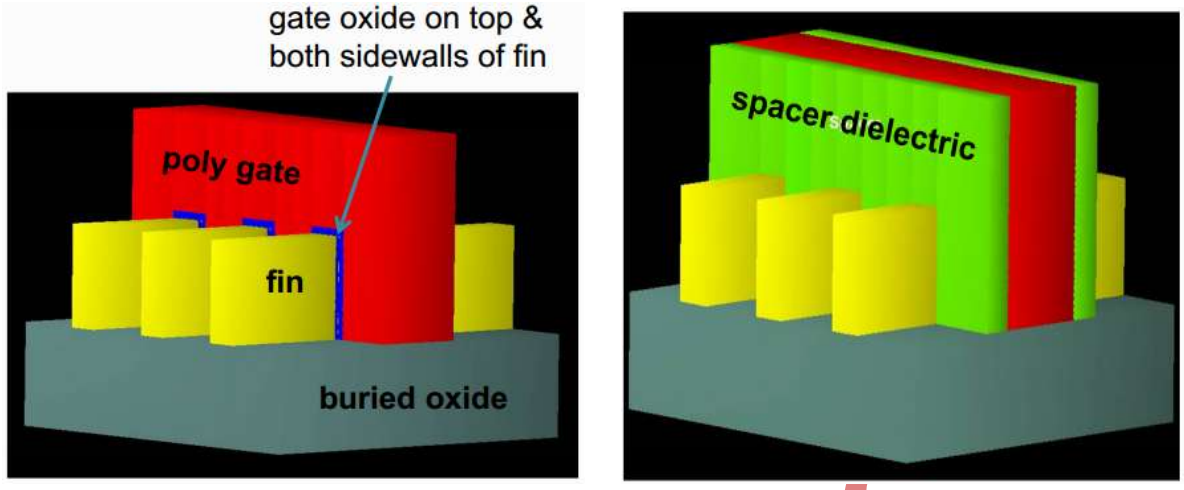


Figure 15 Series of Finfets Before And After SPACER Fabrication

III. CONCLUSION AND FUTURE SCOPE

From the results, derived in research papers, it is concluded that FINFETs are extremely fast and power efficient devices, its disadvantage being difficulties in fabricating it to perfection, being a very small device and its series resistance and extrinsic parasitic capacitance parasitic. Few papers have suggested changes in geometries, dimensions, change in materials used etc. They yielded considerable advancements in drain current, speed, threshold voltage, etc. Out of all, inclusion and change in spacers used proved a considerable improvement over others. They play a major role in deciding the parasitic capacitance of the FINFET. As there is a reduction in capacitance, they offer great performance in analog applications, in which these devices lag also, the threshold voltage is reduced because of which, power consumption too reduced. This can pose great advantage in using FINFETs for analog and high speed devices. The disadvantages of noise and low speed restricted from use of FINFET in such devices.

IV. ACKNOWLEDGMENT

The authors thank Birla Institute of Technology and Science, Pilani for their support, in collaboration with Synopsys Inc, USA for extended software support.

REFERENCES

[1] Piet Wambacq, Bob Verbruggen Et al, “Analog and RF Circuits in 45nm CMOS and Below: Planar Bulk Versus FINFET”, Solid State Conference, vol. 32, pp. 54-57, 2006

[2] Chenyue Ma, Hae Wang Et al, “Asymmetric Issues of FINFET Device after Hot Carrier Injection and Impact on Digital And Analog Circuits”, Quality electronic design 11th international symposium, pp. 432-436, 2010.

[3] Ashutosh Nandi, Ashok K.Saxena Et al, “Enhancing Low Temperature Analog Performance of Underlap FINFET at Scaled Gate Lengths”, Electron Devices on IEEE transactions, vol. pp, no. 99, pp. 1, 2014.

[4] B.Parvais, V.Subramanian Et al, “FINFET Technology for Analog and RF Circuits”, IEEE conference on electronics, circuits and systems, pp. 182-185, 2007.

[5] Chin-Hao Pao, Ming Et al, “Impacts of Random Telegraph Noise On the Analog Properties of FINFET and Trigate Devices and Widlar Current Source”, ICICDT 2012, pp. 1-4, 2012.

[6] Jagar Singh Et al, " analog, rf, and esd device challenges and solutions for 14nm FINFET technology and beyond", VLSI technology:Digest of technical papers, pp. 1-2, 2014.

[7] Sebastien Morrison, "Comparative Study of Fully Differential OPAMP in FINFET and Planar Technologies", PRIME 2014, pp. 1-4, 2014.

[8] Dhruva Ghai, Saraju P.Mohanty, "Comparative Analysis of Double Gate FINFET Configurations for Analog Circuit Design", MWSCAS 2013, pp. 809-812, 2013.

[9] Neha Yadav, Saurab Et al, "Design and analysis of FINFET pass transistor based XOR and Xnor circuits at 45nm technology", ICCCCM 2013, pp. 1-5, 2013.

[10] Julio C. Tinoco Et al, " Impact of Extrinsic Capacitances on FINFET RF Performance", IEEE transactions on microwave theory and techniques, Vol. 61, No. 2, pp. 73-76, 2012.

[11] Adrian M.Ionescu Et al, "Ultra Low Power: Emerging Devices and Their Benefits for Integrated Circuits", IEDM 2011, pp. 61.1.1-16.1.4, 2011.

[12] Chenyu Ma Et al, "Asymmetric Issues of FINFET Device after Hot Carier Injection and Impact on Digital and Analog Circuits", ISQED 2010, pp. 432-436, 2010.

[13] Daniel Tomaszewski Et al, "Fluctuations of Electrical Characteristics of FINFET Devices", MIXDES 2009, pp. 25-27, 2009.

[14] B. parvais et al, "The Device Architecture Dilemma for CMOS Technolgoies: Opportunities and Challenges of FINFET Over Planar Mosfet", VLSI-TSA'09, pp. 80-81, 2009.

[15] Ching Te Chuang, "Modeling, Analysis and TCAD of Nanoscale Devices and Circuits", ISCAS 2009, pp. 2305-2309, 2009.

[16] M.Fulde Et al, "A 10 Bit Current Steering FINFET D/A Converter", IEEE Intl. SOI conference proceedings, 2008, pp. 95-96, 2008.

[17] Piet Wambacq Et al, " The Potential of FINFETS for Analog and RF Circuit Applications", IEEE transactions on circuits and systems, Vol. 54, No. 11, pp. 21-32, 2007.

[18] Vaidy Subramanian Et al, "Planar Bulk MOSFETs Vs FINFETs: An Analog /RF Perspective", IEEE transactions on electron devices, Vol. 53, No.12, pp. 106-115, 2006.

[19] Christian Pacha Et al, "Circuit Design Issues in Multigate FET CMOS Technologies", ISSCC 2006, pp. 1656-1665, 2006.