

A SPWM BASED NINE LEVEL CASCADED FED INDUCTION MOTOR CONTROL

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ABSTRACT

In this paper presented for the industrial applications purpose, now a day's every industrial load are operated with the use of induction machines only, so we have to provide efficient converters are control strategies for the induction motors. In this paper implemented the advanced cascaded h-bridge multi-level inverter (CHBMLI) are used to work with efficient manner, before that we are verified different levels of inverters are examined compare to those inverters CHBMLI is efficient and precise. Except the regulating of the induction machine requires proper controlling strategy for this the investigation is started. First we examined with the pulse width modulation technology to control and maintain the motor requirements. An effective and advanced control strategy sinusoidal pulse width modulation (SPWM) control strategy maintains the motor requirements such as torque, speed and efficiency of the machine. In this paper represents the five level and nine level cascaded inverters are implemented and verified the test results are also discussed in the paper. The five levels and nine levels Simulink model are also verified and tested in the MATLAB/SIMULINK software the results are presented in the paper.

Index terms -- An advanced Cascaded H-bridge multi-level inverter (CHBMLI), sinusoidal pulse width modulation technique (SPWM), total harmonic distortion (THD), induction machine drive

I. INTRODUCTION

In these present days Multi-Level Inverters (MLI) presence very obliging solutions to high power applications point of view as well as in case of the power quality considerations and motor drive troubles. Effectiveness of MLI is enlarged when employing low sampling frequency control are examined. A favored staircase produced output voltage characteristics are achieved by assimilation the single dc voltage sources mutually had been pragmatic.

This utilized dc voltage can be 978-1-4673-6240-5/02 \$31.00 ©2013 IEEE generated from sources such as PV cells, ultra – capacitors, fuel cells and batteries etc. However the three-level inverter having high operating frequency, it affected from higher switching losses creates, audio noise and electromagnetic obstruction generated then the power quality is reduced.

Decontamination its output characteristics minimizes those troubles and its harmonic substance. Multilevel inverters also compensate the common-mode voltage changes checked to a normal inverter had been verified. Thus it is additional suitable for feature applications which necessitate high voltage/ampere evaluation.

At huge multilevel inverters are divided into cascaded H-bridge diode clamped, and flying capacitor. Among those methods the cascade multi-level inverter CHBMLI generates improved output voltage waveform performance with minor Total Harmonic Distortion effect when growing the output levels of inverter. In addition to that the selected output values are prohibited by controlling the pulses of the width by Pulse Width Modulation (PWM) process. Accordingly by the way of adaptable the modulation assortment harmonic deformation get progressively reduced.

The multilevel Pulse Width Modulation inverter has decreased dv/dt checked to normal PWM inverter drive operations since in the middle of many voltage levels operating sequence considered are discussed. This compensated dv/dt will escort to controlling the failure belongs to the motor bearings and windings. These merits of CHB-MLI have designed tremendous attention towards medium voltage high power applications by the inverters and in regenerative motor drive features.

In industries the usage of induction motors and the workhorses are key role for the applications to the loads. In order to offer a wide collection of control appropriate power converter is necessary in the drive arrangement for that cascade multi-level inverters are more appropriate.

As stator electrical energy of CHBMLI is connected to the motor production range of current is almost sinusoidal. In addition while the motor run in accuse mode or constrain mode the charge disturbed load problems will not happened. In this paper proportional investigation of nine-level and five-level CHBMLI with included the induction motor constrain presentation are performed and verified.

The agreement of CHB-MLI is very easy. Similar to the flying capacitor and diode clamped MLI, the usage of capacitors and clamping diodes are not required for CHBMLI. This gives quite elasticity when increasing it to different levels.

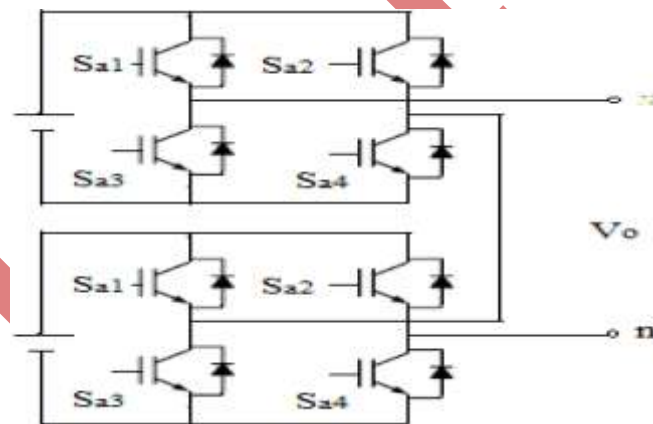


Fig.1 Single phase leg of five-level cascaded inverter

Fig.1 illustrated the single phase leg configuration of five-level cascaded H-bridge inverter. At this time each full bridge inverter produced dissimilar generated output voltages which are $+V_{dc}$, 0 , $-V_{dc}$ during different agreement of four power electronic switches S_{a1} , S_{a2} , S_{a3} and S_{a4} .

To get $+V_{dc}$, S_{a1} and S_{a4} are switched on, where $-V_{dc}$ can be necessitate by rotating on S_{a2} and S_{a3} . When revolving on all the power electronic switches produce voltage generates 0 . The generated output phase voltage stages are specified by $m=2N+1$, where 'N' is the amount of dc sources used and 'm' corresponds to the number of levels.

II. OPERATION OF NINE-LEVEL CASCADED H BRIDGE

The cascaded multi level inverter operated and associated with the induction motor drive applications. The 3-phase induction motors are the commonly considered operated machines in industry since of its simple proposerough and easy preservation. The switching frequency of induction motor is directly comparative to the rated synchronous speed.

The magnetic flux created by three phase currents passes and rotates with a steady speed where the sampling frequency of the drive is comparative to rated speed. Consequently the rotating flux and rotor current produce a force that controlling systems the motor and as a result torque will expanded.

For Cascaded H-bridge multi-level inverter fed induction motor application to the inverter system is functioned based on series association of single phase inverters with individual dc sources. The level shifted multi-carrier Pulse Width Modulation standards are employed to CHBMLI anywhere it includes many triangular carriers operating signals and one reference modulating signal.

Fig.2 demonstrates the PWM production. In this the operated pulse model depends on the ratio of regulating V control to the peak carrier voltage V_{tri} preferred as modulation index that is given by.

$$= M_a \frac{V_{control}}{V_{tri}}$$

The maximum value of V control regulates the amplitude and the frequency of Voltage control it regulates the minimum operating frequency. The figure demonstrates three-phase induction motor operated by nine level cascade inverter anywhere the internal block represents for the generation of pulses from pulse generator have eight number of carrier modulating signals. In that four are employed for the positive half of the regulating signal and the remaining four signals are associated with the negative half cycle of the modulating signal.

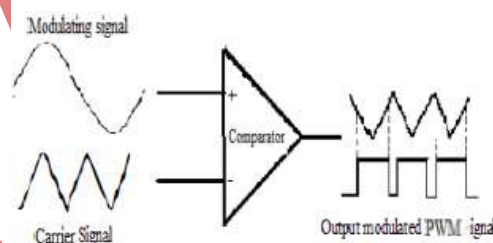


Fig.2 PWM generation

So 16 PWM signals are produced and then specified to the sixteen power electronic switches support. Likewise the generated pulses are generated for outstanding phases. To get balanced condition for the three phase output voltage from the modulation signal is phase conflicting by 120°. The whole time inverter equipped state line to stranded voltage get simply prohibited.

III. EXISTED SYSTEM

The cascaded multi-level inverter is designed to produce output voltage is very effective compare to the other multi-level inverters such as diode clamped inverters and flying capacitor based inverters. The designed block diagram of the CHBMLI is demonstrated the below mentioned figure.3.

The cascaded multi-level inverters are associated depending up on the series connection of H- bridge inverters these are interfaced series with the sinusoidal inputs in order to produce the voltage. The sum of the total voltage is calculated by adding the individual voltages of the each cell.

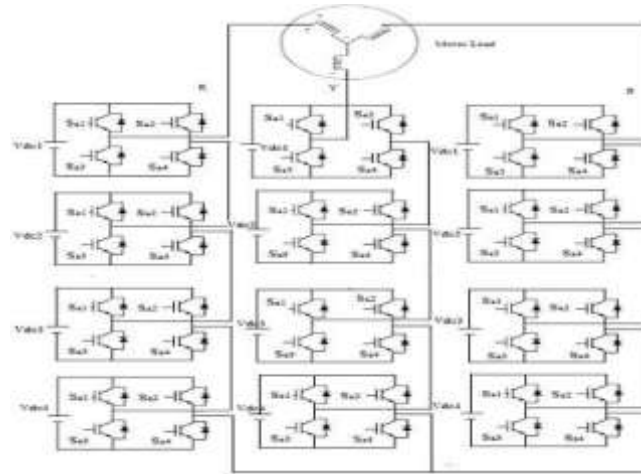


Figure.3.CHBMLI basic block digram

The number output voltage generates is calculated by $2n+1$ where n is the total number cells are used in the converters. The conducting angels are measured to give the gate pulses to the inverters of the circuit.

The required number of components in this inverter is less than the flying capacitor based and the diode clamped based inverters. So size of the inverter is reduced and the overall cost of the inverter is also minimized due to this the cascaded based inverters are frequently used in the induction machine applications.

Here in this project we are designed the five level and nine level inverters are implemented by using the Pulse width modulation control methodology. The PWM method is very successful procedure to generate the pulsed to the inverter to generate the output voltage is effective manner.

The produces are generated by the use of PWM techniques to the multi level inverters then the generated the output voltage has eight step type levels are produced and one zero level is included so it is seemed very close to the sinusoidal output and hence there is very less harmonic contents are produced from the inverters then the usage filter cost also reduced.

The advantages of this inverter there is no requirement of the transformer in the main power conversion of the inverter. Even though there we have to maintain the isolation power supplies of the each cell in the proposed hybrid inverter. The provision of individual isolation power supplies explains the limitations of the each cell designing in the h-bridge inverter.

IV. PROPOSED SYSTEM

The proposed cascaded multi-level inverter is operated by using sinusoidal pulse width modulation control strategy. The SPWM control strategy operates the sub harmonic principle method for the cascaded inverters but in the case of the general PWM control strategy is functioned with the single carrier modulation control technique is performed the multi-level inverters by using the digital signal processing application based principles.

It explains the single carrier based voltage modulation for the modulation inverters. Suppose we use the uni polar multi carrier signals for the flying capacitor based inverters.

In the SPWM control functioned with the use of sub harmonic principle in this dissipation band carrier and the usage of the phase shifted carrier is utilized to operate the multi-level inverters.

The SPWM based pulsed are given to the CHBMLI inverts are performed very effective manner compare to the general PWM inverter. Because in case of PWM produces the pulses without calculation of dissipation values then it does not produce the desired pulses. In the SPWM it calculated the dissipation and phase shifted values then the pulses are generated.

The generation of pulses are directly connected to the inverters in this the production of output voltage is very accurately. It produced total harmonic content is better performance than the losses of the system is reduces then the induction machine properties like torque, speed and efficiency of the system is enhanced corresponds when we change the speed of the induction machine then the time taken to change the response also very quickly. Due to these reasons the reliability of the CHBMLI system is enhanced.

V. CONCLUSION

In this paper we are proposed the multilevel inverter based cascaded H-bridge inverter is suggested. Before that we are studied different types of inverters and different levels of the inverter also tested and verified. Finally proposed the cascaded H-bridge multi level inverter (CHBMLI) is the selected for the industrial induction machine application purpose.

Now a day's induction machine applications are extended so we have to work on the effective control strategies. In that we are proposed the sinusoidal pulse width modulation control strategy (SPWM) is the effective technique to generate our required motor parameters torque, speed and performance of the implemented effective approach.

The SPWM control strategy provided the effective conducting pulses to the CHBMLI to work and maintain with better response. In this we are designed the different levels of CHBMLI in that five level and nine levels are tested and verified and compared to identified that the nine level inverter maintained the better performance.



In the MATLAB/SIMULINK models are designed tested and verified the different are discussed and concluded that the nine level cascaded multi level inverter with SPWM control strategy generates enhanced reliability for the induction machine applications.

REFERENCES

- [1]. Authours G. Sudhakar and S. Prabhakaran "Design of Nine Level Inverter Topology for Three Phase Induction Motor Drives" on Bonfring International Journal of Power Systems and Integrated Circuits, Vol. 4, No. 1, February 2014.
- [2]. Authours bindeshwar singh¹, nupurmittal³, dr. k.s. verma², dr. deependra singh², s.p. singh¹, , rahul dixit³, manvendra singh³, and aanchalbaranwal "Multi-Level Inverter: A Literature Survey On Topologies And Control Strategies" on International Journal of Reviews in Computing 31st July 2012. Vol. 10.3.I. Rodriguez, .I. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind Electron., vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [4]. I. Rodriguez, S. Bernet, B. Wu, I. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930-2945, Dec. 2007.
- [5] K. A. Corzine, F. A. Hardrick, and Y. L. Familiant, "A cascaded multilevel H-bridge inverter utilizing capacitor voltages sources," in Proc. A IASTAD Power Electronics Technology and Applications Conference, Feb 2003.

- [6] J. Chiasson, L. M. Tolbert, K. McKenzie, and Z Du, "A complete solution to the harmonic elimination problem," IEEE Trans. Power Electron., vol. 19, no. 2, pp. 491-499, Mar. 2004.

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