

BUCK-BOOST CONVERTER BASED HIGH CURRENT AND LOW VOLTAGE APPLICATION

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ABSTRACT

This paper develops a pulse width modulation dc–dc non-isolated buck converter with the three-state switching cell, included by two diodes two active switches, and two coupled inductors. Only the load power is developed by the active switches, mitigating the peak current by the switches to 50 percentage of the load current, as much power levels can then be getting by the implemented technique. The compensation of reactive elements can be regulated by the inductors and capacitors, is also reduced. Since the ripple frequency of the output voltage is double the switching frequency. By the intrinsic characteristics of the technique, overall losses are diffused among all semiconductors. Another benefit of this converter is the mitigated region for discontinuous conduction mode when differentiated to the general buck converter or, in other words, the operation limit for continuous conduction mode operation is increased, as signified by the static gain plot. The theoretical technique is detailed by qualitative and quantitative approach by the application of the three-state switching cell to the buck converter performing in non-over lapping mode ($D < 0.5$). Excluding, the mathematical analysis and development of an innovative prototype rated at 1 kW are carried out. The main experimental results are developed and sufficiently examine to clearly identify its claimed benefits.

Keywords: DC–DC Converters, Buck Converter, Three-State Switching Cell (3SSC).

I. INTRODUCTION

Pulse width modulation (PWM) dc–dc converters are mostly used in numerous applications, like as, fuel cell powered systems, and uninterruptible power supplies, audio amplifiers, and fork lift vehicles, despite the fact many other ones can be easily identified. Traditional difficult switching converters including a single active switch such as buck, boost, buck–boost, Cuk, single-ended primary-inductance converter (SEPIC), and Zeta consistently present low power density, while tryout to further reduce the size of filter elements lead to more switching losses, negotiate the efficiency of the converters. In order to reduce such limitation, different soft switching techniques have been developed in the composition. Soft switching is developed to mitigate the mingled between voltage and current at the time of the commutation, and can be restrict in one active or passive techniques, as one must choose between the preceding snubbers for a given application. Active techniques can mitigate the switching losses by including auxiliary switches. Unsuccessfully, an auxiliary switch enhances the difficulty of both power and control circuits. Synchronization faults between control signals of the switches at the time of transient also obscure the control strategy. The design cost is enhanced and reliability is afflicted by using active snubbers. A passive loss-less snubber can effectively moderate switching losses and

electromagnetic interference (EMI) noise using no active parameters and no power destructive components. No external control is needed and no circulating energy is reproduced. Circuit arrangement is as easy as *RCD* (resistor–capacitor–diode) snubbers while circuit efficiency and reliability is as more as active snubbers and resonant converters. Low cost, effective performance, and high reliability are the definite benefits of a passive lossless snubber. On the other hand, soft switching may not be produced for the entire load range, and more over the accurate design of the resonant tank is not a trivial assignment, even what is also accurate when active snubbers are considered. Significant effort has then been made to enhance the characteristics of the conventional non-isolated dc–dc converters in the last few years. For occurrence, the study of a dc–dc buck converter with three-level buck clamping, active clamping, zero voltage switching (ZVS), and fixed-frequency Pulse Width Modulation (PWM) is developed in reference. The generations of converters is also borrowed, which representative the advantages of mitigate voltage across the switches using a three-level commutation cell, and reduced switching losses produced from a soft switching method. As the power rating enhanced, it is often required to combine converters in series or in parallel. By using interleaving methods in high current advantages, the currents through the switches become just portions of the source current. Interleaving accurately twice the switching frequency and also partially cancels the input and output harmonic ripples, as the size of the energy storage parameters like as inductors and differential-mode EMI filter in finally techniques can be reduced. In the last few years, many converters worked on the three-state switching cell (3SSC) have been implemented. The cell can be designed by the combination of two two-state PWM cells (2SSC) attached to a center tap autotransformer, from which novel converters can be borrowed. General benefits over traditional techniques can be developed, e.g., the inductor is implemented for doubles the switching frequency, with consequent mitigation of size and weight; the current through the switches is 50 percentage of the source current; part of the input power is transported to the load by the transformer replace of the main switches, therefore minimized conduction and commutation losses; lower cost switches can be used. Many dc–dc converters operated on the 3SSC have been received in the last few years. On the other hand, the aforementioned works are basically involved with high voltage gain boost-based techniques assigned to dc voltage step-up applications. Biography does not present further detailed studies respecting the remaining dc–dc non-isolated techniques using the 3SSC. Within this context, this paper implements the complete study of the dc–dc converter worked on the 3SSC. Firstly, some theoretical background on the 2SSC and the 3SSC is designed, leading to the conception of the enhanced buck converter using the so-called cell type *B*. Then, the converter operation in non overlapping operation (NOM) is presented, where the main characteristics of the technique are discussed. An experimental prototype is then developed, while the detailed discussion of experimental results is proposed to validate the theoretical conditions and also arranged the benefits of the proposal.

II. CONCEPTION OF THE 3SSC AND THE PROPOSED

2.1 Buck Converter

The canonical switching cell is techniques that allows us to produce and divided the conventional dc–dc converters, from which some existed of converters can be impose. The second-order systems are Buck, boost, and buck–boost converters, as well as Cuk, SEPIC, and Zeta, which is fourth-order systems, has a single switching cell that is part of their respective power stages. Literature has also shown appreciable effort to enhance the characteristics of the original structures; however the novel resulting methods are more difficult

techniques with larger component count. The aforementioned switching cell is included of three points, which are active, passive, and common. Its performance is based on the complementary operation of two switches interfaced with the common terminal. Even though, one switch is turned ON while the other one remains turned OFF, and vice versa. Therefore, this process can be called 2SSC. With the target of getting larger power density, switching frequency is usually enhanced, with consequent decrement of size and volume of reactive elements. Consequently, it tends to enhance of both switching losses and the volume of heat sinks. This proceeding, consequently, compromises the very reduction of physical quantities in static power converters. Consequently mentioned losses must then be mitigated, and soft switching circuits with the resonance technique have been adversely proposed as a possible solution. By using well-known methods such as ZVS and zero current switching, the quality of converters can be enhanced. However, against switching losses are reduced or controlled, conduction losses are still of dangerous problem and may even larger depending on the adopted snubber. With the aim to further mitigate voltage and/or current problems, the interconnection of semiconductors or even converters in series or in parallel has been thoroughly identified. Other techniques can also be produced, such as multilevel converters. It is also useful to enhance the efficiency and reliability by the use of the 3SSC, which has been applied in recent publications and is originally borrowed from the dc–dc push–pull converter. In order to get the cell type *B*, let us consider the general push–pull technology, given in Fig. 1, which is generated by switches *S1* and *S2*, high-frequency transformer and two rectifier diodes *D1* and *D2* in the secondary side.

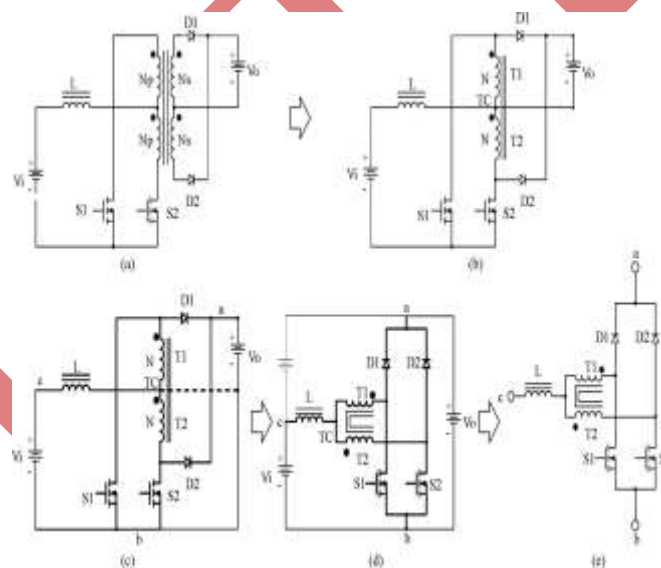


Fig.1. 3SSC Type B

The circuit enables to a dc–ac–dc conversion arrangement. If the central tap transformer is used ideal with unity turns ratio, the primary and secondary windings can be connected by the proper magnetizing inductances, which are coupled and included an autotransformer. The negative terminal of the output stage denoted by V_o , which was normally interfaced to the central tap of the transformer, is then Switched to the negative terminal of the source voltage source to reproduce a boost technique, as shown in Fig. 1(c). Otherwise, if connected to the positive pole, a buck–boost converter is borrowed. The cell type *B* can then be employed to the dc–dc buck converter substituting the 2SSC, while the resulting technique is available in Fig. 2.

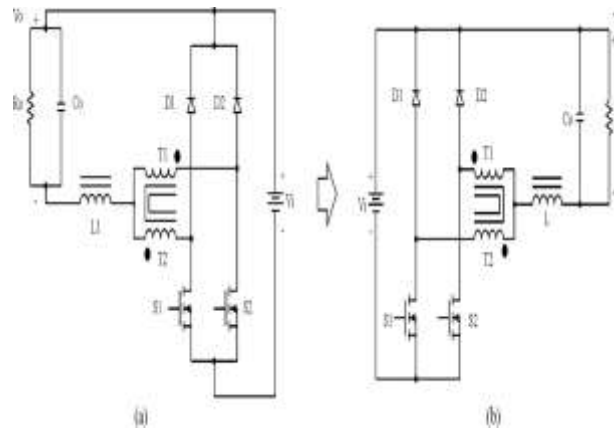


Fig.2. Buck Converter Based On The 3SSC

It can be seen that the 3SSC is generated by two regulated switches $S1$ and $S2$, one autotransformer $T1_T2$, two diodes $D1$ and $D2$, and one inductor L . Although the resulting cell seems more difficult with larger component count than the conventional 2SSC, the benefits over its counterpart will be clearly identified in this literature. For instance, the use of the 3SSC may tend to the necessary of switches with minimized current rating, which is securable in step-down larger-current applications. Considering that the mode of the switch and the diode of a same leg are reciprocal, two modes according the main switches can be generated for the implemented technique. If the duty cycle D is larger than 0.5, overlapping mode (OM) generated, where two switches continue to turned ON at the same Time. Otherwise, if $D < 0.5$, the converter performs in NOM while only one switch continued to turned ON in a given working stage. The developed method can be seen as the interconnection of the interleaving approach and the 3SSC. The following benefits characteristics can be then identified to the design this method:

- 1) Minimized size, weight, and volume of magnetic, which are developed for doubles the switching frequency comparatively to the interlaced buck converter.
- 2) The current stress allows each main switch is similar to 50% of the total output current, allowing the possibility of semiconductors with minimum current ratings.
- 3) Losses are distributed group of the semiconductors, leading to good heat distribution and consequently high efficient with the heat sinks.
- 4) Some part of the input power, i.e., 50%, is connected directly to transfer the power to load through the diodes and the coupled inductors, and not by the main switches. As a result, conduction and switching losses are mitigated. This is the major consideration between the functionality of this technique and that of the interlaced buck method.
- 5) The purpose of the 3SSC allows the parallel connection of switches and, consequently, in over-priced power devices and drives can be used.
- 6) Energy is relocated from the source to the load at that time most part of the switching period, which is a different characteristic of the developed converter, since in other buck type converters, it only available during half of the switching period. As a result, mitigation of current peaks and also conduction losses are conventional.
- 7) The drive diagram of the major controlling switches becomes less difficult because they are associated to the same reference point, what does not appear in the interlaced buck converter.

For the detailed explanation of the dc–dc buck converter with the 3SSC in NOM, the below mentioned conditions are made:

- The converter performs in steady state;
- Switching frequency is fixed and PWM is applied to drive the switches;
- The firing signals of the switches are 180° deranged;
- The autotransformer turns ratio is equal to unity;
- The magnetizing current is very low than the load current;
- All semiconductor and passive parameters are ideal.

III. PRINCIPLE OF OPERATION

3.2 Operation in NOM and Continuous Conduction Mode (CCM) ($D < 0.5$)

The converter working can be explained according to four operating stages as seen in Fig. 3.

The particular main theoretical waveforms are appeared in Fig. 4, where each one of the elements is defined as given as follows:

- $V_g(S1), V_g(S2)$ —gating signals applied to control switches S_1 and S_2 , basically;
- I_L —current flowing through inductor L , while the maximum and Minimum values chosen by this quantity are I_M and I_m , simultaneously;
- I_{S1} —switch S_1 current;
- I_{D1} —diode D_1 current;
- I_{V_o} —current through the final stage, which is the addition Of the currents through the output capacitor I_{C_o} and the Load I_o ;
- V_{S1} —voltage beyond switch S_1 ;
- V_{D1} —voltage beyond diode D_1 ;
- V_L —voltage beyond inductor L .

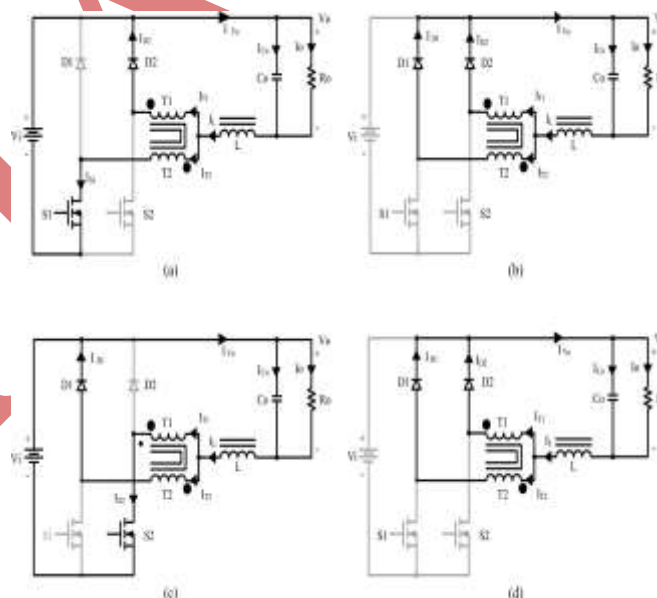


Fig.3. Operating Stages of the Proposed Converter in NOM-CCM
(A) First Stage. (B) Second Stage. (C) Third Stage. (D) Fourth Stage

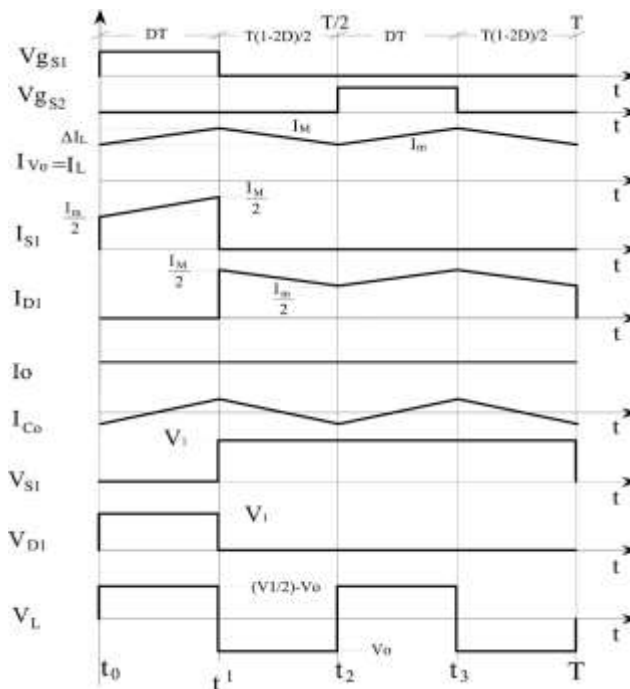


Fig.4. Main Theoretical Waveforms for NOM-CCM

First stage $[t_0, t_1]$ [see Fig. 3(a)]: At first, switch S1 is activated, while switch S2 is deactivated. The current through the inductor is spitted in two parts. The first one allows the current through T1 and D2 with energy being transferred to the load. The second one allows the current through T2 and S1. Current sharing is developed since the number of turns for T1 and T2 are equal. The current through inductance L rises linearly. Windings T1 and T2 have the similar half of the source voltage V_1 . This stage ends when S1 is switched OFF. Second stage $[t_1, t_2]$ [see Fig. 3(b)]: Switch S1 is switched OFF, while switch S2 maintained OFF. Inverted voltage is generated by the inductor L. Diode D1 is forward biased while D2 maintained conducting. The energy stored in L at that time the first stage is then transferred to the load. The current flows through T1_T2, recording to the given terminals, what affects the magnetic flow in the core to be zero. The current returns to the source technique to the first stage. This stage finishes when S2 is switched ON. Third stage $[t_2, t_3]$ [see Fig. 3(c)]: By the poetry of the circuit, this stage is like as the first one, Even though switch S2 is switched ON replace and S1 maintained switched OFF. Diode D1 gets forwarding and D2 is reverse biased. Fourth stage $[t_3, t_4]$ [see Fig. 3(d)]: This stage is like as the second one, as the same approximated circuit and operating procedures are valid in this case.

IV. CONCLUSION

A dc–dc buck converter worked on the 3SSC has been proposed. When the 3SSC is applied, the current is delivers all the semiconductors. Advanced, only part of the energy from the input source allows through the active switches, while the remaining part is directly delivered to the load without being presented by these controlling switches, i.e., this energy is generated to the load through passive devices, like as transformer windings and the diodes. Despite the higher in the number of semiconductors, the current stages on these devices are reduced, working the use of cost-less switches and minimized control circuits because the isolated drive is not necessary like in the interlaced buck converter. Beyond of these waveforms, its use is limited for large-power more-current applications where the conventional technique may be necessary, while good current sharing is generated. The total losses are delivered among all semiconductors, mitigating the heat sink affects. The reactive parameters operate with doubles the switching frequency, with sufficient reduction in weight and



volume of such devices. According the operation in NOM ($D < 0.5$) and the similar ratings, the given characteristics can be notified with the 3SSC-based converter if differentiate with the traditional buck technique:

- 1) Higher number of semiconductor devices;
- 2) The conduction area in CCM is wider;
- 3) The harmonic current through the inductor is mitigated, also currents through the controlling switches;
- 4) Reactive parameters are developed for doubles the switching frequency, affecting the desired critical inductance to be lower, for instance;
- 5) Only 50% of the power is distributed to the load by the main control switches by the magnetic coupling between the transformer tapping windings. Besides, a main benefit of the implemented converter working in OM ($D > 0.5$) is the continuous nature of the input current, which is adversely discontinuous in the traditional buck converter, what may lead to the with the use of an input filter for some Special applications.

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