DESIGN AND IMPLEMENTATION OF LOGIC GATES USING FINFET TECHNOLOGY

G.Saranya[1], S.Jakkammal@Malarvizhi[2], K.Kalarani[3]

[1, 2] PG Scholar, [3.] Assistant Professor, Department of VLSI Design,
Theni Kammavar Sangam College of Technology, Tamilnadu, (India)

ABSTRACT

Scaling as one of the most important challenges from the technology viewpoint. The channel length of Field Effect Transistors (FETs) has passed from micrometers to tens of nano meters. However, drawbacks of scaling have the increase of short channel, parasitic, reliability and variability effects. To overcome the problems related to scaling, new transistor architectures have to be investigated. FinFET is the most promising double-gate transistor architecture to extend scaling over planar device. Multiple gates have better control over the SCEs. Particularly the FinFET technology provides superior scalability of the DG-MOSFETs compared to the planar MOSFET. Fin-FETs are predicted as one of the best possible candidates to replace the bulk MOSFETs. The FinFET technology power consumption compare with the CMOS technology. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. Analyzed different type of operation mode like Shorted Gate, Independent gate, and Low power mode.

Keywords: FinFET, Short Channel Effects (SCEs), Power Consumption, Logic gates, Different modes of operation

I. INTRODUCTION

The FinFET has been developed to overcome the problems faced by MOSFET. It is basically a multi gate Field Effect Transistor which has been scaled further of MOSFET. It has all properties similar to a transistor, but has some advantages on CMOS. As you can see the above figures, multiple drains and multiple sources, we can also use each pair of source and drain can be considered as a single transistor hence increasing the no of transistors in one FinFET.

MOSFET has some technical problems like i) short channel effects and ii) Corner Effect Corner .Effects has following problems: -

a) An enhancement of the leakage current at the edges of the active area adjacent to shallow trench isolation

b) Leakage enhancement is especially strong, if the gate electrode wraps around the corner of the active area

c) Corner effect leads to a not complete switching-off of the STI MOS transistors and worsens the transistor performance.

So to overcome the difficulty faced by traditional MOSFET, FinFET came into role and to make the transistors more efficient. Wider FinFET devices are built utilizing multiple parallel fins between the source and drain. Independent gating of the FinFET's double gates allows significant reduction in leakage current.

II MOSFET

Metal-Oxide-Semiconductor Field Effect Transistor is a three terminal device used for a variety of applications as per the requirement in different fields of electronics. It is used for amplifying or switching electronic signals. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type and is accordingly called an nMOSFET or a pMOSFET (also commonly NMOS, PMOS).

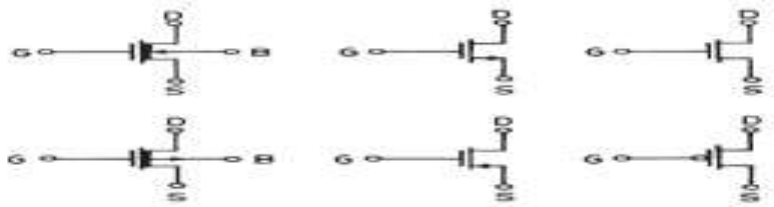

Fig.2.1 Symbols of NMOS & PMOS

G=GATE D= DRAIN S=SOURCE B = BULK

2.1 Operation of MOSFET

A traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a P-type semiconductor (with NA the density of acceptors, p the density of holes; p = NA in neutral bulk), a positive voltage, VGB, from gate to body creates a depletion layer by forcing the positively charged holes away from the gate insulator/ semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If VGB is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator.

Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage. This structure with P-type body is the basis of the N-type MOSFET, which requires the addition of an N-type source and drain regions.

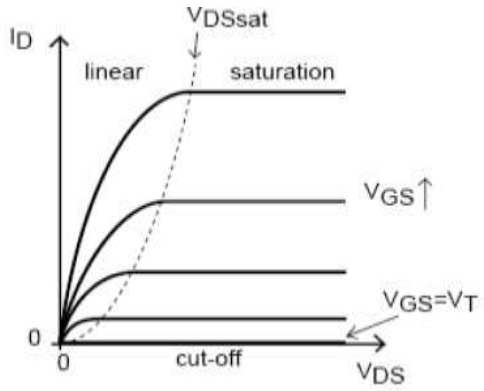

Fig.2.2: Operation of MOSFET

2.2 DG – MOSFET Structure

Currently standard CMOS technology can be replaced by DG MOSFETs technology to increase the integration capacity of silicon technology in the near future [5]. A DGSOI Structure consists, basically, of a silicon slab sandwiched between two oxide layers shows in Fig.2.3. The salient features of the DG MOSFETs are control of short-channel effects by device geometry, as compared to bulk FETs, where the short-channel effects are controlled by doping concentration; and a thin silicon channel leading to tight coupling of the gate potential with the channel potential. These features provide potential DG MOSFET advantages are reduced short channel effects which allows for a larger gate overdrive for the same power supply and the same off-current and better carrier transport as the channel doping is reduced.

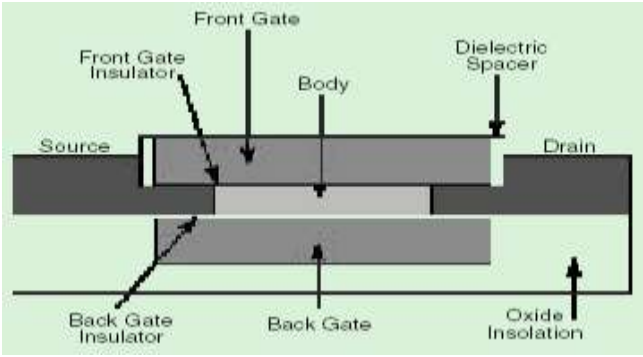

Fig.2.3: Cross Section of a Generic Planar DGFET

Basically there are 2 kinds of DG-FETs: (1) Symmetric: - In Symmetric DG-FETs have identical gate electrode materials for the front and back gates means gate electrode material is same for both gate. When symmetrically driven, the channel is formed at both the surfaces. (2) Asymmetric: - In an asymmetric DG-FET, the top and bottom gate electrode materials can different. Channel is formed only in one surface.

There are three ways to fabricate the DG-FET

- Planar DGMOSFET
- Vertical DGMOSFET
- FinFET

Types 1 and 2 suffer most from fabrication problems, viz. it is hard to fabricate both gates of the same size and that too exactly aligned to each other. Also, it is hard to align the source/drain regions exactly to the gate edges. Further, in Type 1 DG-FETs, it is hard to provide a low-resistance, area-efficient contact the bottom gate, since it is buried.

III PROPOSED METHOD

3.1 FINFET Structure Analysis

Type 3 is called as a FinFET because the silicon resembles the dorsal fin of a fish. It is referred to as a quasi-planar device (3D schematic diagram in Fig: 3.8). [14]In the FinFET the silicon body has been rotated on its edge into a vertical orientation so only source and drain regions are placed horizontally about the body, as in a conventional planar FET. The separate biasing in DG device easily provides multiple threshold voltages

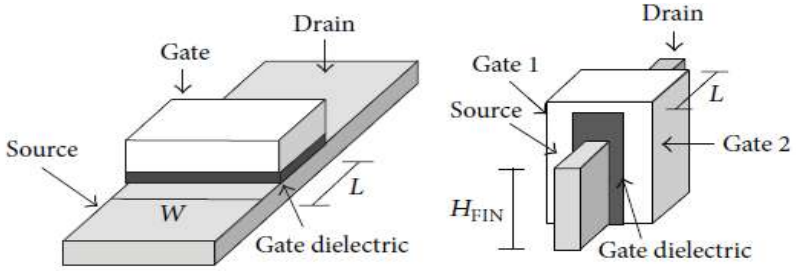

Fig.3.1 Planar MOSFET & FinFET

A gate can also be fabricated at the top of the fin, in which case it is a triple gate FET. The width of a FinFET is quantized due to the vertical gate structure. The fin height determines the minimum transistor width (*Wmin*). With the two gates of a single-fin FET tied together, W_{min} is

$$W_{min} = 2 \times H_{fin} + T_{fin} \qquad (3.1)$$

$H_{fin.}$ is the height of the fin and T_{fin} is the dominant component of the transistor width since T_{fin} is typically much smaller than $H_{fin.}$, Since H_{fin} is fixed in a FinFET technology, multiple parallel fins are utilized to increase the width of a FinFET. The total physical transistor width (W_{total}) of a tied-gate FinFET with *n* parallel fins is:

$$W_{total} = n \times W_{min} = n \times (2 \times H_{fin} + T_{fin}) \quad (3.2)$$

FinFETs are designed to use multiple fins to achieve larger channel widths. Source/Drain pads connect the fins in parallel. As the number of fins is increased, the current through the device increases [8].

Main features of FinFET are follows:

(1) Ultra thin Si fin for suppression of short channel effects

(2) Raised source/drain to reduce parasitic resistance and improve current drive

(3) Gate last process with low V_T, high k gate dielectrics

(4) Symmetric gates yield great performance,but can built asymmetric gates that target V.

The two vertical gates of a FinFET can be separated by depositing oxide on top of the silicon fin is shown in Fig: 3.1, thereby forming an independent-gate FinFET.

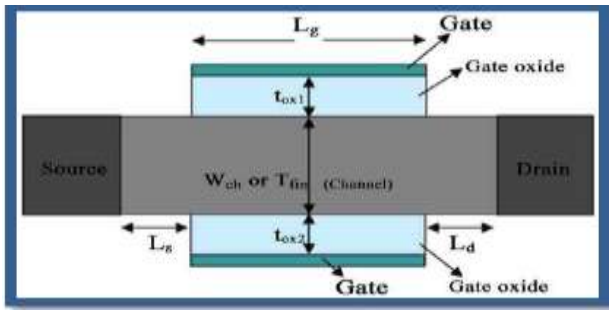

Fig.3.2 Independent-Gate FinFET

3.2 Construction of FinFET

The basic electrical layout and the mode of operation of a FinFET do not differ from a traditional field effect transistor. There is one source and one drain contact as well as a gate to control the current flow [5]. In contrast to planar MOSFETs the channel between source and drain is billed as a three dimensional bar on top of the silicon substrate, called fin. The gate electrode is then wrapped around the channel, so that there can be formed several gate electrodes on each side which leads to reduced leakage effects and an enhanced drive current. The manufacture of a bulk silicon-based multi gate transistor with three gates (tri gate) is described below.

Construction of a Bulk Silicon-based FinFET

1. Substrate: Basis for a FinFET is a lightly p-doped substrate with a hard mask on top (e.g. silicon nitride) as well as a patterned resist layer.
2. Fin Etch: The fins are formed in a highly anisotropic etch process. Since there is no stop layer on a bulk wafer, the etch process has to be time based.
3. Oxide Deposition: To isolate the fins from each other a oxide deposition with a high aspect ratio filling behavior is needed.

4. Planarization: The oxide is planarized by chemical mechanical polishing. The hard mask acts as a stop layer.
5. Recess Etch: Another etch process is needed to recess the oxide film to form a lateral isolation of the fins.
6. Gate Oxide: On top of the fins the gate oxide is deposited via thermal oxidation to isolate the channel from the gate electrode. Since the fins are still connected underneath the oxide, a high-dose angled implant at the base of the fin creates a dopant junction and completes the isolation.
7. Deposition of the Gate: Finally a highly n+-doped poly silicon layer is deposited on top of the fins, thus up to three gates are wrapped around the channel. one on each side of the fin, and - depending on the thickness of the gate oxide on top - a third gate above. The influence of the top gate can also be inhibited by the deposition of a nitride layer on top of the channel. Since there is an oxide layer on an SOI wafer, the channels are isolated from each other anyway. In addition the etch process of the fins is simplified as the process can be stopped on the oxide easily.

3.3 Three Modes of FINFET

3.3.1 Shorted Gate

The two gates are connected together, leading to a three-terminal device [1]. This can serve as a direct replacement for the conventional bulk-CMOS devices.

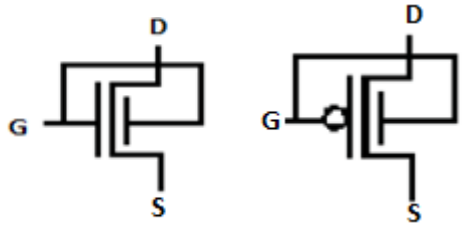

Fig.3.3 Shorted Gate for Both N-Type & P-Type

3.3.2 Independent Gate

The top part of the gate is etched out, giving way to two independent gates [2]. Because the two independent gates can be controlled separately, IG-mode FinFETs offer more design options.

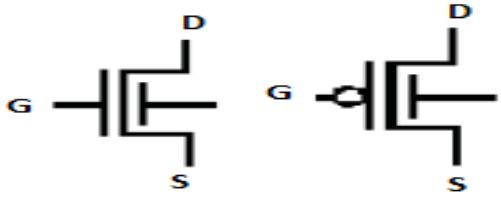

Fig.3.4 Independent-Gate for N-Type& P-Type

3.3.3 Low Power

A low voltage to n-type FinFET and high voltage to p-type FinFET. This varies the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay [1]. A hybrid IG/LP-mode is a combination of LP and IG modes.

3.4 FINFET Logic

3.4.1 Inverter

There are four possible configurations of an INV based on how SG and IG FinFETs are combined to implement them. They are called SG, low-power (LP), IGn, and IGp INV. Their schematic diagrams are shown in Figure 3.22&3.23. As suggested by its name, an SG INV has SG n/p FinFETs. It has a highly compact layout. The other three configurations use at least one IG FinFET. The back-gate of an IG p FinFET (n FinFET) is tied to a VHIGH (VLOW) signal. When these signals are reverse-biased, for example, when VHIGH is 1V above VDD and VLOW is 0 V below ground, there is a significant reduction in Ioff. [1]The presence of an IG FinFET also leads to a more complex layout, resulting in 36% area overhead relative to that of an ×2 SG INV (that is double the size of a minimum-sized SG INV). Table 2 compares the normalized area, delay, and leakage of the various INVs. Clearly, SG INV is the best in area and propagation delay (T p), but incurs much higher leakage current than LP INV. [9] However, LP INV performs poorly in area and propagation delay. IGn INV, however, looks promising based on its intermediate area, delay, and leakage.

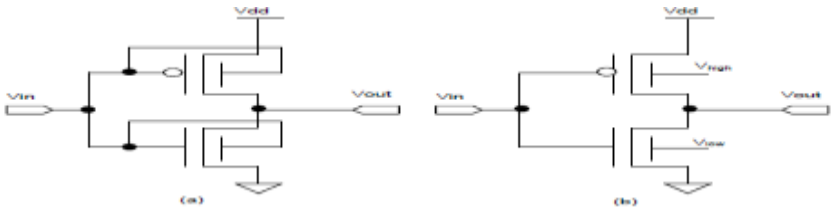

Fig.3.5 FinFET Inverter (a) Shorted gate & (b) Low power gate

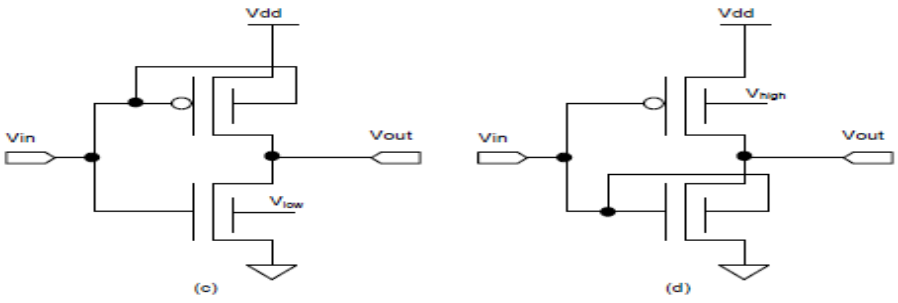

Fig.3.23 FinFET Inverter (c) Independent gate –N Type (d) Independent gate –P Type

3.4.2 NAND

Similar to INVs, NAND2 gates also have SG (LP) configurations in which all transistors are SG (IG) FinFETs. [9] Since there are more transistors in a NAND gate than in an INV, there are more opportunities available for combining SG and IG FinFETs.

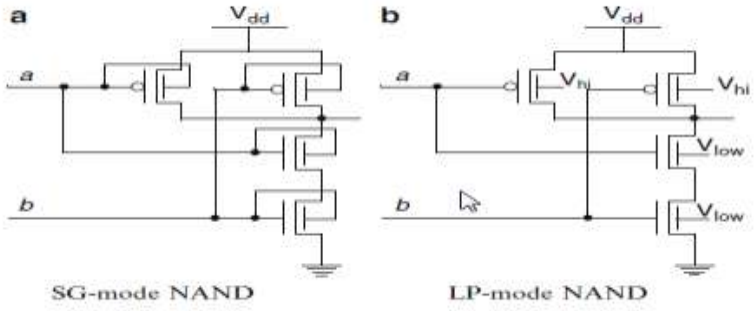

Fig.3.24: FinFET NAND circuit (a) Shorted gate & (b) Low power gate

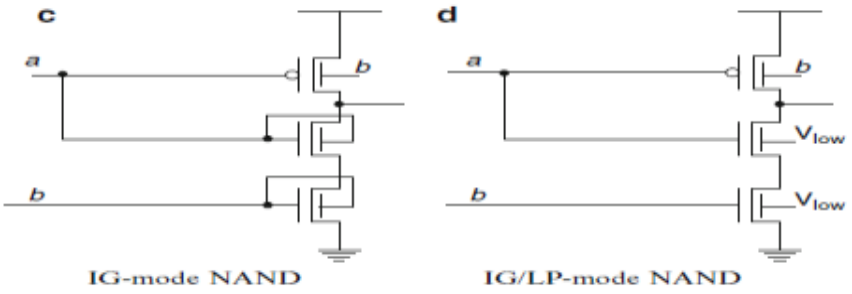

Fig.3.25: FinFET NAND (C) Independent gate & (b) Hybrid mode (IG/LP)

IV. ANALYSIS OF PERFORMANCE CHARACTERISTICS

Table.4.1 Performance Comparison of CMOS & FinFET Inverter

Device	Delay(S)	Power(W)	Bandwidth(G)	Power-Delay Product(PDP)(J)
CMOS	8PS	69µw	16.8G	552AJ
FinFET	7PS	72 µw	18.6G	504AJ

Table 4.1 shows that Performance comparison of CMOS & FinFET Inverter. Analysis describes that compare to CMOS; FinFET has fast switching speed and power delay product also reduced. Leakage also reduced.

Table.4.2 Performance Comparison of CMOS & FinFET NAND

Device	Delay(S)	Power(W)	Bandwidth(G)	Power-Delay Product(PDP)(J)
CMOS	26PS	138µw	20G	3.5Fj
FinFET	20PS	134µw	25G	2.7fj

Table 4.2 shows that Performance comparison of CMOS & FinFET NAND. Analysis describes that compare to CMOS; FinFET has fast switching speed and power delay product also reduced. Leakage also reduced.

Table.4.3 Performance Comparison of different modes in FinFET Inverter

Device	Delay(S)	Power(W)	Bandwidth(G)	Power-Delay Product(PDP)(J)
Shorted	7PS	72 µw	19G	504AJ
Low power	13PS	34 µw	11G	442AJ
Independent-P Type	6PS	65 µw	10G	394AJ
Independent-n Type	14PS	55 µw	20G	770AJ

Table 4.3 shows that Performance comparison different modes of FinFET Inverter. Analysis describes that Shorted gate for high performance, Low power gate for greater driving strength, Independent gate for two different signals. Compare to Shorted gate, Low power and Independent gate has low power consumption.

Table 4.4 shows that Performance comparison different modes of FinFET Inverter. Analysis describes that Shorted gate for high performance, Low power gate for greater driving strength, Independent gate for two different signals. Compare to Shorted gate, Low power and Independent gate has low power consumption.

Table.4.4 Performance Comparison of different modes in FinFET NAND

Device	Delay(S)	Power(W)	Bandwidth(G)	Power-Delay Product (PDP)(J)
Shorted	20PS	134 µw	25G	2.7f
Low power	30PS	71 µw	20.5G	2.1f
Independent	18PS	83 µw	21G	1.4f
Independent/LP	28PS	68 µw	21G	1.9f

V. CONCLUSION

FinFET is a promising substitute for bulk CMOS for meeting the challenges being posed by the scaling of conventional MOSFETs. Due to its double-gate structure, it offers innovative circuit design styles. Logic gates are implemented in SG-, LP-, IG-, and IG/LP-mode of FinFET. FinFET offer faster switching speed and reduces the leakage current. Logic gates net lists are simulated using HSpice simulator. From the simulation result propagation delay, power consumption, bandwidth, and power delay product can be obtained. The future work will address the implementation of Adder circuit and memory device using FinFET because of its high performance.

REFERENCES

[1]. Ajay N.Bhoj and Niraj K.Jha, "Design of Logic Gates and Flip-Flops in High-Performance FinFET Technology" VLSI, IEEE Transactions on Volume:21

[2]. A. Muttreja, N. Agarwal, and N. K. Jha, "CMOS logic design with independent gate FinFETs," in Proc. Int. Conf. Computer Design, Oct. 2007, pp. 560–567.

[3]. Animesh Datta,Ashish Goal ,"Modeling & circuit synthesis for independently controlled double gate FinFET devices" IEEE Transcation, VOL 26,NO 11,2007

[4]. Dipanjan Sengupta and Resve Saleh ,"Generalized power-delay metrics in deep submicron cmos design",IEEE transaction ,VOL 26,2007.

[5] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures" Volume 2014

[6] E.J.Nowak, I.Aller, T.Ludwig, K.kim, R.V.Joshi, "Turning silicon on its edge (double gate cmos/FinFET technology)",IEEE transaction ,VOL 23,2004

[7] International Technology Roadmap For Semiconductors 2007 Edition Emerging Research Materials"

[8] J. P. Colinge, FinFETs and other Multi-Gate Transistors Springer, 2007.

[9] Lu.Z and J. G. Fossum, "Short-Channel Effects in Independent-Gate FinFETs," IEEE ELECTRON DEVICE LETTERS, vol. 28, no. 2, February 2007.

[10] Mohammad Yousefarei,"modeling symmetrical independent gate finfet using predictive technology model"IEEE transaction, 2013

[11] M. Rostami, and K. Mohanram, "Dual Vth independent gate FinFETs for low-power logic circuits," IEEE Trans. CAD of Int. Circuits and Systems, vol. 30, no. 3, March 2011.

[13] Predictive Technology model website Yu (Kevin) Cao, "Nano scale integration and modeling" (www.ptm.asu.edu)

[14] Roy K, Mukhopadhyay, S. ; Mahmoodi-Meimand, H. 2003,"Leakage current mechanisms and leakage reduction techniques in deep-submicrometer cmos circuits" IEEE transaction VOL 91,2003.

[15] Vaidy Subramanian, Bertrand Parvais, Jonathan Borremans, Abdelkarim Mercha," Planar Bulk MOSFETS versus FinFETs," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 12, 2006

BIOGRAPHICAL NOTES

MS.G.SARANYA is presently pursuing M.E final year in Electronics and Communication Engineering Department (specialization in VLSI design) from Theni Kammavar Sangam College of Technology, Theni, Tamilnadu, India.

MS.S.JAKKAMMAL@MALARVIZHI is presently pursuing M.E final year in Electronics and Communication Engineering Department (specialization in VLSI design) from Theni Kammavar Sangam College of Technology, Theni, Tamilnadu, India.

MS.K.KALARANI is working as an Assistant Professor in Electronics and Communication Engineering Department, from Theni Kammavar Sangam College of Technology, Theni, Tamilnadu, India.