

DESIGN AND IMPLEMENTATION OF A LOW VOLTAGE LOW POWER DOUBLE TAIL COMPARATOR

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ABSTRACT

Comparators are the basic elements for designing the modern analog and mixed signal systems. The speed and area is main factors for high speed applications. Various types of dynamic double tail comparators are compared in terms of Delay, Area, Power, Glitches, Speed and average time. The accuracy of comparators it mainly defined by its power consumption and speed. The comparators are mainly achieving the overall higher performance of ADC. The High speed comparators suffer from low voltage supply. Threshold voltage of the device is not scaled at the same time, as the supply voltage of the device. In modern CMOS technology the double tail comparator is designed by a using the dynamic method, it mainly reduces the power and voltage. The analytical expression method it can obtain an intuition about the contributors, comparator delay and explore the trade-off dynamic comparator design.

Keyword: *Double Tail comparator, ADC, Dynamic comparator, Glitches*

I INTRODUCTION

Comparators have essential influence on the overall performance in high speed analog to digital convertors (ADCs). In wide-ranging a comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Since comparators are usually not used with the feedback there is not compensation so neither the area reduction or speed reduction value is invited. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large quantity in A/D converter Dynamic comparators are widely used in the design of high speed ADCs. Due to speed, low power consumption, high input impedance and full swing output, the dynamic latched comparators are very attractive for many kinds of applications such as high speed analog to digital convertors (ADCs), memory sense amplifiers. Increasing packing densities coupled with faster clock frequencies has forced the issue of heat removal and power dissipation to the forefront of virtually every mainstream design application under the SUR. And the problem is predicted to continue to be a major challenge in the coming decade as we approach Giga Scale Integration (GSI) [1]. Analogue to digital conveners are one of the main building blocks of most portable electronic equipments, such as cell phones, electronics products. They increasing demand of longer battery life time of portable equipments has forced circuit designers to use lower supply

voltages. However the supply voltage is lowered the performance of analogue circuits is degraded and the design of low voltage analogue Circuits

This technique is very suitable for very-low power clocked and continuous time circuits such as level shifters, Op-amp and comparators. Design of a 10-bit supply boosted (SB) SAR ADC is presented as an example of the technique. Voltage design techniques such as clock boosting were also used. A unique supply and clock booster was designed as integral part of new supply boosted comparator. Input common mode range of SB comparator was extended by using supply boosted level shifter circuits [6]. Among the key performance metrics of a dynamic latch used in a voltage comparator is its input referred offset voltage. Relevant effects that contribute to the offset can be divided into static and dynamic components. The most commonly discussed source of static offset stems from threshold voltage mismatch in the constituent transistors. Two simple equations for predicting the offset were derived and compared against simulation data [7].

The degeneration resistors are the latching pair and it's to reduce transistor charging time for regeneration. Charging time, they allowing more time for regeneration. The introduction method consists of the emitter degeneration resistors in the latching pair. The degeneration resistors reduce the transistor charging time, providing more time for the critical process of regeneration. As the latching pair is isolated from the input nodes degenerates still improves the sensitivity when a preamplifier is used [8]. To overcome the challenges associated with to reduce the supply voltage, a double tail latched comparator with a variable capacitance, calibration technique they using a metal oxide metal capacitors is implemented. An all-digital time domain delay interpolation technique further enhances the resolution with very little additional power consumption [9].

II CONVENTIONAL DYNAMIC COMPARATOR

The double tail comparator achieves the better performance and the double tail comparator and the architecture it mainly used in the better performance used in the low voltage applications. The comparator designed based on double tail architecture. The main idea of this method is to increase $\Delta V_{fn}/f_p$ is to increase the latch regeneration speed. The main operation of the comparator is during reset phase $CLK = 0$, M_{tail1} and M_{tail2} is off, to avoiding these static power, M_3 and M_4 switches pulls both f_n and f_p nodes to V_{DD} . Hence the transistor M_{c1} and M_{c2} are cut off, intermediate stage transistors M_{R1} and M_{R2} is reset both latches outputs to ground. During decision making phase $CLK = V_{DD}$. M_{tail1} and M_{tail2} are on transistors M_3 and M_4 turn off. Furthermore, at the beginning of the phase, the control transistors are still off. Thus, f_n and f_p start to drop with different rates according to the input voltages. The second term, t_{latch} , is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of $V_{out} = V_{DD}/2$ has to be obtained from an initial output voltage difference V_0 at the falling output. This is a self biasing differential amplifier. An inverter was added at the output of the amplifier as an additional gain stage, to isolate any load capacitance from the self biasing differential amplifier.

The size of M_1 and M_2 are set by considering the differential amplifier's transconductance and the input capacitance. The transconductance sets the gain of the stages, while the input capacitance of the comparator is determined by the size M_1 and M_2 . Similar to the conventional dynamic comparator, the delay of this comparator

comprises two main parts, t_0 and t_{latch} . The delay t_0 represents the capacitive charging of the load capacitance C_L out (at the latch stage output nodes, Out_n and Out_p) until the first n-channel transistor (M_9/M_{10}) turns on, after which the latch regeneration starts; thus t_0 is obtained where I_{B1} is the drain current of the M_9 and approximately equal to the half of the tail current. Thus, it can be concluded that two main parameters which influence the initial output differential voltage and thereby the latch regeneration time are the transconductance of the intermediate stage transistors ($g_{mR1,2}$) and the voltage difference at the first stage outputs (f_n and f_p) at time t_0 .

III PROPOSED DOUBLE TAIL COMPARATOR

To achieve the better performance of double tail architecture in low voltage applications, the proposed method comparator is designed based on the double-tail structure

Operation of Proposed Comparator

1. Voltage is sense at the second stage input and the second stage latch regenerate output voltage Reset Phase: $Clk = 0$, M_{tail1} and M_{tail2} OFF. For this process static power is avoided. n_p and n_f nodes to VDD. Latches to be Ground.

2. Decision making phase: $Clk = VDD$, M_{tail1} and M_{tail2} are ON, M_3 and M_4 OFF.

During reset phase $clk=0$, M_{tail1} (M_3) & M_{tail2} (M_{20}) are OFF, M_{10} & M_{13} will pull both f_n & f_p nodes to VDD. Hence M_C (M_{11}) & M_C (M_{12}) are cut off, M_6 M_9 are discharge to output nodes to VSS. During an decision making phase $clk = VDD$, M_{tail1} (M_3) & M_{tail2} (M_{20}) are ON, transistor M_{10} & M_{13} will OFF and f_n & f_p nodes are start drop with different rates according to input voltage. $V_{INP} > V_{INN}$ means f_n is faster than f_p , M_{15} transistor provide more current than M_{14} . M_C (M_{11}) is turn on, f_p node pulling back to VDD M_C (M_{12}) remains OFF, f_n node discharged. Offset will low and delay reduced. Parallel connected dynamic latch is used as load of first stage to increase voltage difference due to cascade connection delay will more compare to parallel connection. The latch of this first stage start regenerating depending on the input differential voltage (V_{in1} , V_{in2}), producing a large difference voltage. This difference Out_1 and Out_2 . As fast sensing it is exploiting less time to produce output when compare to previous work. It consumes less power compared to conventional one. As the way delay has reduced.

IV EXPERIMENTAL RESULTS

Existing Model

In order to compare the proposed comparator with the conventional and double tail dynamic comparator all circuits have been simulated in a 130nm CMOS technology the post layout simulation have been simulated in Tanner EDA which is used to calculate the area of the conventional dynamic comparator as shown in Fig 1, Double tail dynamic comparator as in Fig 3 and proposed double tail dynamic comparator.

Circuit Diagram

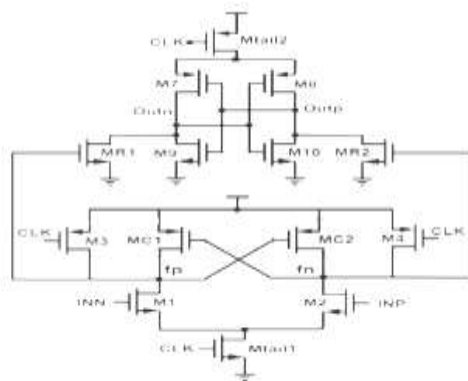


Fig .1 Existing Dynamic Comparator

Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistor to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors *M3* and *M4* of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors *M5* or *M6* to start complete regeneration.

Graph Output

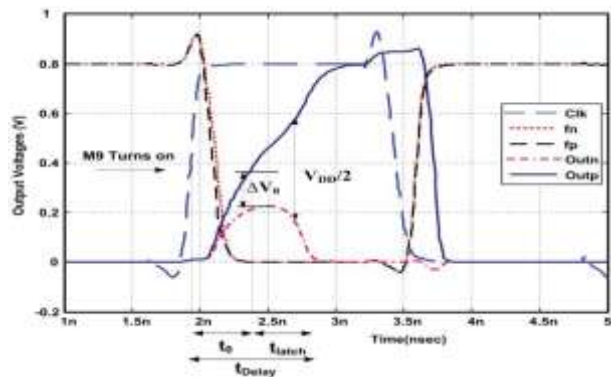


Fig.2 Energy diagram of existing system.

Proposed Method

As long as *fn* continues falling, the corresponding PMOS control transistor (*Mc1* in this case) starts to turn on, pulling *fp* node back to the VDD; so another control transistor (*Mc2*) remains off, allowing *fn* to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which V_{fn}/f_p is just a function of input transistor transconductance and input voltage difference in the proposed structure as soon as the comparator detects that for instance node *fn* discharges faster, a PMOS transistor (*Mc1*) turns on, pulling the other node *fp* back to the VDD.

Circuit

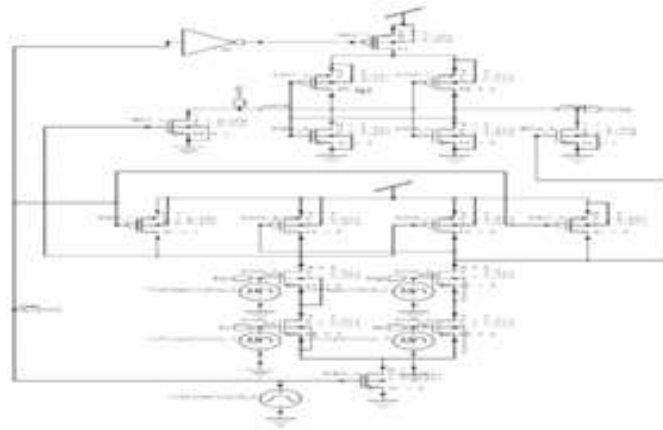


Fig 3 Proposed Circuit

Therefore by the time passing, the difference between f_n and f_p (V_{fn}/f_p) increases in an exponential manner, leading to the reduction of latch regeneration time.

It is evident that the double-tail topology can operate faster and can be used in lower supply voltages, while consuming nearly the same power as the conventional dynamic comparator. The case is even much better for the proposed comparator when compared to the conventional double-tail topology.

Parsing	0.10 seconds
Setup	0.01 seconds
DC operating point	0.00 seconds
Transient Analysis	1.14 seconds
Overhead	2.01 seconds
Total	3.26 seconds

Simulation Graph

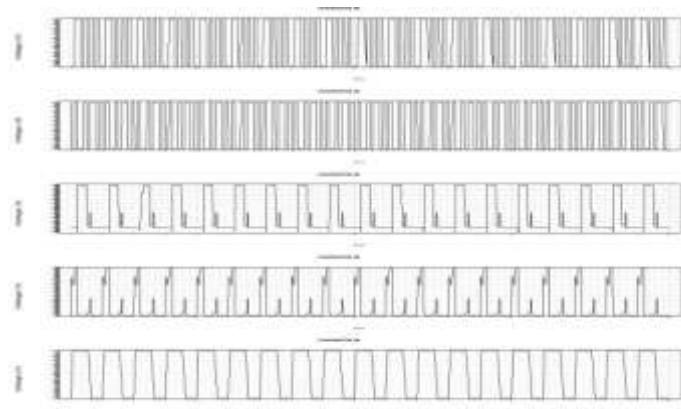


Fig.4 Proposed Output

V CONCLUSION

This work presents that comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators have been analyzed. A new dynamic comparator with low-voltage low-power capability has been proposed in order to improve the performance of the comparator and also reduces the delay. The area estimation is evaluated using post layout simulation with the help of micro wind simulator.

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