DESIGN AND ANALYSIS OF LOW POWER CHARGE PUMP CIRCUIT FOR PHASE-LOCKED LOOP

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ABSTRACT

CMOS is used to construct the integrated circuits with low level of static leakage. With this low level leakage we are designing all the transistor circuits in CMOS logic. To control this static leakage in the circuits the supply voltage is a major concern. Here the step-up converters with charge pump and the level for maintaining its threshold voltage (V_T) is to be analyzed and proposed. Here we are going to propose the novel approach as body bias effect and sub-threshold logic. This will be applied for the step-up converters for energy harvesting applications. The backward control is to be processed for control the internal voltage when the charge transfer switch could be in activation. This will be used to boost the voltages from the circuit for step-up converters. When the supply voltage is to be raise from the fixed voltage level it will be turn OFF the transistor. The maximum level of the converters circuits contain the branch A and branch B which could be contains all p-MOS and n-MOS combinations. The oscillator circuit also to e designed and applied to the proposed six stage charge pump circuit to reduce the power consumption. To reduce the standby mode leakage we are designing the circuit by using power gating logic. These circuits are to be designed and verified by using the TANNER T-SPICE TOOLS.

Keywords: Body Bias, Sub Threshold, Linear Charge Pump.

I. INTRODUCTION

A charge pump circuit provides a voltage that is higher than the voltage of the power supply or a voltage of reverse polarity. In many applications such as Power IC, continuous time filters, and EEPROM, voltages higher than the power supplies are frequently required. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load and do not involve amplifiers or transformers. For that reason a charge pump is a device of choice in semiconductor technology where normal range of operating voltages is limited.

Charge pumps usually operate at high frequency level in order to increase their output power within a reasonable size of total capacitance used for charge transfer. This operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

The charge pump employs either low quiescent current Burst Mode operation or low noise constant frequency mode. In Burst Mode operation the charge pump VOUT regulates to –0.94 • VIN, and the Charge pump draws only 100µA of quiescent current with both LDO regulators on. In constant frequency mode the charge pump produces an output equal to –VIN and operates at a fixed 500 kHz or to a programmed value between 50kHz to 500kHz using an external resistor. The Charge pump is available in low profile (0.75mm) 3mm x 4mm 14-pin DFN and thermally enhanced 16-pin MSOP packages.

The charge transfer frequency can be adjusted between 50 kHz and 500 kHz using an external resistor on the RT pin. At slower frequencies the effective open-loop output resistance (ROL) of the charge pump is larger and it is able to provide smaller average output current. It can be used to determine a suitable value of RT to achieve a required oscillator frequency. If the RT pin is grounded, the part operates at a constant frequency of 500 kHz.

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II. EXISTING SYSTEM

2.1 Dickson Charge Pump

The Dickson charge pump and single cascade charge pump, shown in fig 1. , are derived from the ideal diode charge pump architecture. Both circuits output voltage obey equation that can be simplified as in equation.

$$Vout = VDD - Vth(0) + \Sigma [\alpha VDD - Vth(i)] \ldots\ldots (1)$$

$$Vout = VDD + n (VDD-Vth) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

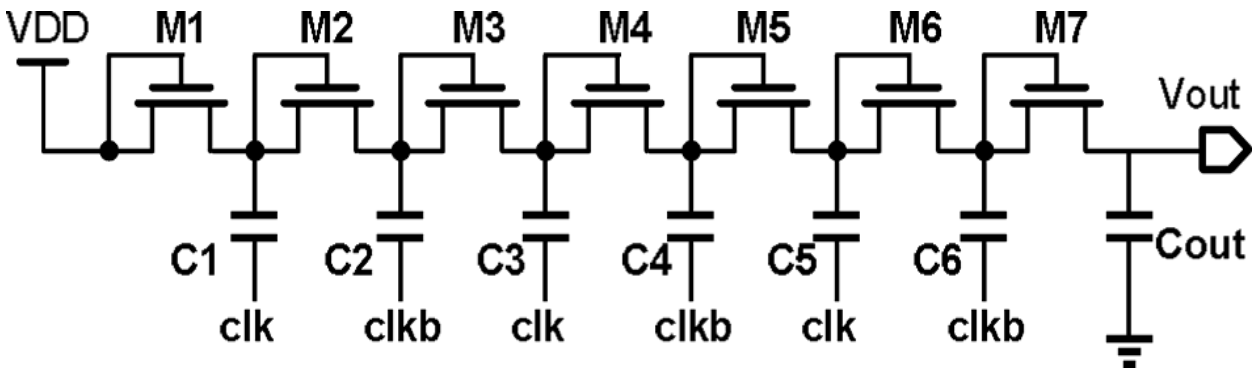

Fig 1. Dickson Charge Pump

The term VDD-Vth is called the voltage gain per unit stage. Note that this gain is additive and not multiplicative as in the voltage doubler architecture. In the Dickson charge pump, as the voltage of each stage increases, the threshold voltage of the diode-connected MOSFET increases due to body effect, and the voltage gain decreases as the number of stages increases. This effect is not present with the single cascade architecture. For large number of stages (>10), the Dickson charge pump has an average voltage gain of 0.25*VDD, while the single cascade circuit produces an average gain of 0.5*VDD.

2.2. Wu Chang Charge Pumps

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Six consecutive stages of the charge pump of are shown in Fig. 1. Assume the circuit is in steady-state. When CLK changes from 0 to VDD (when CLKB, the inverse of CLK, falls), the nth stage output, V, increases by CV and the voltages of neighboring stages reduce by the same amount. Consequently, the auxiliary NMOS switch, for the control of nth charge transfer switch, turns on by Vn-Vn-1 = 2CV and the PMOS switch, PMOS, turns off. Thus, V falls from Vn+1 to Vn-1 and turns off NMOS, and Vn-1 and Vn+1 rise to turn on the (n-1) th and (n+1) th charge transfer switches, PMOS and NMOS. Hence, the (n+1)th stage is charged up to the peak voltage of V. Similarly, when CLK falls (CLKB rises), Vn+1 is charged by CV. Thus, the output voltage of the charge pump with n stages is determined.

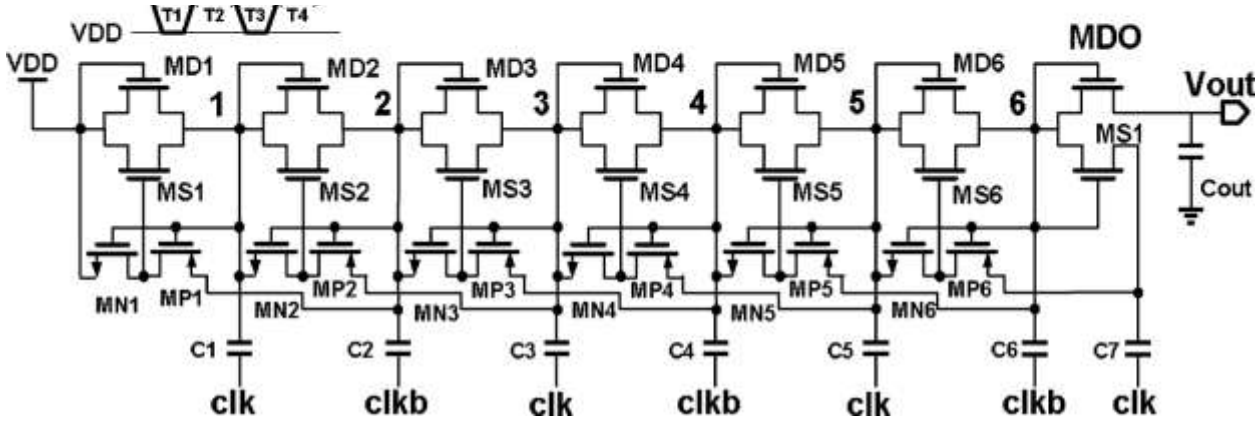

Fig.2 WU CHANG charge pump

Ideally, CV should be close to VDD. However, the parasitic capacitance at each node and the unwanted reverse currents cause CV to be smaller than VDD. Since the parasitic capacitance effect is not significant and can be overcome with ease by increasing unit capacitance Cu, the reverse current effect becomes the dominant loss factor.

2.3. Linear Charge Pumps

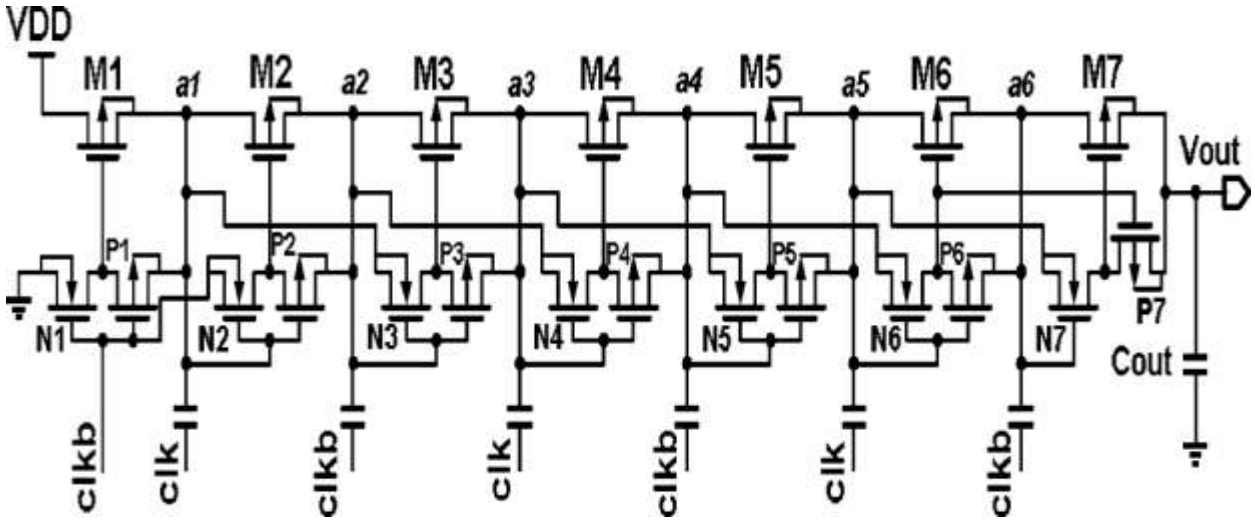

Fig.2 Linear charge pump

The charge pump was not an acceptable solution, until now .The minimum additional requirement was a linear regulator for stabilizing the output voltage. Newer charge pumps are regulated internally and can deliver substantially higher output currents. This way charge pumps are becoming more viable in applications that have been the domain of inductive DC/DC converter. This topic will give an overview on which topologies are used, how charge pumps are regulated and how external capacitors influence the performance of the system.

The main drawback of this topology is constituted by the parasitic capacitances which affect the behavior and performance more than the other topologies. Indeed, as demonstrated in, the reduction of the output voltage with respect to an ideal charge pump (i.e., without parasitic capacitances) strongly increases by increasing the number of stages. Moreover, another critical aspect concerns the switches implementation.

III. PROPOSED SYSTEM

The proposed two branch and six stages of charge pump has been analyzed and this could be uses the body bias effect and the backward control scheme for low power consumption and high amplification. Ignoring leakage effects, this effectively provides double the supply voltage to the load (the sum of the original supply and the capacitor). And also the Charge pumps offer high-efficiency and compact solutions for applications with generally low-output current requirements. This Regulated output charge pumps maintain a constant output with a varying voltage input. This high level of amplification gives the linear output of the all level implementation from the designed circuits. And also this proposed charge pump cannot give any errors or damage during the manufacturing process. The implementation level could be modified when we are designing this charge pump with more number of stages.

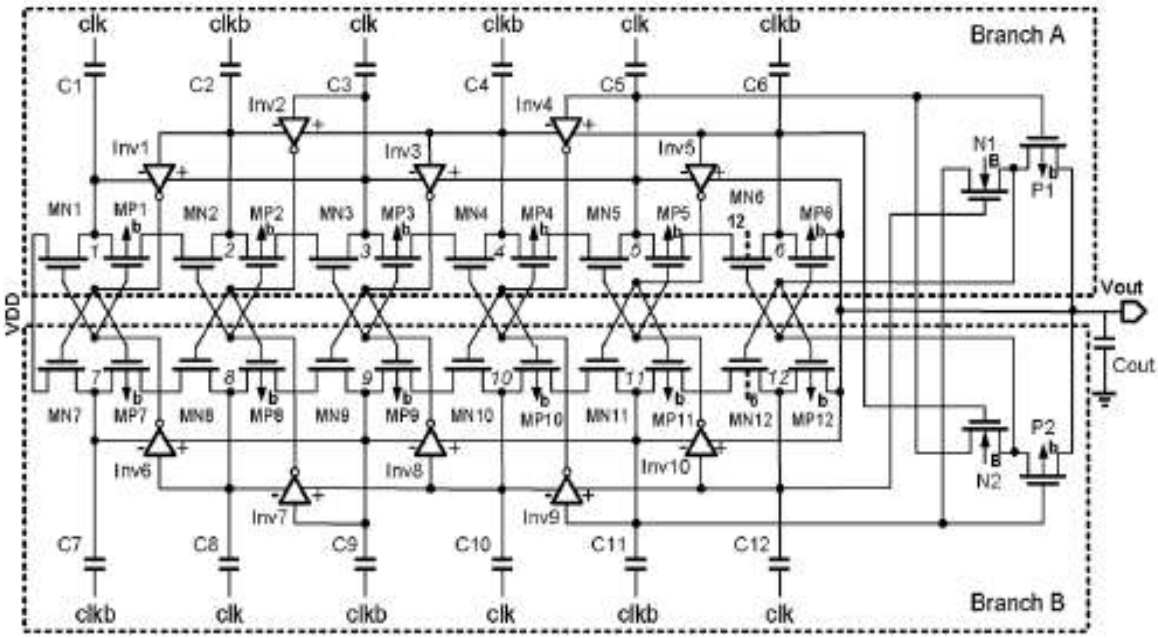

Fig.4 proposed charge pump circuit by using sub-threshold logic

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IV. SIMULATION RESULT

The new charge pump circuit is designed in TSMC CMOS process, simulated using T-Spice under a 2 mv power supply. This low voltage input supply gives the high amplification stages of the proposed charge pump. The operating frequency is 1000Hz and Fig. shows the charging and discharging result of the new charge pump circuit. The output voltage range is from 995mV up to 1010mV.

The parameter values has been analyzed and tabulated below. This could be a parameter gain of the all charge pump circuits with the input voltage and the output voltage variation of the all other degradations

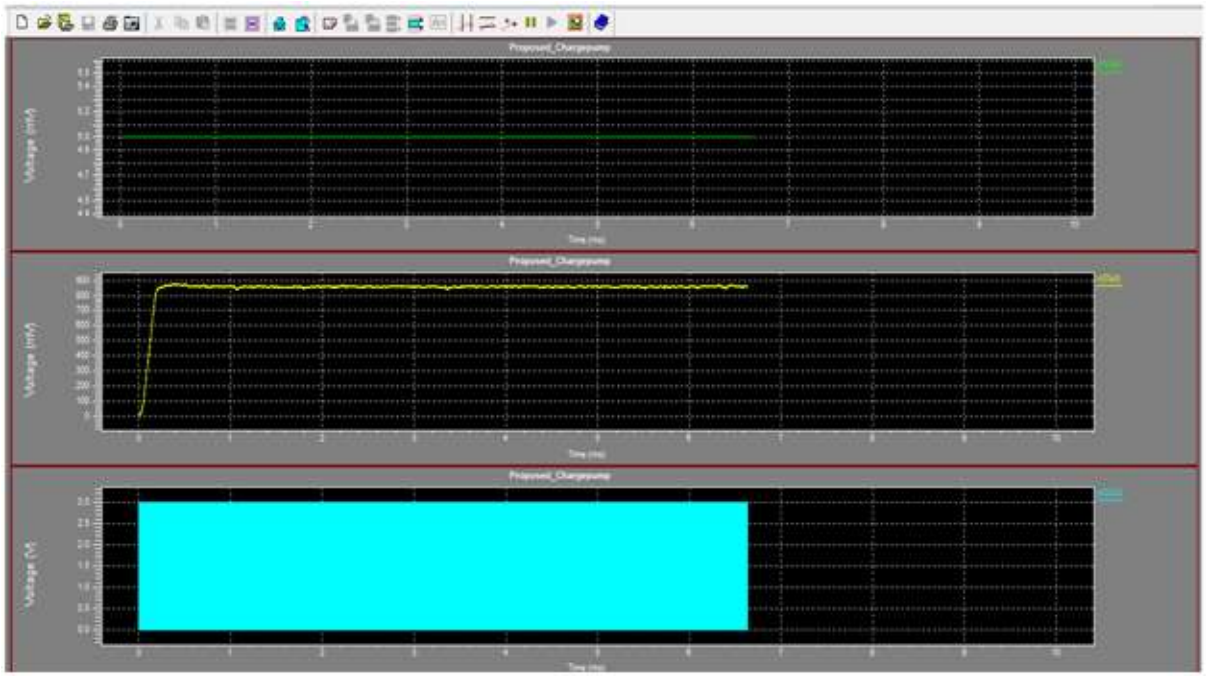

Fig.5 simulation result of proposed system

V. COMPARISION TABLE

CHARGE PUMP	POWER	AMPLITUDE
Dickson charge pump	8.60 W	50 mV
Wu_Chang charge pump	8.04 W	20mV
Linear charge pump	5.84 W	100mV
Proposed charge pump	3.29 W	1000mV

IV. CONCLUSION

Charge pump based on body biasing and the backward control scheme has been proposed in this system. The power and the amplification could be efficient when compared to the other existing charge pump. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test chip and get better performance. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the charge pump circuit so as to improve the power conversion efficiency. By using this efficiency calculation the pumping efficiency also calculated and gets the detailed configuration of the proposed charge pump parameter evaluation. The degradation of the amplification could be highly reduces and it could be generated as per the test identification stages proposed in the charge pump design circuit. This circuit could be further used for the implementation of the like PLL based analog devices.

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