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MINIMIZATION OF REDUNDANT INTERNAL VOLTAGE SWING IN CMOS FULL-ADDER

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ABSTRACT

In this paper a CMOS full-adder cell is proposed for low-power applications. The proposed logic structure of CMOS full-adder is used to minimize unnecessary internal voltage swing taken place in the prior CMOS full-adder by adding four nMOS transistors to the logic structure of SUM circuit and three nMOS transistors to the logic structure of CARRY circuit. These nMOS transistors are used to minimize the internal voltage swing from ($0 \rightarrow V_{DD}$) to (($0 - V_{tp}$) $\rightarrow V_{DD}$) during redundant internal voltage transitions. For area constrain applications, we can use these extra nMOS transistors either to the SUM or CARRY circuit depending upon our need. The proposed full-adder has maximum of 36ps longer data to output delay as compared to the prior CMOS full-adder. The full adder was designed with a 0.18μm CMOS technology.

Keywords: Delay, Dynamic Power, Full-Adder, Voltage Swing, Double Pass Transistor Logic.

I. INTRODUCTION

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. Thus a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.

The average power dissipation in digital CMOS circuits depends on

1) Dynamic power,

2) Short-circuit power,

3) Leakage power and

4) Static power.

The dynamic power dissipation is the dominant factor compared with the other components of power dissipation in digital CMOS circuits. As technology scales down, i.e. for submicron technologies, the contribution of dynamic power dissipation also increases because of increased functionality requirements and clock frequencies [1]. The dynamic power $P = CV^2f$ equation consists of three terms: voltage, capacitance and frequency. Frequency reduction is the best applied to signals with larger capacitance. One effective method of reducing switching frequency is to eliminate logic transitions that are not necessary for computation [2]. In this paper, the inputs to the nMOS transistors are blocked during redundant internal logic transitions taken place in existing

CMOS full-adder structure by adding extra nMOS transistors serially and thereby reducing the redundant internal voltage swing.

II. LOGIC STRUCTURE OF EXISTING FULL-ADDER

The logic scheme is shown in Fig.1 [4]. The true-table for a 1-bit full-adder is given in Table 1. Examining the true-table and by referring the logic scheme, it can be seen that for producing the SUM output, MUX 1 select the output of $A \oplus B$ value when C = 0 whereas it select the output of $\overline{A \oplus B}$ value when C = 1. Similarly for producing the CARRY output, MUX 2 select the output of A • B value when C = 0 whereas it select the output of A + B value when C = 1.

The features and advantages of this logic structure listed in [5] are as follows.

- There are not signals generated internally that control the selection of the output multiplexers. Instead the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.
- The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus the overall delay for larger modules where the C signal falls on the critical path can be reduced.
- The propagation delay for the SUM and CARRY outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this features is advantageous for applications where the skew between arriving signals is critical for a proper operation, and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.
- The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR
- Gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

In addition to the advantages, the important drawback we have found about the logic structure is explained below:

According to the logic scheme of CMOS full-adder, MUX 1 select the $A \oplus B$ value when C = 0 whereas it select the $\overline{A \oplus B}$ value when C = 1. But the logic structure of XOR continuously produces the output to net 1 (denoted in Fig.1) even when the input C = 1. Similarly logic structure XNOR produces the output to net 2 (denoted in Fig. 1) even when the input C = 0. It causes redundant logic transitions on net 1 and net 2. The logic structure of XOR/XNOR in the full-adder was implemented using doublepass-transistor logic style (DPL) and swing restored complementary pass transistor logic style (SR-CPL) [5]. However both logic styles suffer from redundant internal voltage transitions. Since net 1 and net 2 have higher capacitances (approximately half the oxide capacitances of pass transistors in XOR and XNOR logic, wire capacitances, and half the oxide capacitances of transmission gates) it causes higher power dissipation. It also follows for net 3 and net 4 (denoted in Fig.1). due to continuous operations done by AND and OR circuit. So we need to avoid this unwanted internal logic transitions without much degradation in performance.

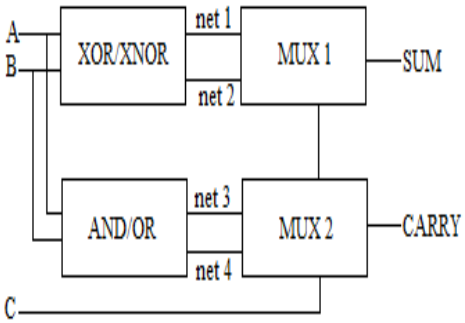

Fig-1: Existing logic scheme for designing full-adder cells.

TABLE I

True-Table For A 1-Bit Full-Adder

C	B	A	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

III. MODIFIED LOGIC STRUCTURE TO REDUCE REDUNDANT INTERNAL VOLTAGE SWING

Double Pass transistor Logic

DPL uses both PMOS and NMOS devices in the pass- transistor network to avoid non full swing problems. Double pass-transistor logic is shown to improve circuit performance at reduced supply voltage. Its symmetrical arrangement and double-transmission characteristics improve the gate speed without increasing the input capacitance. DPL gates are symmetrical whereby the

load in any DPL gate is distributed equally among the inputs. DPL XOR/XNOR gate is perfectly symmetrical.

The modified DPL logic of XOR and XNOR to produce the SUM output is shown in Fig.2. Here we added four nMOS transistors to the existing XOR and XNOR logic structure. The gate control of added nMOS transistors in XOR logic structure is $\overline{C}$ whereas in XNOR logic structure is input C. So that inputs to the nMOS transistors are blocked in XOR logic when the input C = 1 and in XNOR logic when the input C = 0. Thus switching transitions are taken place from $(0 - V_{tp}) \rightarrow V_{DD}$ instead of $0 \rightarrow V_{DD}$ during redundant operations (XOR output when C = 1 and XNOR output when C = 0). This minimizes the redundant voltage swing in net 1 and net 2. However this will increase the load for input C due to the increased gate voltages. But due to the smaller size of transistors the capacitive load will be smaller compared to thenet 1 and net 2. In addition, the input transitionprobability of input C is lesser when compared to the input transition probability of A and B. Similar actions are taken for net 3 and net 4

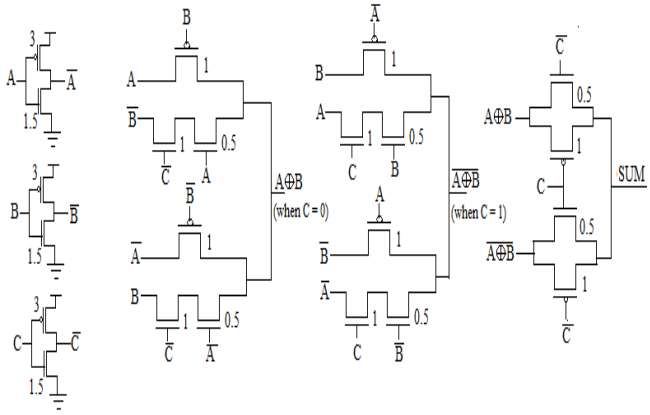

Fig-2: DPL logic of modified XOR and XNOR to produce the SUM output

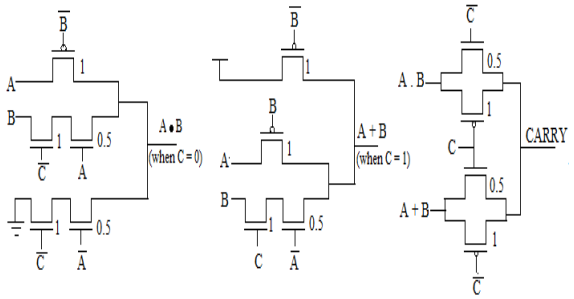

Fig-3: Modified AND and OR circuit to produce the CARRY output.

Three nMOS transistors are added to the existing AND and OR logic structure such that inputs to the nMOS transistors are blocked in AND logic when the input C = 1 and in OR logic when the input C = 0. The modified pass transistor logic structure to produce the CARRY output is shown in Fig.3.We control the inputs of nMOS transistors to avoid extra delay and to minimize area. However if we control the inputs of pMOS transistors the peak voltage on the nets will be reduced to (V_{DD}-V_{tn}) during redundant operations.

IV. PERFORMANCE COMPARISONS

- **Dynamic Power**

The average power dissipation of the circuit is expressed as

$$\mathbf{P_{average} = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage} + P_{static}} \quad (1)$$

$P_{dynamic}$ is the dynamic power dissipation due to switching of transistors. $P_{dynamic}$ is caused by the charging and discharging of capacitances in the circuit.

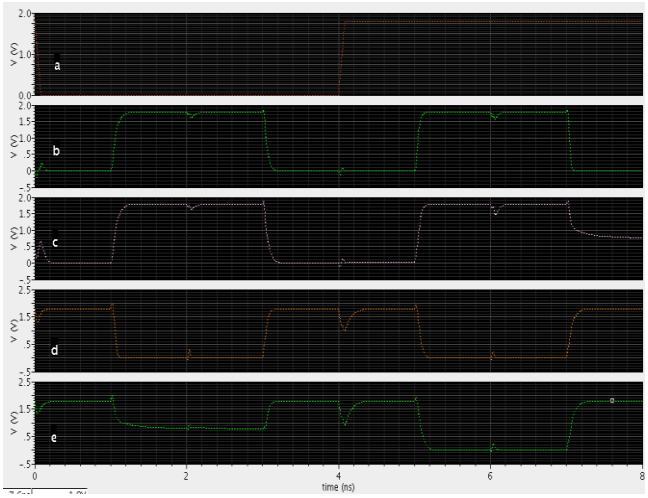

Fig-4: a) Input voltage C b) existing XOR logic output to net 1 c) modified XOR logic output to net 1 d) existing XNOR logic output to net 2 e) modified XNOR logic output to net 2.

$$P_{dynamic} = C_L.V_{DD}^2.N\ (0 \rightarrow V_{DD}).f \quad (2)$$

In the above equation N ($0 \rightarrow V_{DD}$)is the number of rising transitions at the output or equivalently the number of times C_L is charged to V_{DD}. Fig.4 shows the existing and modified output voltages of net 1 and net 2 with respect to the input voltage C. Fig.5 shows the existing and modified output voltages of net3 and net4 with respect to the input voltage C. The inputs C, B and A are as per the true-table (i.e. $000 \rightarrow 111$). V_{DD} for the operation is 1.8 V. For redundant operations (XOR and AND logic output on net 1 and net 3 when C = 1, XNOR and OR logic output on net 2 and net 4 when C = 0) in the modified logic structure the equation (2) is modified as

$$P_{dynamic} = C_L.V_{DD}^2.N\ ((0 - V_{tp}) \rightarrow V_{DD}).f \quad (3)$$

The capacitances on the net 1, net 2, net 3 and net 4 are charged to V_{DD} from $(0 - V_{tp})$ instead of 0 during redundant operations. This reduces the voltage swing which can be clearly seen from Fig.4 and Fig.5.

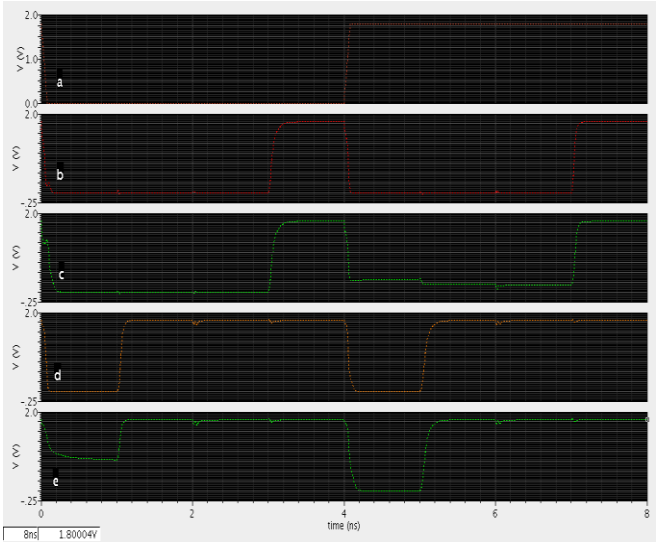

Fig.-5: a) Input voltage C b) existing AND logic output to net 3 c) modified AND logic output to net 3 d) existing OR logic output to net 4 e) modified OR logic output to net

The proposed full-adder can operate properly with voltage supply as low as 0.6 V. Since these realization have neither static consumption, nor internal direct paths from V_{DD} to Gnd (except for the inverters at the inputs, which could be avoided if the inputs come from Flip-Flop's with complementary outputs), they are good candidates for battery-operated applications where low consumption modules with standby modes are required. The transistors in the proposed full-adder are minimal and not largerthan 1 μm (except for the symmetrical response inverters at the input).

TABLE II Simulation Results of Full Adder Designs

S.NO.	Schemes Used	Dynamic power consumption (μw)	Delay (ps)	VDD min (V)
1.	Hybrid Pass logic	314.4	425	1.2
2.	Existing Method	109.2	289	0.6
3.	Proposed Method	92.82	325	0.6

- **Delay**

Due to the extra nMOS transistors the proposed logic structure of full-adder introduces a falling delay compared to the existing logic structure of full-adder. The maximum output delay associated with proposed full adder structure compared to the existing is only 36ps.

V. CONCLUSION

A modified logic structure is to reduce redundant internal voltage swing in CMOS full-adder cell was proposed. The proposed logic is used to minimize the voltage swing from ($0 \rightarrow V_{DD}$) to (($0 - V_{tp}$)$\rightarrow V_{DD}$) during redundant internal logic transitions. The outputs are simulated using Cadence virtuoso. The simulations showed that the proposed logic structure of full-adder is well suitable to low-power applications, and the power supply voltage can be lowered down to 0.6 V, maintaining proper functionality.

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