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VIDEO CODEC APPLICATIONS BASED ON ARCHITECTURE OF MULTI STANDARD VIDEO QUANTIZATION

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ABSTRACT

With the advent of video coding standards, such as Motion Pictures Expert Group (MPEG-2/4), Window Media Video 9 (VC-1), Advanced Video Coding (H.264/AVC),and Audio Video Coding Standard of China (AVS), there is an urgent need to integrate them into a single chip. Simply combining multi-standard codec circuits together will increase the silicon area and power consumption, which makes the design unacceptable. When looking deeply into the principle of encoding and decoding process, many sharing logic can be found. Therefore, through reconfigurations, different standards may be efficiently incorporated.In this paper the area of the video codec has been reduced at quantization level by sharing the components for all video standards (MPEG2/4,VC-1,AVS,H.26A).The division and multiplications done on the quantization are performed only by adders and shifters.

I. INTRODUCTION

For multi standard video codec design area reduction is done on three ways (i) by modifying trans form section (ii) by modifying quantization section (iii) by modifying motion estimation architecture. Already so many papers came for area reduction at trans form [5] the next step is quantization level. only few papers are came from this area [1],[2]&[3] .in this paper quantization area has been taken for each and every video standard separate quantization procedure is there While developing the architecture, we have carefully considered all the quantization (*Q*) coefficients of the *Q* tables of different standards and established a relationship between them. The quantization in MPEG-2/4 defined as the division of the DCT coefficient by the corresponding *Q*-values specified by the *Q*-matrices. On the other hand, the two most popular video standards, H.264/AVC and AVS exploit multiplication and shift operation for the purpose of quantization to avoid the division operation for reduced computational complexity. The quantization in VC- 1 is user-defined and similar to the process in MPEG-2 . Based on the observation, paper propose new multiquantizer architecture to support these five codecs.

II. GENERAL ALGORITHM FOR PROPOSED ARCHITECTURE

Step 1 : (w[i,j]<< r).MF[i,j], for i,j=0,1,2,…7,

Step 2 : q=p+(offset<<qbits)

Step 3 : y=q>> (n+qs bits),

If we apply the above algorithm to individual standards we can get the individual quantized value .here w is the transform co-efficient, MF is the multiplication factor.

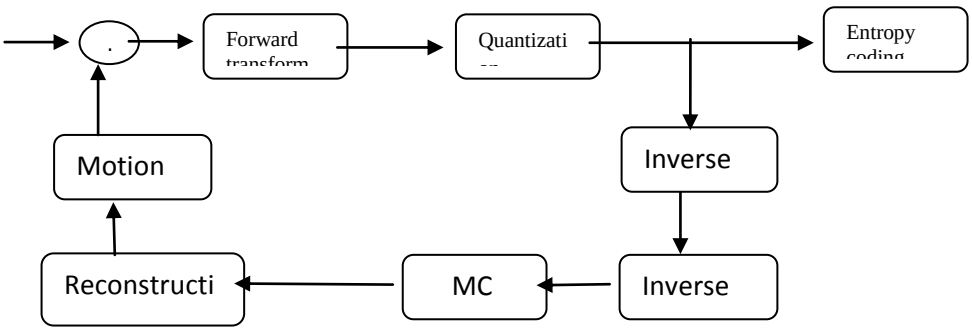

Fig.1 block diagram of video coder

TABLE 1: Description of different parameters of the proposed DFQA.

Parameters	AVS	H.264	VC-1	MPEG-2/4	JPEG
r	0	0	4	4	0
offset	1	0–0.5	0	0	0
*q*bits	14	16 + (QP mod 6)	0	0	0
n	15	16 + (QP mod 6)	8	8	8
*qs*_bit	0	0	5	5	0

The core unit of the multiquantizer unit, as shown in Figure 3, contains adder and shared right shifter. Right shift operation depends on the select standard pin. The look-up tables contain all the MF matrices for five standards. However, one look-up table is used at a time based on the specified standard. The multiplexer is used to select the valid data from the look-up tables. To reduce the power consumption, only one look-up table is activated at a time by the enable pin. Once the standard is chosen by the user, the desired look-up table is activated by the controller and all the other look-up tables go into the sleep mode. The control logic assigns the enable signal as well as the MUX selection signals. The quantization in MPEG2/4 and VC-1 uses only division but AVC ,H.26A and AVS uses multiplication and shifters only so to share the hardware for all video standards a common architecture is made which contains only multiplication and shifters instead of division and multiplication ,in this proposed architecture only adders and shifters are used this shared architecture and reducing the area.

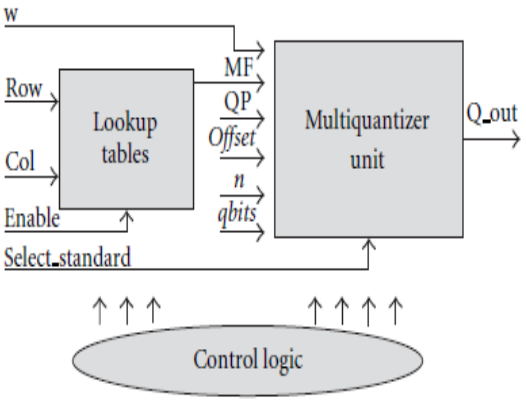

Fig .2 Quantization Unit

The overall architecture of the proposed algorithm can perform the 8 × 8 quantization of any of the five different standards as selected by the user using the select standard pin. The proposed architecture contains three main blocks with four-stage pipelining: (1) lookup tables to hold the multiplying factors (MF), (2)common adder and shifter (3) one finite state machine to control all the standards. The description of these blocks and their operations are described below. However, QP processing is not necessary for hardware implementation as it does not process data but calculates parameters used for data processing in the quantization block. Hence we assume that QP processing is previously done by software. The core unit of the multiquantizer unit, , contains adder and shared right shifter. Right shift operation depends on the select standard pin.

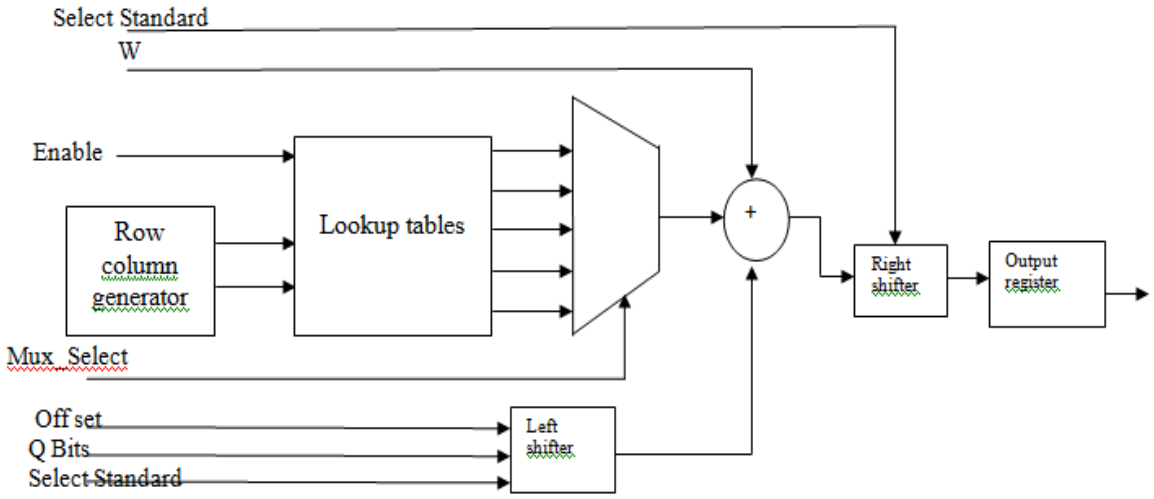

Fig.3 over all architecture

The look-up tables in Figure 2 & 3 contain all the MF matrices for five standards. However, one look-up table is used at a time based on the specified standard. The multiplexer is used to select the valid data from the look-up tables. To reduce the power consumption, only one look-up table is activated at a time by the enable pin. Once the standard is chosen by the user, the desired look-up table is activated by the controller and all the other look-up tables go into the sleep mode.

III. CONCLUSION

The proposed architecture is designed to support five video standards and implemented on FPGA which is using only adders and shifters due to division free hardware which is supporting multi video standards and area is further reduced by replacing the general purpose registers by adder and shifters. This shared architecture provide the multi quantization for modern video codec.

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