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A 7.3 GHZ LOW POWER TRUE SINGLE PHASE CLOCK CMOS 2/3 PRESCALER 247 µW

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ABSTRACT

In this paper a high operating frequency and power efficient TSPC prescaler layout is proposed and compared with the existing TSPC and E-TSPC prescalers on the basis of operating frequency and power consumption. The maximum operating frequency of the proposed TSPC prescaler is 7.3 GHz which is 10% higher than other prescalers with average power consumption of 309 µW at 1.8 V supply voltage. This High Frequency is achieved by reducing propagation delay in PMOS and NMOS at different stages. Unequal transistor width is taken for each NMOS and PMOS to receive equal propagation delay in pull-up network and pull-down network in each stage. The power consumption in divide by 2 mode is 3% and in divide by 3 mode is to 10% better than all other prescalers and four times better than those prescalers which can be operated higher than 6.5 GHz frequency. This prescaler consumes 349 µW in divide by 2 mode and 247 µW in divide by 3 mode.

Keywords: Dual modulus prescaler, D Flip-flop (DFF), Microwind, Propagation Delay,True single phase clock (TSPC).

I. INTRODUCTION

True Single phase Clock Dual modulus prescaler is an essential part of frequency synthesizer which generates variable frequency by using only one clock signal. Frequency synthesizers are digital circuits used to generate variable frequency which plays a major role in digital devices where multiple and/or variable clock frequency are required. Frequency synthesizers uses different techniques such as frequency divider, frequency multiplier and direct digital synthesizer. A high speed dual modulus prescaler frequency synthesizers is used in many electronic systems such as timing recovery circuit, clock generator etc.

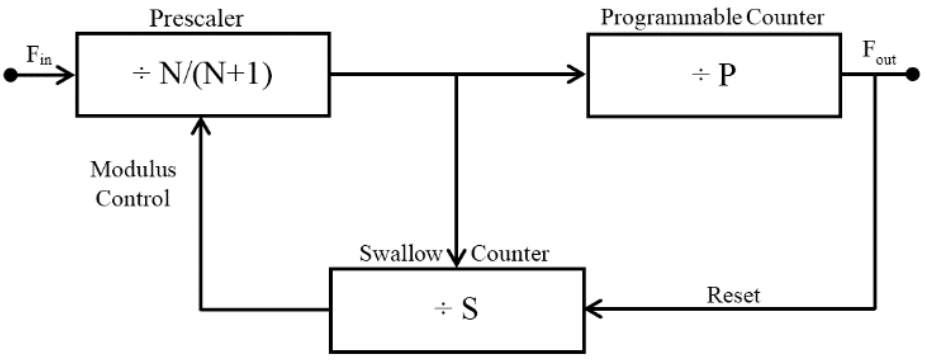

Fig. 1. Topology of the Pulse Swallow frequency divider

In a frequency synthesizer, prescaler consumes maximum power with respect to other components. By reducing the power consumption of prescaler it is possible to make a power efficient frequency synthesizer. A dual modulus prescaler uses a wideband swallow frequency divider and has N and N+1 division ratios. Frequency synthesizer produces variable frequency by using prescaler and control circuit. This control unit uses two counters, Programmable Counter (P) and Swallow Counter (S), it is shown in Fig. 1. The combination of Prescaler and counters P and S performs N × P + S programmable division ratio.

Basically prescaler are made of D flop-flop and logic gates. These D flop-flops can be driven by single phase clock [3], [4] or multiple phase clock. These logic gates are used between D flop-flops to generate two consecutive divisional ratios. In the prescaler the D flip-flops are controlled directly by clock signal so the speed of the circuit is dependent on the speed of logic gates and switching power also increases.

The CMOS N/ (N +1) current mode logic (CML) [6] based prescaler can be operated as high as 24 GHz [5]. But the major drawback of the prescaler is the large load capacitances which increases power consumption. On the other hand the injection locked frequency dividers (ILFDs) have very small locking range and it also required large chip area for injection locking circuit. While Dynamic CMOS needs very small chip area with low power needs.

II. ANALYSIS OF TSPC FLIP-FLOP

In this section TSPC [3], [7] based flip-flops are analysed with its power consumption and frequency response. In dynamic latch frequency synthesiser, multiple phase clock frequency synthesiser are better for compact circuits and these are more power efficient than single phase frequency synthesizer. The maximum operating frequency is also higher. But these are not good for complex and big circuits because these generally prone to the clock skewing problem. It is difficult to maintain equal electrical length of all the clocks signals in same phase difference through tracks to each component in entire device. That's why single phase clock frequency synthesiser are widely used for big and complex circuit.

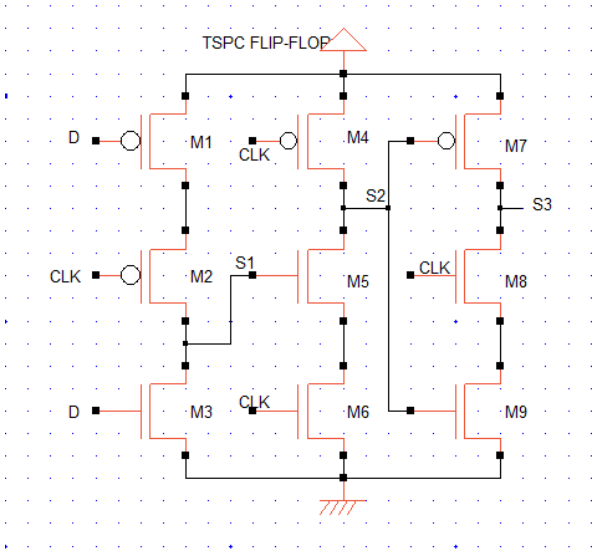

Fig. 2. TSPC flip-flop

The TSPC flip-flop have three stages to generate output from input. The TSPC flip-flop acquires three Transistors in each stage as in Fig. 2. The calculation of load capacitances is done by connecting output (Q) of the flip-flop with input (D). The load capacitance of TSPC according to method [8] and [9] is given by

$$C_{L_{TSPC}} = C_{DB_{M8}} + 2C_{GD_{M8}} + C_{DB_{M7}} + 2C_{GD_{M7}} + C_{G_{M3}} + C_{G_{M1}}$$

Equations shows that, the load capacitance of TSPC flip-flop which directly proportional to the switching power consumption which is given by

$$P_{switching} = f_{clk} C_L V_{dd}^2$$

Though the TSPC has higher switching power but ideally there is on direct path between supply voltage and ground during operation. As the transistors are not identical and PMOS and NMOS are not reciprocal as long as electrical properties are concerned, some power is consumed, it is called short circuit power. It also depends on rise and fall time of the input signals and clocks. The short circuit power [10] is directly proportional to the load capacitance. There is no direct path between each consecutive stages at the time of transition between supply voltage and ground, the TSPC flip-flop consumes negligible short circuit power. The short circuit power also dependent on the time for which a transistor is in floating state (neither high nor low) which increases with increasing frequency.

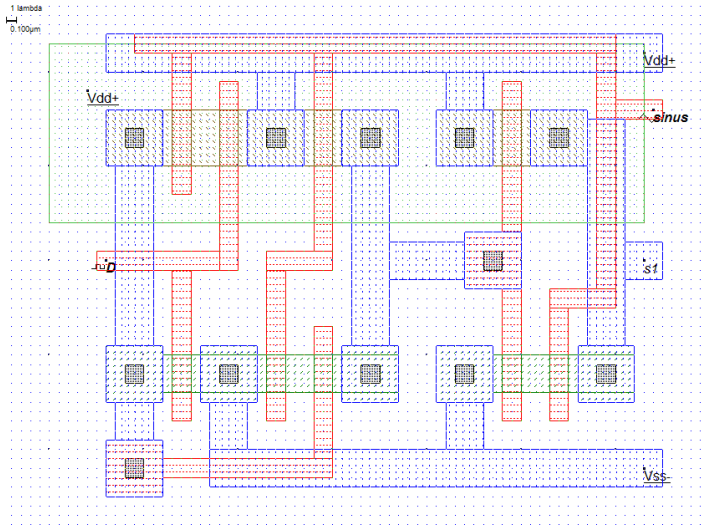

Fig. 3. TSPC flip-flop Layout

The circuit analysis is done by Microwind using 180nm technology at 1.8 Volts V_{dd}. The layout TSPC flip-flop shown in Fig. 3 are designed simulated with deferent DC levels and variable amplitudes at same 4 GHz frequency to find out dependency of circuits on output of VCO and also to analyse the power consumption. In simulation both circuits are tested on DC levels from 0.7 to 1.2 volts, and for each DC level, clock amplitude is also varied from 400mV to 700mV. The input is a 1 GHz signal with 50 ps of rise time and fall time. The simulation shows the power consumption of TSPC flip-flop varies from 50 to 65 µW for entire range of tested DC level and Amplitudes It is also observed that the output waveforms of TSPC flip-flop is quiet identical in all simulation.

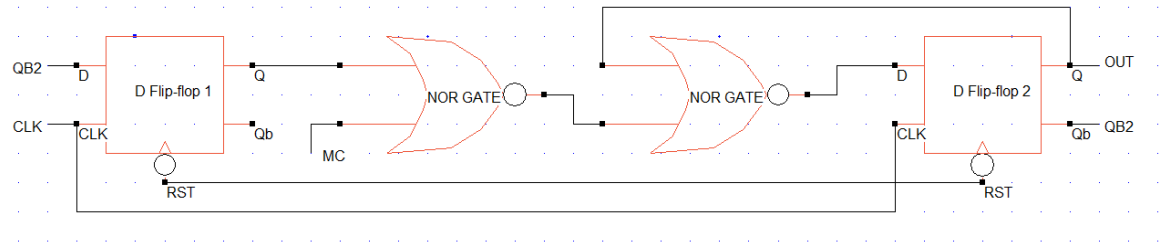

Fig. 4. TSPC 2/3 prescaler circuit proposed in [1]

III. ANALYSIS OF PROPOSED TSPC PRESCALER

In the 2/3 prescaler proposed in [1] shown in Fig. 4, the two NOR gates are implanted in to the flip-flops. This helped to reduce total number of transistors used to implement each NOR gate, as depicted in Fig. 5.The first NOR gate is embedded in to first D flip-flop using only one NMOS transistor M10 at the output node S3 in the third stage of flip-flop. This node S3 is connected to the second NOR gate which is embedded in to the first stage of second D flip-flop. This implementation reduced the additional stages introduced by an extra invertor used to invert the output of DFF1 and the digital gates between both the D flip-flops of the conventional TSPC 2/3 prescaler. This elimination reduced the total number of switching nodes from 12 to 7, and less number of nodes also reduced the switching power $P_{switching_[1]}$of prescaler, it is given by

$$P_{switching\_[1]} = \sum_{j=1}^{7} f_{clk} C_{Lj} V_{dd}^2$$

The total capacitance $C_{L\_[1]}$ of 2/3 prescaler of [1] at the output node Q is given by

$$C_{L\_[1]} = C_{DB_{M19}} + C_{DB_{M20}} + 2\left(C_{GD_{M19}} + C_{GD_{M20}}\right) + C_{G_{M11}} + C_{G_{M15}} + C_{G_{M22}} + C_{G_{M23}}$$

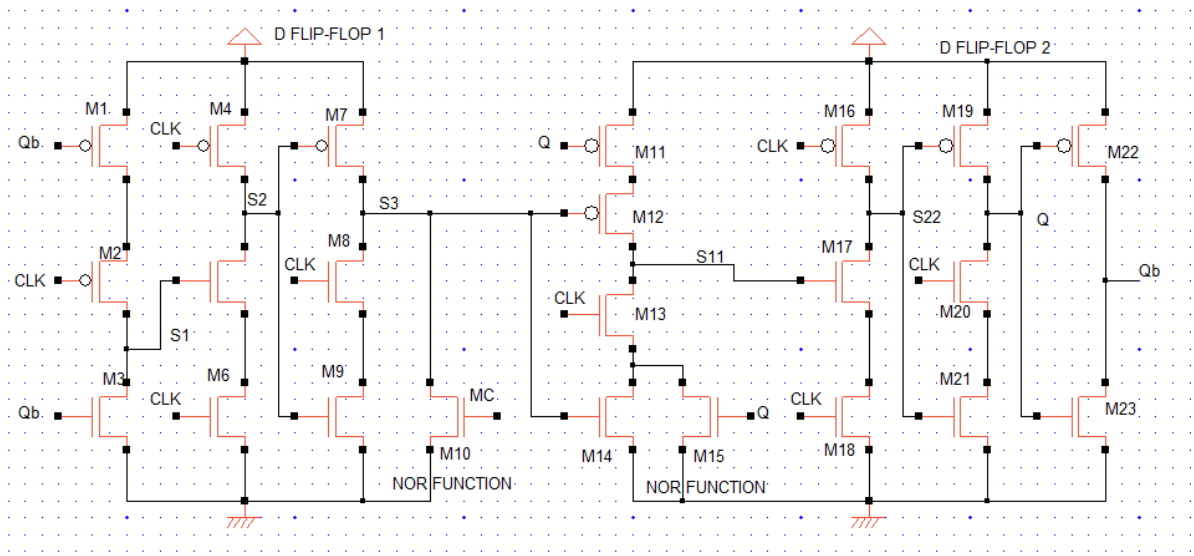

Fig. 5. Gate level schematic diagram of proposed TSPC 2/3 prescaler

In the proposed 2/3 prescaler the width of NMOS M3, M5, M6, M9, M10, M13, and M23 is 600nm and NMOS M14, M15, M17, M18, M20, M21 is 900nm. The width of the PMOS used to implement D flip-flop and Invertor is taken between 1000nm to 1400nm but for PMOS M11 and M12 it is taken 600nm to make a little

delay while feed-back cycle is low. This helped the circuit to significantly reduce power consumption in divide by 2 mode. These different width of each transistor is chosen to equalise the speed of electrons and holes in each stage which reduced propagation delay. This analogy is applied because the number of PMOS and NMOS is not equal in each stage. A TSPC stage either having two PMOS and one NMOS or one PMOS and two NMOS and also the mobility of electrons is much higher than holes so the width of PMOS is usually be higher than NMOS. Layout of Proposed 2/3 prescaler is shown in Fig. 6.

In both pull-up and pull-down networks which are driven by same input signal. It helped to reduce propagation delay difference between NMOS and PMOS of every stage driven by same input signal. This prescaler is almost three times power efficient and supports 58% higher operating frequency compared to that of the conventional TSPC 2/3 prescaler, And comparing with the [1] prescaler, it is 10% power efficient and supports 25% higher operating frequency which are verified by simulation results.

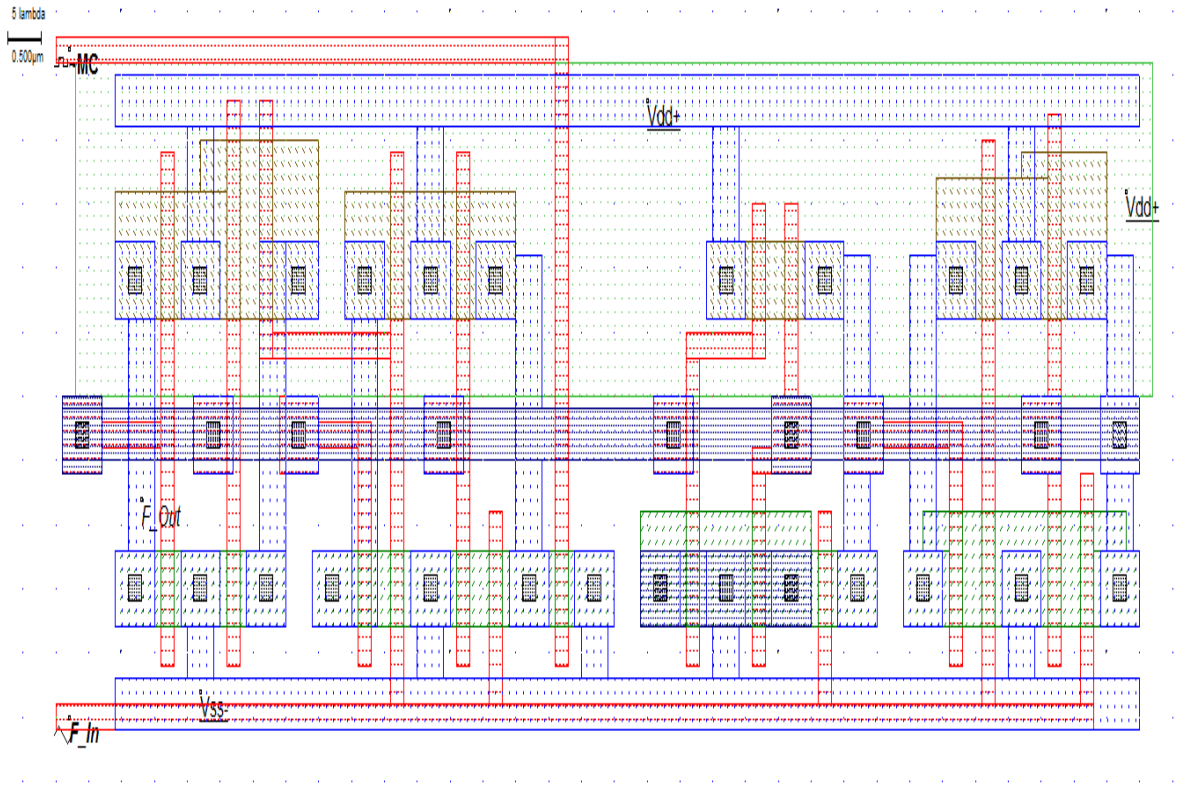

Fig. 6. Proposed Layout of TSPC 2/3 Prescaler

IV. SIMULATION AND MEASURMENT RESULTS

Microwind 3.5 software is used to perform all the simulations with 180nm CMOS Technology. All simulations are done by taking all parameters constant with 1.8 V supply voltage. From the simulation the [1] is most power efficient with 5.5 GHz operating frequency. While [2] can be operated up to 6.5 GHz which is highest for a TSPC based prescaler. In the simulation of proposed circuit an input sinusoidal signal of 7.3 GHz is applied as clock input on F_In with 0.9 V DC level is and 0.9 V peak to peak amplitude. Sinusoidal input signal is taken for simulation because on chip available VCO generates sinusoidal signal. And the Module Control input is feed

with a 100 MHz clock signal with 50 ps rise time and fall time to observe response in divide by 2 and divide by 3 mode and the output is taken from F_Out.

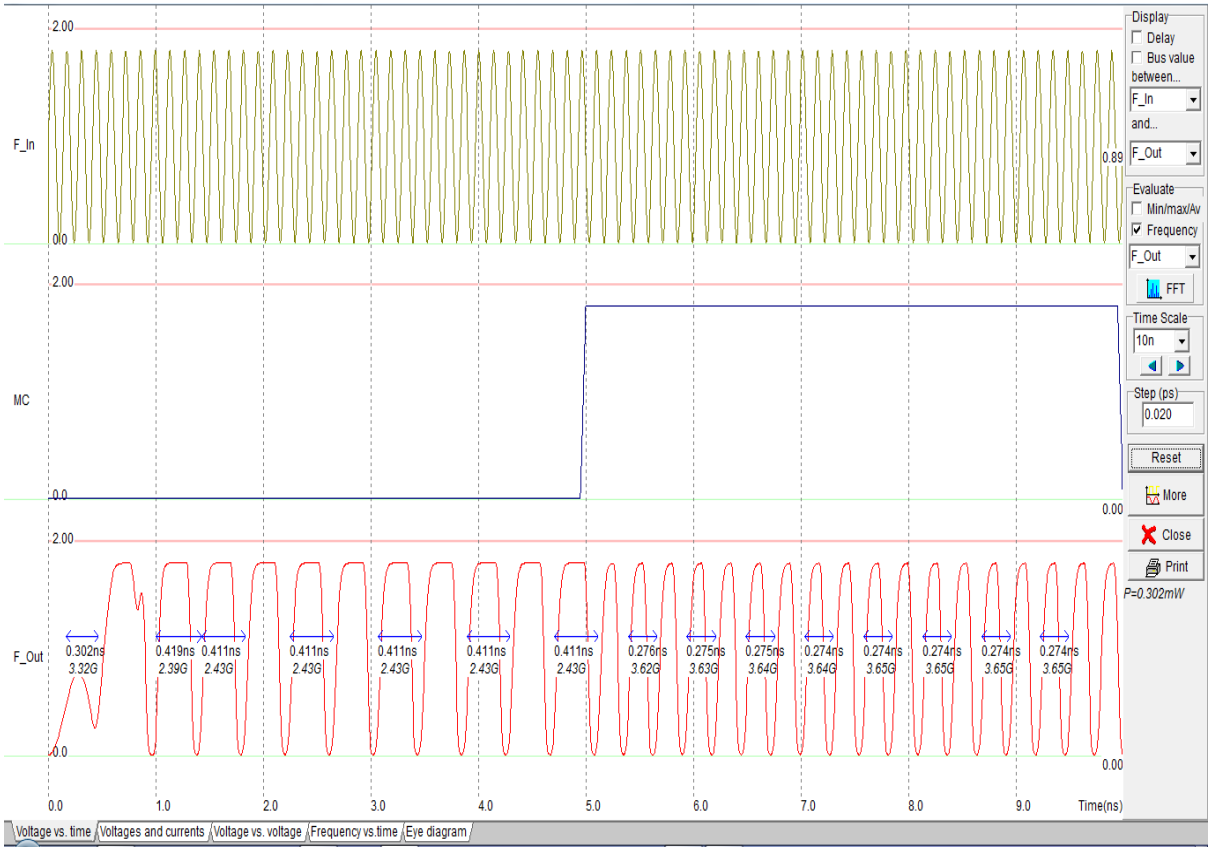

Fig. 7. Frequency response of Proposed TSPC 2/3 prescaler at 7.3 GHz

The frequency response shown in Fig. 7 shows that the circuit generates very stable output. In divide by 3 mode the output measured is 2.433 GHz and in divide by 2 mode the output measured is 3.65 GHz which is strictly proportional to the input clock frequency 7.3 GHz. The time delay, high time and low time are shown in Table 1 with power consumption and output frequency in both divide by 2 and divide by 3 mode.

Table 1. Simulation measurements of Proposed TSPC 2/3

Simulation Parameters	Output High time and Low Time (T_h/T_l) (ps)	Time Delay (T_r/T_f) (ps)	Power consumption (µW)	Output Frequency (GHz)
Divide-by-2 mode	75/70	12/24	349	3.65
Divide-by-3 mode	210/70	15/24	247	2.433

The time taken to produce stable output is less than 3 ns for both divide by 2 and divide by 3 mode. The average power consumption of the prescaler is 302 µW shown in Fig. 7. The power consumption in divide by 2 mode and divide by 3 mode are 349 µW and 247 µW respectively. The maximum operating frequency and power consumption of proposed prescaler is compared with different Prescalers, it is shown Fig. 8 and in Table 2.

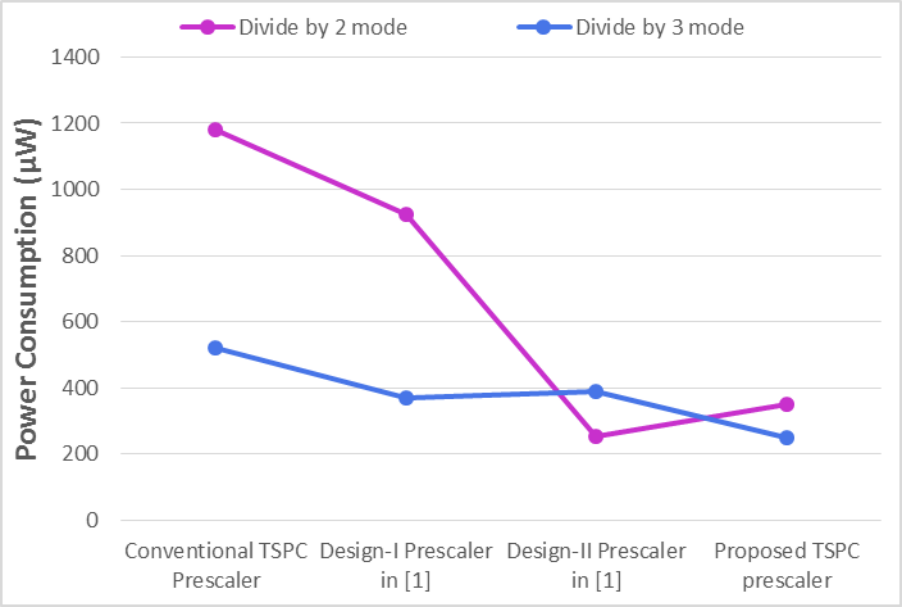

Fig. 8. Performance of different prescalers

Table 2. Maximum Operating Frequency & Power consumption comparison among different Prescalers

Design Parameters	Conventional TSPC Prescaler	Prescaler in [2]	Design-I Prescaler in [1]	Design-II Prescaler in [1]	Proposed TSPC Prescaler
Process (nm)	180	180	180	180	180
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.8
Maximum Frequency (GHz)	4.2	6.5	5.5	5.5	7.3
Power consumption (µW) Divide-by-2 mode	1182	1000	923	252	349
Power consumption (µW) Divide-by-3 mode	522	1800	369	387	247

V. CONCLUSION

In this paper a high frequency 2/3 prescaler is proposed which can operate up to 7.3 GHz which is 30% higher than the prescalers proposed in base paper, 10% higher than all other TSPC prescalers and 7% higher than E-TSPC based prescalers. The software used for all simulation is Microwind 3.5 with 180nm technology at supply voltage 1.8V. This proposed prescaler is not only supports high frequency but also consumes least power than all other TSPC and E-TSPC prescalers in both divide by 2 mode and divide by 3 mode. In divide by 2 mode it consumes 349 µW and in divide by 3 mode it consumes 247 µW. This prescaler also consumes four times less power than those prescalers which can be operated 6.5 GHz or higher frequency. This circuit is suitable for low power frequency synthesiser with high frequency response.

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