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A COMPREHENSIVE REVIEW ON FAULT – TOLERANT PARALLEL FILTER ESTIMATION

Priyanka Patel[1], Prof. Tarun Varma[2]

[1]Research scholar, [2]Assistant Professor, Department of Electronics and Communication
LNCT, Bhopal (INDIA)

ABSTRACT

Digital filters are ordinarily used in signal processing circuits and communication systems therefore these must be protected from set of errors more accurately.As complexity is continuously increasing , design and reliability engineers will demand to address several key areas to enable advanced SoC (System-on-chip) products in commercial sector. The first challenge will be to develop more accurate system level modeling of soft errors including not just device and component failure rates but architectural and algorithmic dependencies as well.Many techniques has been identified for error free circuit in which fault tolerant parallel filter using Error correction codes is latest.

Keywords – Digital Filter ,Error correction code,Fault Tolerant architecture.

I. INTRODUCTION

In electronic systems,filters are used to force signal in a particular frequency range.In signal processing, filters are the important device that removes unwanted data.In signal processing, a digital filter is a device or process that removes some unwanted component or feature from a signal. Digital filters are used for two general purposes; separation of signals that have been combined, and restoration of signals that have been distorted in some way. Most often, this means removing some frequencies and not others in order to suppress interfering signals and reduce background noise.. As the scale of integration increased from small/medium to large and to today's very large scale, the reliability per basic function has continued its dramatic improvement. Due to the demand for enhanced functionality, the complexity of contemporary computers, measured in terms of basic functions, rose almost as fast as the improvement in the reliability of the basic component. Secondly, our dependence on computing systems has grown so great that it becomes impossible to return to less sophisticated mechanisms. Previously, reliable computing has been limited to military, industrial, aerospace, and communications applications in which the consequence of computer failure had significant economic impact and/or loss of life. Today even commercial applications require high reliability as we move towards a cashless/automated life-style. Reliability is of critical importance in situations where a computer malfunction could have catastrophic results.

The cause for the fault-tolerant architecture being used is to accomplish a trust worthy design which is not given by fault intolerant design. The redundancy cost in computer system is main problem against using fault

tolerant techniques. High performance general purpose computing systems are very capable of being affected by transient errors and permanent faults. As performance demand increases, fault tolerance may be the only course to building commercial systems. The most important necessity for adaptation to non-critical failure is progressively control frameworks, where defective calculation could imperil human life or have high financial effect. Calculations must be right, and recuperation time from deficiencies must be limited. Specially designed hardware must be employed with fault-tolerance mechanisms so that incorrect data never leaves the faulty module.As the measurements and working voltages of electronic devices are decreased to fulfill the regularly expanding interest for higher thickness and low-power, their affectability to radiation increments drastically. A soft error arises in the system depend on their coverless against high energy radiation (cosmic rays, a particles, neutrons, etc.).

Soft errors in past were primarily a concern only in space applications. Significant single event arise because of a particle emissions radioactive elements found in packaging materials. Even though SEUs are the preponderant phenomenon, there are important instances in which multiple upset occur. Numerous event bombshells are those where an occurrence overwhelming ion can bring about a SEU in a string of memory cells, in a microcircuit, that happen to lie physically along the entrance particle track. The problem gets severe and recurrent with shrinking device geometry. Shorter channel lengths mean fewer number of the charge carriers, resulting in a smaller value of critical charge. The basic charge of a memory array memory cell is characterized as the biggest charge which is infused without changing the cell's original state. SEUs were at first connected with little and thickly stuffed recollections yet are currently ordinarily seen in combinational circuits and latches. Exponential development in the transistor's number in microprocessors,in addition to,signal processors which has increased rate of soft error generationly. The most effective method of dealing with soft errors in memory components is to use additional circuits for error detection and correction.

The IBM BlueGene system, featuring 106,496 computing nodes connected over a 3D torus direct interconnection network.Such huge networks are very susceptible to faults. Failures that occur in hardware is classified into hard failures, where the system's hardware

is physically broken, and transient faults. In a transient fault, the information that is hoarded in a system is altered, for example due to radiation or Gaussian noise on a channel. Within the last years, transient bit faults have maintained an almost constant fault rate per bit that is hoarded in memory or transmitted over cable. With an increasing complexity and size of computers, the probability of transient bit fault per system is increasing steadily. To keep the availability of parallel computers at a high level, error correction and fault-tolerance are becoming a very much essential issue. In the end, the error rate may rise at a level where high level error recovery becomes too costly if lower layers do not perform error correction that is transparent to the layers above.

A most efficient method of adding redundancy to computation is via an error-correcting code. Redundancy means to add extra bits with the data bits in the representation of data in the system. During error-free operation, the system's state remains within a fixed subset of valid states. If an error occurs, the system state is perturbed, and the redundancy is utilized to detect errors, much like fault-correcting code for a communication system. Standard fault-correcting codes are used to protect system's input matches the output. In general, these codes is not utilized for protection of system computation because their distance structure is destroyed during

computation. They have been successfully used to guard certain components of computer systems, such as buses and storage devices, where reliability is needed and no computation is performed. The central motivation behind the utilisation of arithmetic codes is to provide robust computation at low price than modular redundancy. Modular redundancy is always a workable alternative for protecting any computation and thus it serves as a benchmark for evaluating the efficiency with which arithmetic codes. Another important observation is that arithmetic codes protect the bulk, but not the entirety, of computation.Ifnecessary, these functions may be protected by modular redundancy.

Parallel FIR Filters

Signal processing, the function of a filter is to evacuate undesirable components of signal, for example, irregular clamor, or to extricate valuable component of the signal, for example, the segments existing in a specific frequency range. Filter forms two primary sorts ,analog and digital. They are very extraordinary in their physical cosmetics and by the process they work. A simple filter utilizes simple electronic circuits up from segments, for example, resistors, capacitors as well as operational amplifiers to create the needed filtering impact.A distinct time filter implements the following equation:

$$y[n] = \sum_{l=0}^{\infty} x[n-l].h[l] \dots\dots\dots\dots\dots\dots (1)$$

where x[n] is the input signal, y[n] is the output, and h[l] is impulse response of the filter. When the given response h[l] becomes nonzero, only for a given number of samples, the filter is known as a FIR filter, otherwise the filter is an infinite impulse response (IIR) filter. There are several structures to implement both FIR as well as IIR filters.

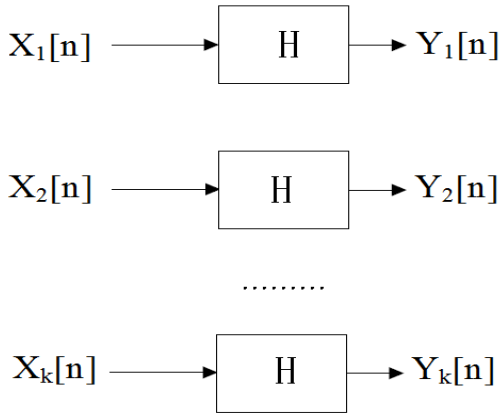

Fig.1 Parallelfilter with the same response.

In the following, a set of k parallel filters with the same response and different input signals are considered. These parallel filters are illustrated in Fig.1. This kind of filter is found in some communication systems that use several channels in parallel.

II. LITERATURE SURVEY

Z. Gao et al, 2015 [1] said that digital filters are ordinarily used in signal processing circuits and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters' structure and properties to achieve fault

tolerance have been proposed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel.

Z. Gao, W. Yang, X. Chen, M. Zhao and J. Wang,2012 [2] according to the Triple Modular Redundancy (TMR) scheme, the arithmetic residue codes based fault-tolerant DSP design consumes much less resources. However, the price for the low resource consumption is the fault missing problem. The basic tradeoff is that, smaller modulus used for the fault checking consumes fewer resources, but the fault missing rate is higher. The relationship between the value of modulus and the fault missing rate is analyzed theoretically in this research work for fault-tolerant FIR filter design, and the results are verified by FPGA implemented fault injections.

P. Reviriego, C. J. Bleakley and J. A. Maestro,2011 [3] The filters are specifically designed so that, when a soft error occurs, they produce distinct error patterns at the filter output. An error detection circuit monitors the basic filter outputs and identifies any mismatches. An error correction circuit determines which filter is in error based on the mismatch pattern and selects the error-free filter result as the output of the overall error-protected system. This technique is referred to as structural dual modular redundancy (DMR) since it enhances traditional DMR to provide error correction, as well as error detection, by means of filter modules with different structures. The proposed technique has been implemented and evaluated.

Y. H. Huang, 2010 [4] the research work proposes a subword-detection processing (SDP) technique and a fine-grain soft-error-tolerance (FGSET) architecture to improve the performance of the digital signal processing circuit. In the SDP technique, the logic masking property of the soft error in the combinational circuit is utilized to mask the single-event upset (SEU) caused by disturbing particles in the inactive area. To further improve the performance, the masked portion of the datapath can be used as the estimation redundancy in the algorithmic softerror-tolerance (ASET) technique. This technique is called subword-detection and redundant processing (SDRP). In the FGSET architecture, the soft error in each processing element (fine grain) can be recovered by the arithmetic datapath-level ASET technique. Analysis of the fast Fourier transform processor example shows that the proposed FGSET architecture can improve the performance of the coarse-grain SET (CGSET) by 8.5 dB.

Byonghyo Shim and N. R. Shanbhag,2006[6] Authors present energy-efficient soft error-tolerant techniques for digital signal processing (DSP) systems. The proposed technique, referred to as algorithmic soft error-tolerance (ASET), employs low-complexity estimators of a main DSP block to achieve reliable operation in the presence of soft errors. Three distinct ASET techniques - spatial, temporal and spatio-temporal- are presented. For frequency selective finite-impulse response (FIR) filtering.

M. Nicolaidis, 2005[7] Innanometric technologies, circuits are increasingly sensitive to various kinds of perturbations. Soft errors, a concern for space applications in the past, became a reliability issue at ground level. Alpha particles and atmospheric neutrons induce single-event upsets (SEU), affecting memory cells, latches, and flip-flops, and single-event transients (SET), initiated in the combinational logic and captured by the latches and flip-flops associated to the outputs of this logic. To face this challenge, a designer must dispose a variety of soft error mitigation schemes adapted to various circuit structures, design architectures, and design constraints. In this research work, Authorsdescribe various SEU and SET mitigation schemes that could help the designer meet her or his goals.

A. L. N. Reddy and P. Banerjee, 1990 [8] the increasing demands for high-performance signal processing along with the availability of inexpensive high-performance processors have results in numerous proposals for special-purpose array processors for signal processing applications. A functional-level concurrent error-detection scheme is presented for such VLSI signal processing architectures as those proposed for the FFT and QR factorization. Some basic properties involved in such computations are used to check the correctness of the computed output values. This fault-detection scheme is shown to be applicable to a class of problems rather than a particular problem, unlike the earlier algorithm-based error-detection techniques.

III. PROBLEM IDENTIFICATION

The method is based on the use of the ECCs. The decoders should perform higher either by following bit parallel operation or through running very high clock rate. Existing work has used hamming code as an ECC code, here system protection against set of errors is less, require large amount of system resources as used small parallel filter bank, decoding is not simpler**.** An arithmetic code must in addition be easily encoded and decoded, and must protect against the expected set of errors. These issues were only cursorily examined and not fully explored. however, that these issues are most important and that it is impossible to design a practical arithmetic codes without taking them into consideration. It is doubtful, though, that a general solution to this problem can be found. The set of expected errors is too closely linked to the architecture utilized to perform the processing, and varies greatly across systems. Also, in some cases, the application of fault tolerence filter reduces to a class of error-correcting codes for which these issues have not yet been fully resolved.

IV. CONCLUSION

Existing work has used hamming code as an ECC code, here system protection against set of errors is less, require large amount of system resources as used small parallel filter bank, decoding is not simpler. The proposed scheme can be used to explore the use of more powerful multibit ECCs, such as Bose-Chaudhuri-Hocquenghemcodes, to correct errors on multiple filters.The proposed scheme can also be applied to the IIR filters. Future work will consider the evaluation of the benefits of the proposed technique for IIR filters. This will be of interest when the number of parallel filters is small as the cost of the proposed scheme is larger in that case[1]. The extension of the scheme to parallel filters that have the same input and different impulse responses is also a topic for future work.

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