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Design of Area & Power Efficient Approximate Multipliers

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Abstract:-In brief, we proposed two approximate 16- bit multipliers for error resilient applications. In multiplier-1 we are approximating all Coolum's and in multiplier-2 approximating only in *15* least significant part. For this we aremodifying the partial products of the multiplier as *generate* and *propagate* signals. We are also using approximate adders,compressors to get efficient low power multiplier.After that we are comparing proposed multiplier with existing multiplier in all aspects like power,area and delay, and we showing how proposed multiplier gives best and efficient performance compared to others.we are using Xilinx 14.5 to simulate and compare all the multipliers with proposed one.

Keywords- multiplier; approximate circuit design; compressor; adders; image signal processing

I. INTRODUCTION

When we discuss about error resilient applications such as image signal processing, data mining,digital signal processing accurate results are not necessary.For this type of applications we can design circuits such as multipliers, adders and compressors with low power and less complexity with some modifications.Mainly in a multiplier design we have three parts

The Fast Multiplication Process

The speedy multiplication process consists of three steps:

• Partial product generation,
• PP'sminimizations and
• Final Carry propagating addition.

In the above steps 2nd one consumes more electricity and takes lot of area.So mainly are focusing on this one.We are reducing number of partial products by using approximation techniques.Up to now we are having different approximate multipliers.

In fixed width multipliers we are lowering the complexity through the usage of truncation but in this we are going through quantization errors. To compensate quantization error we are introducing a steady or vari-able correction term.

In Broken array multiplier the least good sized bits of inputs are truncated, whilst forming partial products to minimize hardware complexity. In dada multiplier we are minimizing no.of pp's by

using approximate compressor.The most important downside in this is it offers nonzero output for zero valued inputs, which generally influences the mean relative error (MRE).

. In this m*m multiplication is performed alternatively of n*n bit multiplication where (n>m) so that it decrease number of partial products in the multiplication process. In Wallace tree multiplier with the aid of using binary counter and compressor we can limit partial products. By using or gate in place of xor gate in approximation logic we can reduce the delay in most circuits

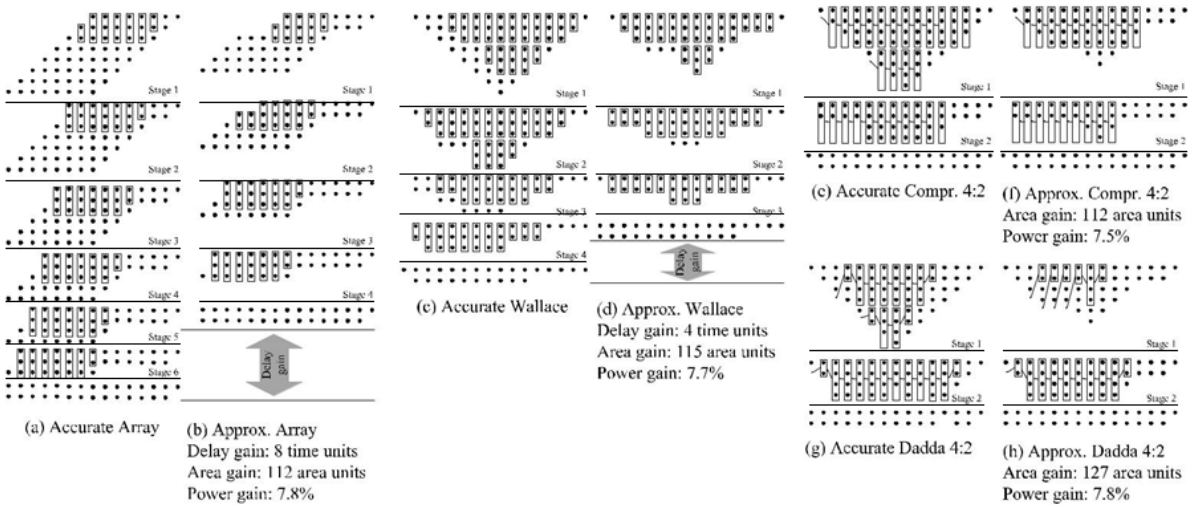

Fig. 1. Partial product reduction process for 8 × 8 multiplication with (a) accurate array, (b) approximate array, (c) accurate Wallace, (d) approximate Wallace, (e) accurate compressor 4:2, (f) approximate compressor 4:2, (g) accurate Dadda 4:2, and (h) approximate Dadda 4:2. Approximation is performed by perforating the third and fourth partial products. The boxes with four dots are 4:2 compressors, those with three are full adders and those with two are full- or half-adders.

Fig1:-DESIGN OF EFFICIENT APPROXIMATE MULTIPLICATION CIRCUITS

In proposed approximated multiplier we are altering the partial products and introducing new signals like propagate and generate in the place of partial products.After that we are approximating the generate signal depending on their places and the probability of error occurrence at that place by using Simplified arithmetic units (HA, FA, and 4-2 compressor). This arithmetic unit not only reduces the complexity but also consumes the less power.

Our proposed multiplier over come all the drawbacks existing multiplier multipliers in terms of area, power, and error, and achieves better peak signal to noise ratio (PSNR) values and (ED) error distance in image processing application .

So in this paper in section II we are discussing about proposed architecture in detail, in section II We are presenting the result analysis which gives the information about proposed multiplier advantages over existing multipliers.In section IV we are discussing how proposed multiplier is useful in image signal processing..

II.PROPOSED ARCHITECTURE

We are explaining proposed approximation method by way of taking A 8-bit unsigned multiplier as aexample.Let us assume two 8-bit unsigned operands two The partial product am,n = αm • βn in Fig. 2 is the end result of AND operation between the bits of αm and βn.

Table2:

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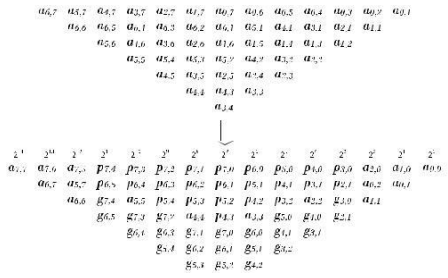

Fig. 2.conversion ofactual pp's into altered pp's.

Table1 Table3

PROBABILITY STATIS TICS OF*Generate* SIGNALS

m	Probability of the *generate* elements being				P_{err}
	all zero	one 1	two 1's	three 1's and more	
2	0.8789	0.1172	0.0039	-	0.00390
3	0.8240	0.1648	0.0110	0.00024	0.01124
4	0.7725	0.2060	0.0206	0.00093	0.02153

TRUTH TABLE OF APPROXIMATE HA

Inputs		Exact Outputs		Approximate Outputs		Absolute Difference
$x1$	$x2$	$Carry$	Sum	$Carry$	Sum	
0	0	0	0	0 ✔	0 ✔	0
0	1	0	1	0 ✔	1 ✔	0
1	0	0	1	0 ✔	1 ✔	0
1	1	1	0	1 ✔	1 ✗	1

TRUTH TABLE OF APPROXIMATE FULL ADDER

Inputs			Exact Outputs		Approximate Outputs		Absolute Difference
$x1$	$x2$	$x3$	$Carry$	Sum	$Carry$	Sum	
0	0	0	0	0	0 ✔	0 ✔	0
0	0	1	0	1	0 ✔	1 ✔	0
0	1	0	0	1	0 ✔	1 ✔	0
0	1	1	1	0	1 ✔	0 ✔	0
1	0	0	0	1	0 ✔	1 ✔	0
1	0	1	1	0	1 ✔	0 ✔	0
1	1	0	1	0	0 ✗	1 ✗	1
1	1	1	1	1	1 ✔	0 ✗	1

As per statically point of view the product term $a_{m,n}$ has a probability of 1⁄4 of being 1.as shown in the above figure the columns containing more than three partial products, the partial products $a_{m,n}$ and $a_{n,m}$ are combined to form *propagate* and *generate* signals.Thepp's$a_{m,n}$ and $a_{n,m}$ are replaced by altered pp's$p_{m,n}$ and $g_{m,n}$.

We are getting thevalues $p_{m,n}$and $g_{m,n}$

$$^{p}m,n=^{a}m,n+^{a}n,m$$

$$^{g}m,n=^{a}m,n\cdot^{a}n,m.$$

From the facts The risk of the altered partial product gm,n being one is 1/16. The probability of altered partial product pm,n being one is 1/16 + 3/16 + 3/16 = 7/16.by questioning about all these readings we are doing approximation.

A. Approximation of Altered Partial Products $g_{m,n}$

. As each issue includes a chance of 1/16 of being one, 2 parts being one within the equal column even decreases. for instance, in a very column with4 generate signals, chance of all numbers being zero is (1 − pr)4, only 1 part being one is 4pr(1 − pr)3, the chance of 2 factors being one within the column is 6pr2(1 − pr)2, 3 ones is 4pr3(1−pr) and chance of all parts being one is pr4, wherever pr is 1/16. The probability records for a quantity of generate elements in every column are given in Table. From the desk we can say that we can accumulate the column wise generate factors in the altered partial product matrix via the use of or gate to get precise end result in most of the cases. But As the wide variety of generate signals increases, the error chance will increase linearly. So we have to group maximum four elements to the or gate. For a column having m generate signals, m/4 OR gates are used.

B. Approximation of Other Partial Products

We are approximating other partial products by using arithmetic circuits such as approximate adder,multipliers and compressors. *Carry* and *Sum* are two outputs of these approximate circuits. Since *Carry* has higher weight of binary bit, error in *Carry* bit will contribute more by producing error difference of two in the output.The approximation is done in such way that the absolute difference between actual output and approximate output is always maintained as one.here we are using one or gate to accumulate sum why because the x-or gate consume more power and it takes more delay also.So there is a error in the sum calculation A tick mark in the table two denotes that approximate output fits with right output and cross mark denotes mismatch

$$Sum = x1 + x2$$

$$Carry = x1 \cdot x2. \qquad (2)$$

In the approximation of full adder we are using one or gate in the place of x-or gate when we calculate the sum term.Resultserror occurs in cases out of eight cases. This provides more simplification, while maintaining the difference between original and approximate value as one.

$$W = (x1 + x2)$$

$$Sum = W \oplus x3$$

$$Carry = W \cdot x3. \quad (3)$$

As mentioned in reference paper [5] the two 4-2 compressors produce non zero output even for the cases where all impute are zeros.This drawback is overcome by approximated 4-2 compressors. In approximated mechanical device 3 bits ar needed for the output only if all the four inputs arone, that happens one time out of sixteen cases. This property is taken to eliminate one in every of the 3 output bits in 4-2 compressor. To maintain minimal error difference as one, the output "100" (the value of 4) for four inputs being one has to be replaced with outputs "11" (the value of 3). For *Sum* computation, one out of three XOR gates is replaced with OR gate. Also, to make the *Sum* corresponding to the case where all inputs are ones as one, an additional circuit $x1 \cdot x2 \cdot x3 \cdot x4$ is added to the *Sum* expression. This results in error in five out of 16 cases. *Carry* is simplified as in (4).

$$W1 = x1 \cdot x2$$

$$W2 = x3 \cdot x4$$

$$Sum = (x1 \oplus x2) + (x3 \oplus x4) + W1 \cdot W2$$

$$Carry = W1 + W2.$$

Table 4Table 5

TRUTH TABLE OF APPROXIMATE 4-2 COMP RES S OR

Inputs				Approximate outputs		Absolute Difference
$x1$	$x2$	$x3$	$x4$	$Carry$	Sum	
0	0	0	0	0 ✔	0 ✔	0
0	0	0	1	0 ✔	1 ✔	0
0	0	1	0	0 ✔	1 ✔	0
0	0	1	1	1 ✔	0 ✔	0
0	1	0	0	0 ✔	1 ✔	0
0	1	0	1	0 ✗	1 ✗	1
0	1	1	0	0 ✗	1 ✗	1
0	1	1	1	1 ✔	1 ✔	0
1	0	0	0	0 ✔	1 ✔	0
1	0	0	1	0 ✗	1 ✗	1
1	0	1	0	0 ✗	1 ✗	1
1	0	1	1	1 ✔	1 ✔	0
1	1	0	0	1 ✔	0 ✔	0
1	1	0	1	1 ✔	1 ✔	0
1	1	1	0	1 ✔	1 ✔	0
1	1	1	1	1 ✗	1 ✗	1

SYNTHES IS RES ULTS OF EXACT, EXIS TING, AND PROP OS ED APPROXIMATE MULTIP LIERS

Multiplier Type	Area (μm^2)	Delay (ns)	Power (μW)	PDP (fJ)	APP ($\mu m^2 \cdot \mu W)(10^5)$
Exact	4859.28	0.68	1776.49	1208.01	86.32
Multiplier1	2158.56	0.47	503.15	236.48	10.86
Multiplier2	3319.20	0.66	1102.03	727.34	36.57
ACM1 [5]	2871.72	0.4	435.31	174.12	12.50
ACM2 [5]	3782.16	0.63	1250.70	787.94	47.30
SSM [6]	3953.88	0.69	1225.29	845.45	48.44
PPP [7]	4547.52	0.64	1570.79	1005.31	71.43
UDM [8]	3938.00	0.67	1318.51	883.40	51.92

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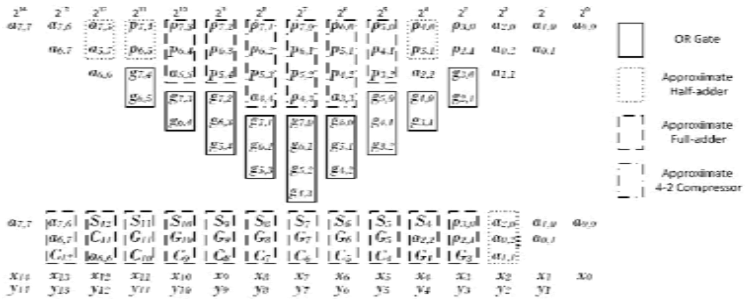
Table6 Error Metrics for 16-bit Multiplier, Fig3 Reduction of altered partial products



Multiplier	Mean Relative Error	Normalized Error Distance
Multiplier1	7.63×10^{-2}	1.78×10^{-2}
Multiplier2	2.44×10^{-4}	7.10×10^{-6}
ACM1 [7]	16.6	4.96×10^{-2}
ACM2 [7]	2.30×10^{-3}	6.36×10^{-6}
SSM [8]	6.34×10^{-4}	1.07×10^{-1}
PPP [9]	8.98×10^{-4}	4.58×10^{-5}
UDM [10]	3.32×10^{-2}	1.39×10^{-2}

The above figure indicates the reduction of altered partial product matrix of 8*8approximate multiplier. for the reduction of generate indicators we need two stages to produce sum and Carry outputs for vector merge addition step.fot we want 4 2 enter or gates, four three enter or gates, and one four input or gates .for the reduction of different partial products we need 3 approximate half adders,3-approximatefull sdders,3-approximate compressors in the first stage. The factors in the second stage are decreased the usage of 1 approximate half-adder and eleven approximate full-adders producing final two operands xi and yi to be fed to ripple carry adder for the final computation of the result.

C. Two Variants of Multipliers

In this in brief 2 multipliers are suggested. in multiplier-1 all n-columns are approximated in n*n multiplier where as in multiplier-2 $n-1$ least significant columns are approximated using proper approximatedcircuits

III.RESULTS AND DISCUSSIONS

For result analysis all multipliers are for n=16. The multi-pliers area unit enforced in Verilog and synthesized victimization Synopsys style Compiler and a TSMC sixty five nm galvanic cell library at the standard method corner, with temperature twenty five °C and provide voltage one V. From the Synopsys dc reports, we tend to get space, delay, dynamic power and leakage power.In proposed method approximation is applied for all columns,where as in Multiplier2, approximation is applied in 15 least significant columns during partial product reduction. For altered partial products arithmetic circuits such as approximate adder, 4-2 compressor is used to form final two rowsof partial products.The efficiency of proposed multiplier is compared with all existing approximate multipliers with respective MRE and ED.the results are presented in table6.

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Table7

RANKING OF APPROXIMATE MULTIPLIERS IN TERMSOF DES IGN AND ERROR METRICS

Approximate Multiplier Type	APP Gain	PDP Gain	NED	MRE
Multiplier1	1	2	6	6
Multiplier2	3	3	2	1
ACM1 [5]	2	1	7	7
ACM2 [5]	4	4	1	4
SSM [6]	5	5	4	2
PPP [7]	7	7	3	3
UDM [8]	6	6	5	5

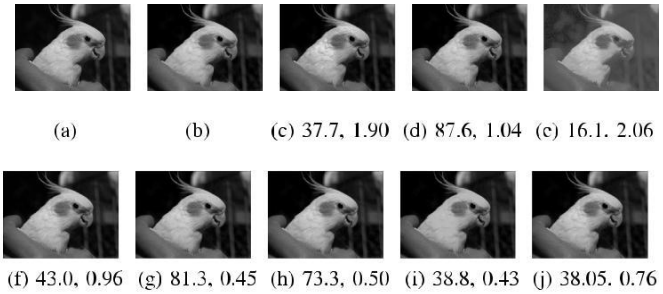

Fig. 4.(a) Input image-1 with Gaussian noise. Geometric mean filtered images and corresponding PSNR and energy savings in μJ using (b) exact multiplier, (c) Multiplier1, (d) Multiplier2, (e) ACM1, (f) ACM2, (g) SSM,(h) PPP, (i) UDM, and (j) VOS.

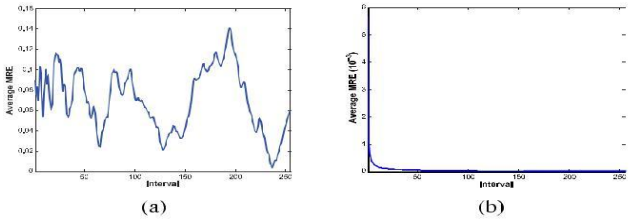

Fig6:-MRE distribution of (a) Multiplier1 and (b) Multiplier2

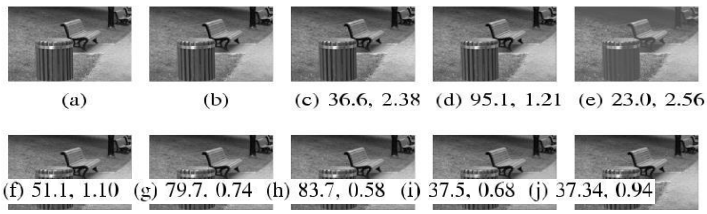

Fig. 5. (a) Input image-2 with Gaussian noise. Geometric mean filtered images and corresponding PSNR and energy savings in μJ using (b) exact multiplier, (c) Multiplier1, (d) Multiplier2, (e) ACM1, (f) ACM2, (g) SSM, (h) PPP, (i) UDM, and (j) VOS.

IV. APPLICATION—IMAGE PROCESSING

Geometric mean filter is broadly used in image processing to reduce Gaussian noise [13]. The geometric mean filter is higher at maintaining part facets than the arithmetic mean filter..three × 3 suggest filter is used, the place every pixel of noisy photograph is changed with geometric imply of three × 3 block of neighboring pixels established on it..these exact and approximate multipliers are used to generate pixals of image.when we want high clarity image we are using exact multiplier where as for low clarity using approximate multipliersame trick only we are using in several multimedia applications. to examine the excellent of approximate multipliers we the use of PSNR as figure of merit. Actually imply rectangular error decides the PSNR which is nothing but the distinction of the ensuing photograph generated by using actual multiplier and the image generated by using proposed multiplier logic.

We are calculating the energy taken by these two multipliers while they are generating the image by using synopsisprimetime. Further we are scaling down the exact multiplier voltage from 1v to 0.8v and checking the power consumption and generated image quality. The analysis what we have done on exact multiplier and approximate multiplier when we apply noisy input image and denoisy input image with respect to power consumption and PSNR are listed in the table. The energy required to generate fig1 and fig2 by exact multiplication process is given by 3.24 and 2.62 μJ , respectively. We can conclude ACM1 has better electricity saving when compared to multiplier1.multiplier has better PSNR than ACM1.multiplier2 has fantastic PSNR among all approximate multipliers. When compared to ACM2, PPP, SSM, UDM, and VOS multiplier2 has nice strength saving.

V.CONCLUSION

In brief,we have taken existed multiplier. We have replaced partial products with new generate and propagate signals. We have approximated x-or gate with or gate so that we can reduce the delay on the critical path. We have also approximated all generate signals depending on their places and error statistics. We also used approximated half adder, full adder and approximated 4:2compressor. Over all we have proposed two multipliers. In multiplier1 we have approximated all n- columns and in multiplier2 we have Approximated n-1 columns. At last we compared proposed multipliers with existed approximated multipliers in terms of power and delay.multiplier1 and multiplier2 has saved APP 87% and 58% respectively when compared to existed approximated multipliers.Proposedmultipliers have betterprecision, areaand power reading when compared to existed multipliers. Proposed multipliers can use in error resilient application where we need low area, less power and better quality.

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