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A Novel Approach for Signal Integrating and Standby Power Reduction by CMOS RFF

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ABSTRACT

In this paper, we propose a level-converting retention flip-flop (RFF) for ZigBee systems-on- chips (SoCs). The proposed RFF allows the voltage regulator that generates the core supply voltage ($V_{DD,core}$) to be turned off in the standby mode, and it thus reduces the standby power of the ZigBee SoCs. The logic states are retained in a slave latchcomposedof thick-oxide transistors using an I/O supply voltage ($V_{DD,IO}$) that is always turned on. Level-up conversion from $V_{DD,core}$to $V_{DD,IO}$ is achieved by an embedded nMOS pass-transistor level- conversion scheme that uses a low-only signal-transmitting technique. By embedding a retention latch and level-up converter into the data-to-output path of the proposed RFF, the RFF resolves the problems of the static RAM-based RFF, such as large dc current and low readability caused by threshold drop. The proposed RFF does not also require additional control signals for power mode transitioning. Using 0.13-μm process technology, we implemented an RFF with $V_{DD,core}$and $V_{DD,IO}$ of 1.2 and 2.5 V, respectively. The maximum operating frequency is 300 MHz. The active energy of the RFF is 191.70 fJ, and its standby poweris350.25 pW.

Keywords*— *I/O supply voltage, retention flip-flop (RFF), standby leakage current, standby mode, thick-oxide transistor.

I. INTRODUCTION

In Recent years, wireless sensor networks (WSNs) have been evolving at an accelerated pace. To buildWSNs,the ZigBee protocol, in which medium access control and the physical layer are defined by IEEE 802.15.4, has been generally used [1]. Because the ZigBee protocol has low data rate and power specifications, its use can prolong battery life. This feature makes the ZigBee protocol preferred over other technologies such as 802.11.× and Bluetooth [2]. In addition, most ZigBee systems-on-chips (SoCs) support a number of power modes including a standby mode that occupies the system 99.9% of the time to maximize the battery life [3]–[5]. Thus, standby power reduction is extremely importantforminimizing the power consumption of ZigBee SoCs—standby power consumption becomes more critical as the process technology scales down because the leakage current increases exponentially with the scaling threshold voltage (V_t) and the gate oxidethickness.

To ensure that ZigBee SoCs can operate properly after returning to the active mode, the logic states containing

hardware calibration, hardware configuration, and network routing information should be preserved before entering the standby mode [6]. Data preservation is also required to achieve a smooth power mode transition between the standby mode and the active mode. Thus, retention flip-flops (RFFs) are used in many ZigBee SoCs for storing the logic states, and several types of RFFs have been widely researched [7]–[12].

The balloon-circuit RFF proposed in [7] stores data in an additional retention latch called a balloon circuit; however, this structure is not suitable for battery-operated mobile applica- tions because a balloon circuit increases the circuit area and standby leakage current. The static RAM (SRAM)-based RFF proposed in [8] uses a simple architecture to reduce the area overhead and standby leakage current; however, this structure should perform the readoperation during the mode transition from standby mode to active mode because the retention latch is not on the data-to-output path, which possibly incurs incorrect outputs owing to the thresholddrop.

In this paper, we propose a level-converting RFF. In the standby mode, logic states are preserved in a slave latch composed of thick-oxide transistors utilizing an I/O supply voltage ($V_{DD,IO}$) that is always turned on. To use both the core supply voltage ($V_{DD,core}$) and $V_{DD,IO}$ domains with- out incurring problems due to the threshold drop, as in an SRAM-based RFF, an nMOS pass-transistor level-conversion scheme is embedded into the data-to-output path. Because the power management scheme using the proposed RFF enables the voltage regulator generating $V_{DD,core}$to be turned off in the standby mode, the standby power consumption can be significantly reduced. The proposed RFF also reduces the area overhead because it does not require an additional retention latch, a level-up converter, control signals for power mode transition, and powerswitches.

The remainder of this paper is organized as follows. The power management schemes to support the standby mode are explained in Section II. The SRAM-based and proposed RFFs are described in Section III. In Section IV, the SRAM-based RFF is compared with the proposed RFF, and the experimental results are presented in Section V. Finally, we conclude with a summary in Section VI.

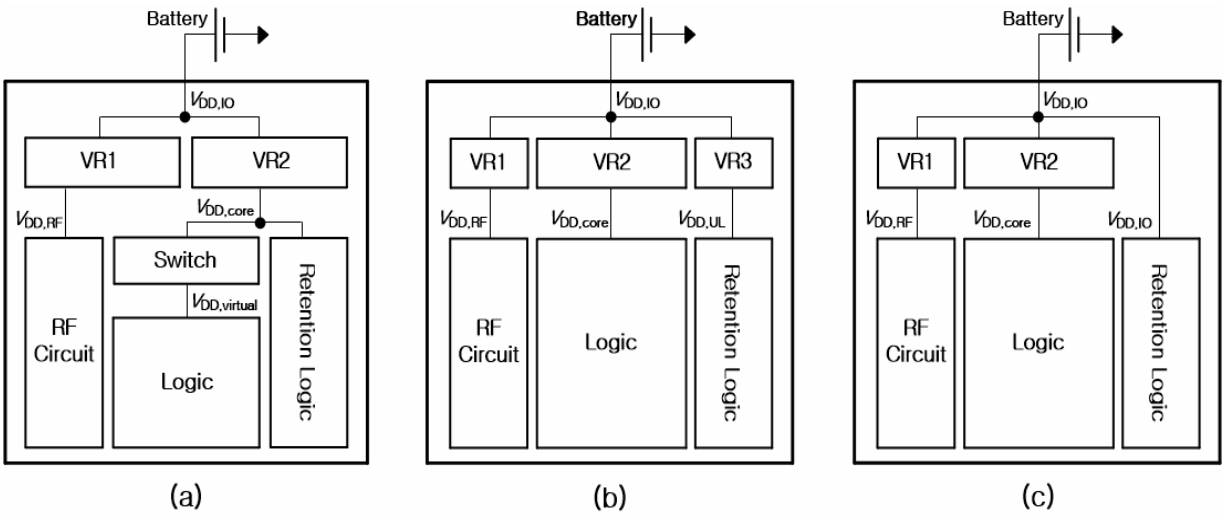

Fig.1.Retention architecture with (a) MTCMOS scheme, (b) ultralow supply voltage ($V_{DD,UL}$), and (c) I/O supply voltage($V_{DD,IO}$).

II. RETENTION ARCHITECTURE IN ZIGBEESOCS

A. Retention Logic withthe Multithreshold-Voltage MOSScheme

A power-gating scheme using multithreshold-voltage CMOS (MTCMOS) represents one solution for reducing the standby power [13], and many conventional RFFs adopt the MTCMOS scheme shown in Fig. 1(a). Retention logic sup- plied by $V_{DD,core}$preserves the logic states in the standby mode, whereas the computation logic supplied by the vir- tual supply voltage ($V_{DD,virtual}$) is power-gated to reduce the standby power [7]–[12]. However, the power reduction is limited because the voltage regulator generating $V_{DD,core}$(VR2) must remain on during the standby mode to supply the retention logic. Another flaw of the power- gating scheme using MTCMOS is the area inefficiency due to the requirement of large head/footswitches.

B. Retention Logic WithUltralow SupplyVoltage

The usage of an ultralow supply voltage for data retention allows for the minimization of the leakage power during the standby mode [14]. Thus, the power management scheme with the ultralow-supply voltage retention logic shown in Fig. 1(b) is another solution for reducing the standby power. Because all the transistors in the retention logic operate in weak inversion with a low drain-to-source voltage, the subthreshold leakage current isexponentiallyreduced. Compared with the scheme in Fig. 1(a), an additional voltage regulator (VR3) generating an aggressively scaled supply voltage is employed only for the retention logic at the cost of area overhead and active power. This power management scheme also has the same disadvantage as the power management scheme in Fig. 1(a) in that the voltage regulator for the retention logic (VR3) must be turned on during the standby mode. Thus, a power management scheme to turn off the voltage regulator in the standby mode is required [15].

C. Retention Logic WithI/O SupplyVoltage

The power management scheme for turning off the voltage regulator in the standby mode is shown in Fig. 1(c). In this architecture, the voltage regulator for the retention logic is not required, and the retention logic is directly supplied from $V_{DD,IO}$. The standby power of the retention logic itself is actually a little large owing to the use of $V_{DD,IO}$ that is larger than $V_{DD,core}$. However, compared with the power consume- tion of the voltage regulator for retention logic, the increase in the standby power caused by $V_{DD,IO}$ is insignificant. The current flowing through the turned-on voltage regulator is a few microamperes [16]. This current is much larger than that flowing through the several hundred bits of the retention logic required in ZigBee SoCs [17].

To use this power management scheme, level conversion between the $V_{DD,core}$and $V_{DD,IO}$ domains should be supported; otherwise, the power management scheme cannot be applied owing to the dc current path created by the level difference between $V_{DD,core}$and $V_{DD,IO}$. The proposed RFF achieves level-up conversion from $V_{DD,core}$ to $V_{DD,IO}$ by an embed- dednMOS pass-transistor level-conversion scheme using a low-only signal-transmittingtechnique.

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III. RETENTIONFLIP-FLOPS

A. SRAM-BasedRFF

Fig. 2 shows an SRAM-based RFF [8]. The master latch is based on a cross-coupled-inverter latch, which is generally used in a typical CMOS static D flip-flop (DFF), whereas the slave latch consists of a transmission gate (TG1), inverters (INV2 and INV5), and a 6T SRAM cell. All gates on the data-to-output path are composed of thin-oxide transistors to avoid performance degradation, and the 6T SRAM cell uses thick-oxide transistors to reduce the standby leakage current. As the SRAM-based RFF adopts the MTCMOSscheme,

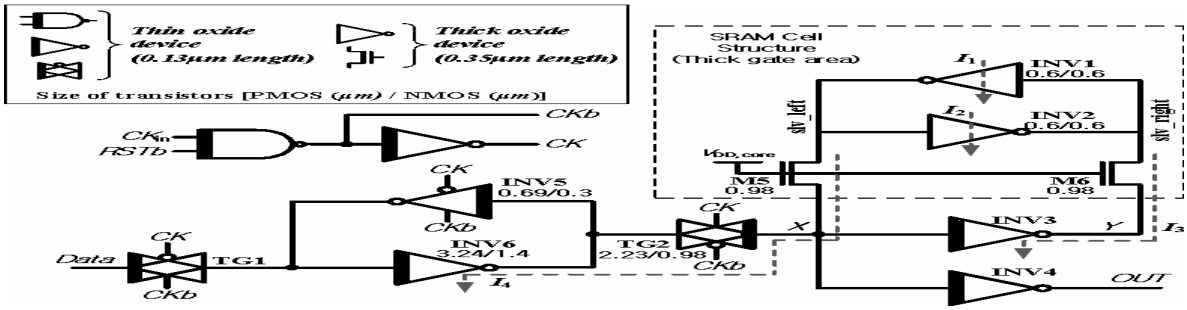

Fig.2. Structure of the SRAM-basedRFF.

the thin-oxide transistors and access transistors (M5 and M6) are originally supplied by $V_{DD,virtual}$, whereas the retention latch (INV3 and INV4) is originally supplied by $V_{DD,core}$. However, to use the power management scheme for turning off the voltage regulator in the standby mode, $V_{DD,virtual}$and $V_{DD,core}$used for the transistors are changed to $V_{DD,core}$and $V_{DD,IO}$, respectively, as shown in Fig. 2. Then, the voltage regulator generating $V_{DD,core}$can be turned off, and the retention latch powered by $V_{DD,IO}$ retains the logic state in the standbymode.

The SRAM-based RFF uses access transistors to convert the voltage level. In the active mode, access transistors are turned on and perform write/read access. During write access, the access transistors provide differential write-access, enabling a conversion in the voltage level from $V_{DD,core}$to $V_{DD,IO}$ when the clock is asserted high. The logic states at *X* and *Y* are the low and high $V_{DD,core}$levels, respectively, or vice versa. A low state is completely transferred to the retention latch through M5 (or M6), after which INV4 (or INV3) generates a high $V_{DD,IO}$ level through M2 (or M1). A high $V_{DD,core}$is transferred as ($V_{DD,core}$–V_{t_thick}) ($V_{t_thick}$is V_t of the thick- oxide transistor) to the retention latch through M6 (or M5), after which the access transistor that transferred the high $V_{DD,core}$is turned off, avoiding the creation of a dc current path. During read access, the access transistors supply the correct state to the $V_{DD,core}$domain. In the standby mode, $V_{DD,core}$is turned off, and the clock is asserted low before the access transistors are turned off; as a result, the retention latch supplied by $V_{DD,IO}$ is isolated by the access transistors and isable to hold data.

The SRAM-based RFF effectively reduces the area overhead in comparison with the balloon-circuit RFF proposed in [7] by eliminating additional control codes for power mode transition and embedding the retention latch into the slave latch. The standby power is also reduced, as the leakage paths in the standby mode (I_1, I_2 ,

I_3 , and I_4) include the thick-oxide transistors M1–M6. However, several problems can occur because the retention latch is not on the data-to-output path. After write access for the high $V_{DD,core}$level is performed through M5 when CK is asserted high, M5 is turned off, and node *X* is left floating temporarily as CKbecomeslow. Node *X* is vulnerable to glitch-creating noise such as cross-talk because it is floating until the value of node *X* drops to ($V_{DD,core}$–V_{t_thick}). During the transition from the standby mode to the active mode, data in the retention latch need to be transferred to nodes *X* and *Y* ; however, if the node value of slv_left is high, *X* becomes ($V_{DD,core}$–V_{t_thick}) owing to the threshold drop, and a dc current will flow through the p and nMOS in INV2.

B. Proposed Level-ConvertingRFF

The proposed level-converting RFF is shown in Fig. 3. The master latch is also based on a cross-coupled-inverter latch as the DFF, and an additional data transmission path (M3 and M1) is embedded. Both thin- and thick-oxide transistors are used, and the core logic and retention logic are supplied by $V_{DD,core}$and $V_{DD,IO}$, respectively. Level-up conversion from the $V_{DD,core}$domain in the master latch to the $V_{DD,IO}$ domain in the slave latch is achieved through an nMOS pass-transistor level-conversion scheme similar to that developed in [18].

The proposed RFF operates as follows (Fig. 4). When nodes *X* and *Y* (or *Y* and *X*) in the master latcharehigh and low, respectively, an access transistor M4 (or M3) is turned on, and another access transistor M3 (orM4)isturned off. Then, the ON-state access transistor M4 (M3) forms a transmission path between the masterlatchand the slave latch, and node *Y (X)* becomes an input of the transmission path. In other words, onlythetransmission path from the master latch to the slave latch is determined on the basis of the state of data inthe masterlatch, and the voltage level can be converted in the slave latch without generating a dc-current path because onlyalow signal is transmitted at all times. Thus, the $V_{DD,core}$domain is converted into the $V_{DD,IO}$ domainwithoutthe need for an additional level-up converter. Level-down conversion from $V_{DD,IO}$to $V_{DD,core}$occurs at INV3and INV4, which are composed of thick-oxide transistors but supplied by $V_{DD,core}$. In the standby mode, when RSTb is asserted low, CK become slow, and $V_{DD\ ,core}$ is collapsed by turning off the voltage regulator; in thiscase, the slave latch is isolated by turning off the access transistors (M1 and M2) and operates as a retention latchtoholdlogic states by $V_{DD,IO}$ that is always turned on. It is important to note that the sizes of thetransistorson the data-to-output path need to be determined carefully. There are two considerations, standby power and write- ability. As the standby power is consumed by only a slave latch, INV1 and INV2 should be sized to minimize the subthreshold leakage current that is generally proportional to the width of the transistor. However, in deep sub micrometer process technology, V_t sharply decreases with a decrease in the channel width, and this is called the inverse narrow width effect (INWE). This effect results in an exponential increase in the leakage current, making the INWE increasingly important with technology scaling [19]. The sizes of the transistors of the slave latch that minimize the subthreshold leakage current are determined by the simulation results shown in Fig. 5. The second consideration is write-ability.

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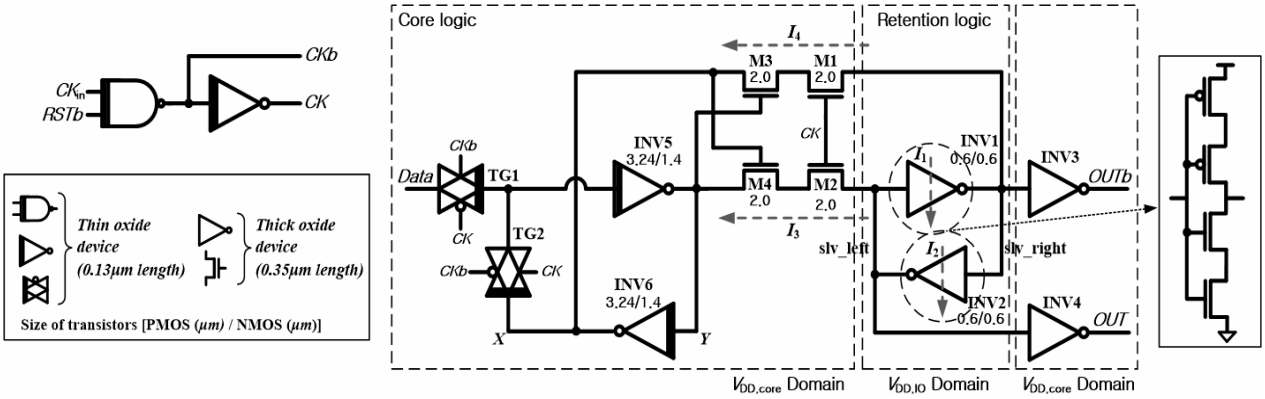

Fig.3. Structure of the proposedRFF.

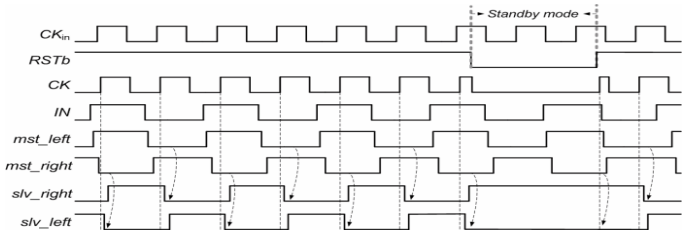

Fig.4. Timing diagram of the proposedRFF.

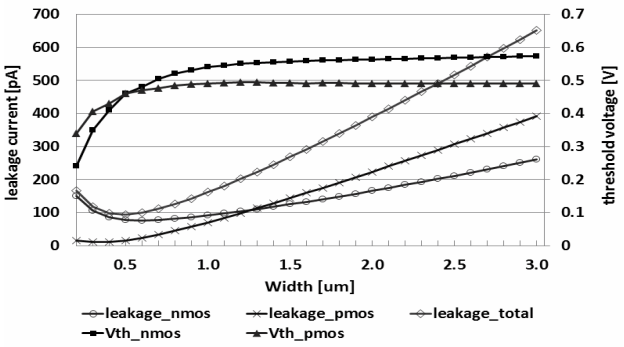

Fig. 5.Plot of the threshold voltage versus width, demonstrating the INWE.

The write operation is performed by pulling down slv_left or slv_right in Fig. 3 because the master latch always transmits a low signal to the slave latch in the proposed RFF. The pull-down network of slv_right (slv_left) consists of M1 and M3 (M2 and M4) and the nMOS in INV6 (INV5). However, the pull-up network of slv_right (slv_left) composed of two-stacked pMOS transistors in INV2 (INV1) is simulta- neously turned on if the data to be transferred is different than the retained data. Thus, the pull-down network (three-stacked nMOS transistors) should be much stronger than the pull-up network (two-stacked pMOS transistors in INV1 or INV2). The pull-down network is designed to be 10 times stronger than the pull-up network in the proposed RFF. To check the write operation, 1 000 000 Monte Carlo simulations were performed with a high $V_{DD,IO}$ of 2.7 V at a high temperature of 85 °C to consider the worst condition. The results show no failures and thus,

reliable write operation isverified.

The proposed RFF does not require an additional retention latch nor does it require the write/read operations necessary in SRAM-based RFFs. As all standby leakage paths (I_1 , I_2 , I_3 , and I_4) in the proposed RFF consist of thick-oxide transistors, the standby leakage current will be less than that of an SRAM-based RFF. Further reduction in the standby leakage in paths I_3 and I_4 can be achieved by arranging the access transistors (M1 and M3, and M2 and M4) in a stacked structure, and the inverters (INV1 and INV2) in the slave latch are designed using stacked p/nMOS transistors, allowing the standby leakage of I_1 and I_2 to also be reduced. Because the retention latch in the proposed RFF is located on the data-to- output path, and level-up conversion from the $V_{DD,core}$domain to the $V_{DD,IO}$ domain is achieved through an nMOS pass- transistor level-conversion scheme, the problems of threshold drop in the SRAM-based RFF are resolved with only a degradation in speed. However, the speed degradation is not a problem in this target application because the digital logic in ZigBee SoCs operates at a low frequency ofapproximately20 MHz [20]. Thus, the proposed RFF can be appropriately applied to the ZigBee SoCs and also implemented using deep submicrometer process technology.

IV. EXPERIMENTALRESULT

The test chip fabricated using 0.13-μm bulk-CMOS process technology contains a shift register composed of 1000 pro- posed RFFs. A micrograph of the test chip is shown in Fig. 11. The active area of the shift register is0.127 mm^2. Fig. 12 shows the measured active energy per RFF in terms of $V_{DD,core}$. When measuring the active energy, the switching factor was set to 1, and $V_{DD,IO}$ was set to 2.5 V, whereas the clock frequency was set to 20 MHz.However, the leakage current cannot be measured because the measured leakage current is dominated by the leakage current of the peripherals in the fabricated testchip.

It compares the overall performance of the proposed RFF with the conventional structures. Balloon and SBRFF are the balloon-circuit RFF [7] and SRAM-based RFF [8], respectively. The CCRFF reported in [10] uses cross-coupled inverters for data retention with no extra data-preserving latch required. The MRFF reported in [11] is a memory RFF. Data- preserving memory elements are integrated into the MTCMOS flip-flop. The ARFF reported in [12] is the autonomous RFF that also does not require an additional control signal for the mode transition, as in the proposed RFF. Although the SBRFF structure exhibits the lowest leakage current per RFF, the conventional structures [7]–[12] including the SBRFF adopt the MTCMOS power management scheme, and thus the power of the voltage regulator should be considered in

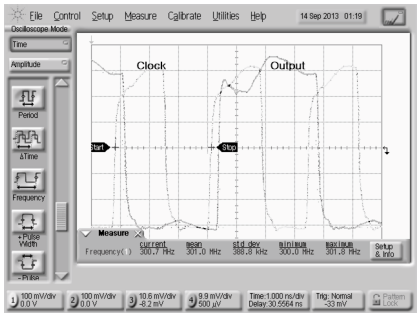

Fig.6.Measured waveform illustrating that the proposed RFF operatesat300 MHz.

the standby power. Compared with the MTCMOS power management scheme using the SBRFFs in [8] and the voltage regulator in [16], the I/O supply voltage power management scheme using the proposed RFFs is beneficial when the number of required RFFs is less than 9000 because the power overhead of the voltage regulator is substantial. Because the required number of RFFs used in commercial ZigBee SoCs is about 1000, it is preferable from an architectural point of view to employ a power management scheme to turn off the voltage regulator in the standby mode, as shown in row 6 of Table I. In the comparison of the standby leakage of the retention logic, the quiescent current of the voltage regulator in [16] and the leakage current of the 1000 RFFs are considered; the quiescent current of the voltage regulator in [16] is 0.9 μA at the minimum load, which is a very low value amongst state-of-the-art voltage regulators. The cell-area comparison is superseded by the comparison of the number of transistors in a cell because the compared RFFs are fabricated using different process technologies. The proposedRFFconsists of 24 transistors, similar to the conventional RFFs. However, the conventional RFFs require additional transistors for power-gating. The RSBRFF is the revised SRAM-based RFF using the $V_{DD,IO}$for data retention, as shown in Fig. 2. When compared with the RSBRFF, the leakage current of the proposed RFF is reduced by 63% at the cost of active energy and speed. The maximum operating frequency of the proposed structure is 300 MHz, as shown in Fig. 6, which is sufficient to satisfy the operating frequency requirements of the target application—the ZigBee[22,23]SoCs.

V. CONCLUSION

An RFF that retains data using $V_{DD,IO}$ and performs level conversion using an embedded nMOS pass-transistor level-conversion scheme employing a low-only signal- trans- mitting technique was proposed in this paper. The proposed RFF achieves ultralow-standby power by adopting a power management scheme to use $V_{DD,IO}$ for data retention and to turn off the voltage regulator in the standby mode. The embedded level conversion scheme eliminates the need for an additional level-up converter in the proposed RFF. In addition, the retention latch in the proposed RFF is composed of a stacked structure with thick-oxide transistors toreducethe standby leakage current. As validated in the simulations and experiments, the proposed RFF is highly suitable for deployment in low-activity sensor networks using the ZigBee[23]protocol.

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