3-BIT ENCODER FOR FLASH ADC

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ABSTRACT

High speed devices play an important role in many applications, for example disk drives, wireless communications, and ultra wide band receivers. For all high speed ADCs, regardless of the architecture, one of the critical performance limiting building blocks is the encoder, which determines the overall performance of data converters, including the maximum sampling rate, bit resolution, and total power consumption. Encoder circuit is made using static logic gates and domino logic gates. Static gates are power efficient because static gates have no static power dissipation but have larger delay than the dynamic gates. To enhance the speed, dynamic gates become the best suitable option. Another dynamic approach is carried out using single stage domino circuit. This technique requires least number of transistors and gives the required delay. The third approach is used through NORA logic, which is fully dynamic logic. In the NORA logic gates, binary codes are generated in a single clock period. Although the NORA architecture requires larger number of transistors as compare to first approach but the speed is enhanced.

Keywords: Description of ADC, Encoder for flash ADC

1. INTRODUCTION

In the past decades, the advancements in the field of VLSI manufacturing technology has driven the IC design trend eventually towards, the integration of the digital and analog functional blocks into a single chip. To incorporate these two quantitatively contradictory types of signals, an interface serving as a bridge between analog and digital signals, for instance, an analog to digital converter (ADC), is inevitably required. For different applications, various types of analog to digital converters targeted on specific purpose have been proposed. For example sigma delta ADC aims at a high resolution products; flash ADC is for high speed while pipeline ADC is for medium resolution and medium speed applications. Flash ADCs are designed for the lowest possible power consumption. Pipelined ADCs serve a wide range of applications because of flexible resolution bits and sampling rate. In general, pipelined ADCs have proven to be very efficient architectures for meeting the low-power dissipation and high-input-bandwidth requirements. Pipelined ADCs operate at high sampling rates with high dynamic performance. Successive approximation ADCs are used for low-power, medium-quality applications like data acquisition. Sigma-Delta ADCs are most used for high-resolution and low-sampling-rate audio applications like Minidisk, AV receivers, and musical instruments that require high linearity and wide dynamic range.

II. DESCRIPTION OF ADC

One of the most important functions in signal processing is the conversion between analog and digital signals. As more products perform calculation in digital or discrete time domain, more sophisticated data converters must translate the digital data to and from our inherent analog world. Consequently it is necessary to be able to convert back and forth between the two types of signals. Therefore, analog to digital and digital to analog conversions are important part of any signal processing system.

III. ARCHITECTURE OF FLASH ADC

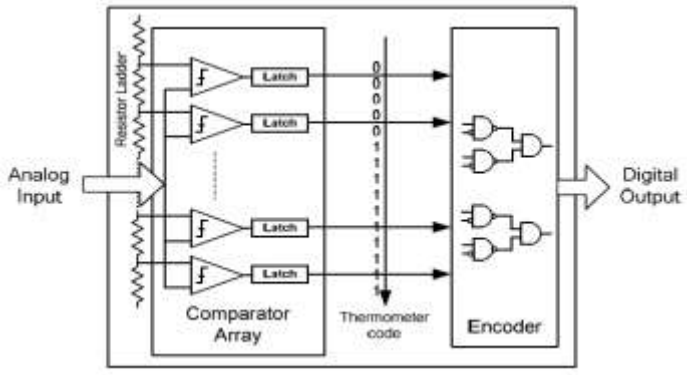

Fig.1: Architecture of Flash ADC

A generic architecture for a flash ADC is shown in Figure 2. The input signal of the ADC is compared against evenly-spaced reference voltages generated by a resistor ladder. Comparators, including several amplification-and-latching stages, amplify the differences between the input signal and those reference voltages. They deliver the comparison results as an array of digital bits or a code word to the encoder. This code word is called a thermometer code, due to the thermometer-like appearance of 1's and 0's in it. The encoder converts the thermometer code to a Gray or a binary code. A prefilter is necessary to avoid the aliasing of higher frequency signals back into the baseband signal of ADC. Sample and hold circuit converts the analog signal into discrete signal. This discrete signal is converted into digital signal after quantizing it. The nature of quantizer is to segment the signal levels of discrete signal into fix levels. For N bit of digital output code there are 2^N fixed levels. Finally encoder encodes these levels into digital codes. The codes at the output of the encoder may be in binary form or may be in gray code format depending on the application of the converter. Generally, the intermediate code of the converter is in the thermal code format

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1V.REGION OF OPERATION.

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REGION	CONDITON	p-device	n-device	OUTPUT
A	$0 =< V_{in} < V_{tn}$	Nonsaturated	Cutoff	Vout = VDD
B	$V_{tn} =< V_{in} < V_{DD}/2$	Nonsaturated	Saturated	Eq. 2
C	Vin = VDD/2.	Saturated	Saturated	$V_{out} != f(V_{in})$
D	$V_{DD}/2 < V_{in} =< V_{DD} + V_{tp}$	Saturated	Nonsaturated	Eq. 5
E	$V_{in} >= V_{DD} - V_{tp}$	Cutoff	Nonsaturated	$V_{out} = Vss$

.V. ENCODER CIRCUITS BY DIFFERENT LOGIC

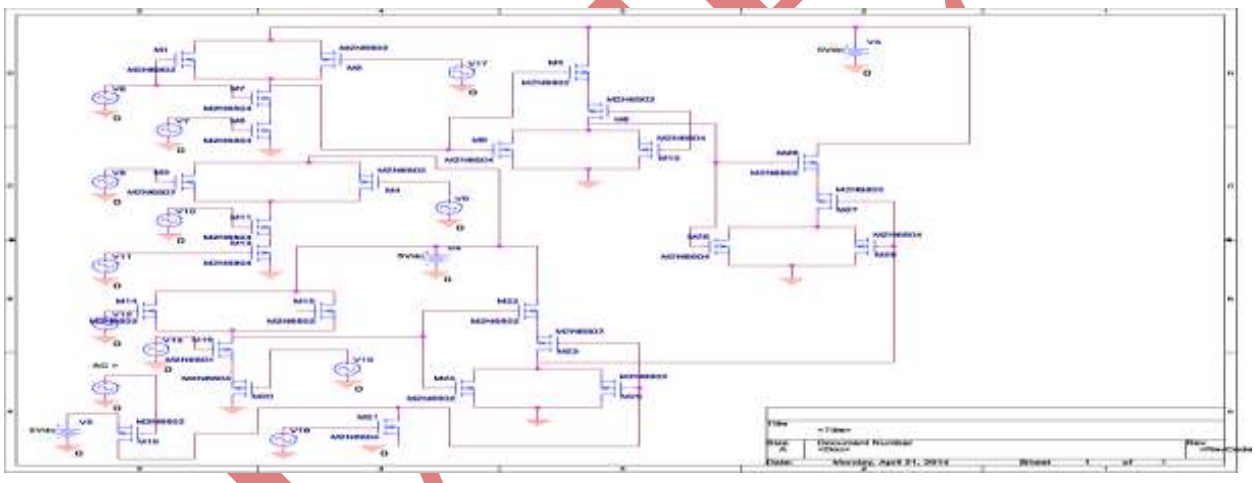

Fig.2: Circuit diagram for bit B0 of encoder

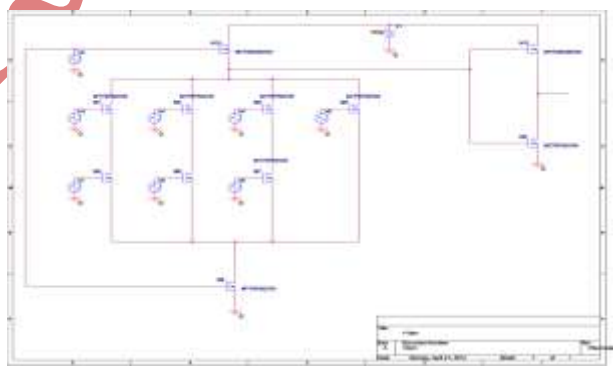

Fig.3: using DOMINO Logic

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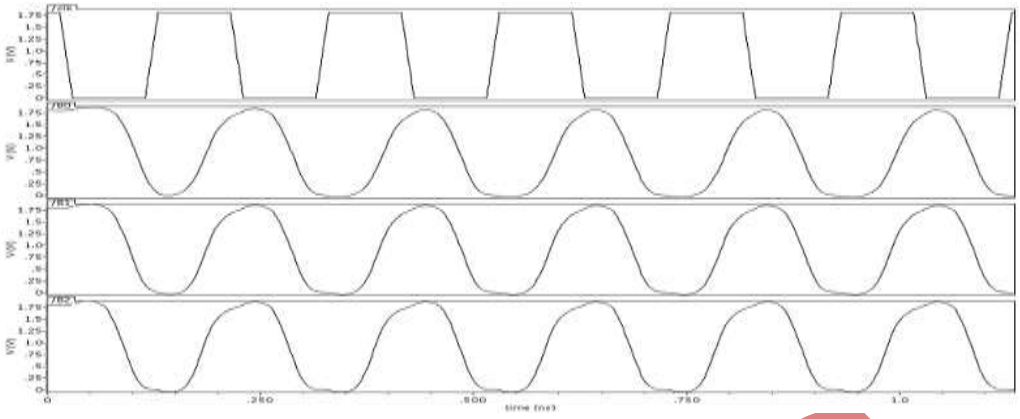

Fig.4:Simulated waveform for DOMINO Encoder

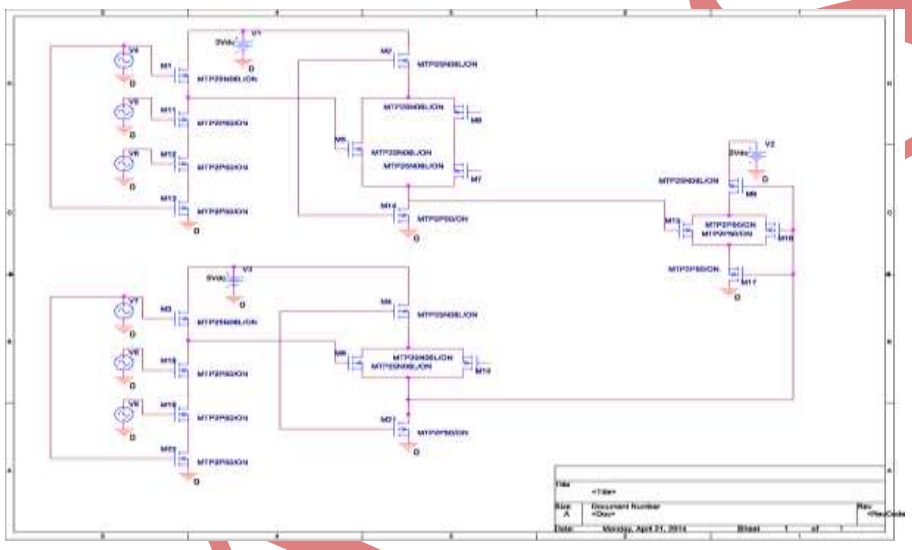

Fig 5: using NORA

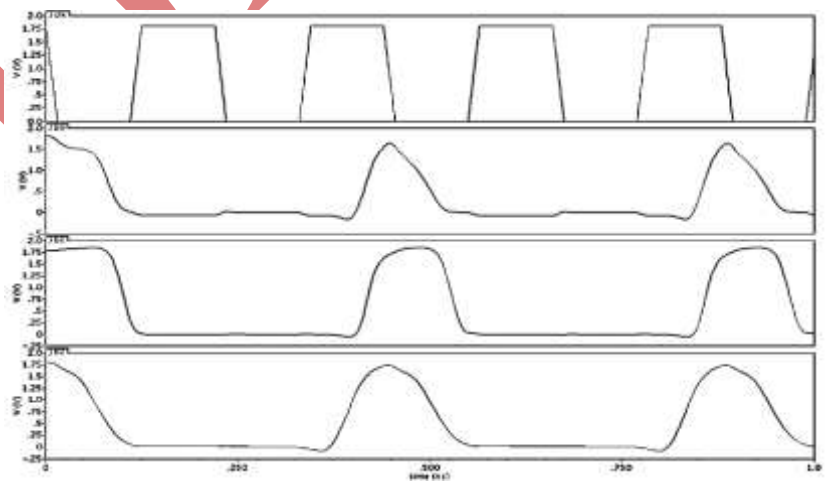

Fig 6: Simulated waveform for NORA Encoder

VI. CONCLUSION

The encoder in a flash ADC is one of the bottlenecks in high speed operation. Furthermore, the encoder should be able to properly handle the speed. Different topologies for 3 bit encoder using 0.18um technology are presented in this work. A digital encoder has been proposed, which operates at a frequency of 1 GHz. Different topologies are analysed and simulated using cadence spectre tool. The output of different topologies are summarised in table 1.

Table 1 Comparison of different topologies

S. No.	Topology	Delay
1	Simple gate	High
2	DOMINO	Low
3	NORA	Moderate

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