# DESIGN AND VERIFICATION OF DDR3 MEMORY CONTROLLER

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## ABSTRACT

DDR3 SDRAM or double-data-rate three synchronous dynamic random access memories is a random access memory interface technology used for high bandwidth storage of the working data of a computer or other digital electronic devices. DDR3 is part of the SDRAM family of technologies and is one of the many DRAM (dynamic random access memory) implementations. DDR3 SDRAM is the 3rd generation of DDR memories, featuring higher performance and lower power consumption. In comparison with earlier generations, DDR1/2 SDRAM, DDR3 SDRAM is a higher density device and achieves higher bandwidth due to the further increase of the clock rate and reduction in power consumption..The architecture of DDR3SDRAM controller consists of Initialization fsm Command fsm, data path , bank control ,clock counter, refresh counter, Address FIFO, command FIFO ,Wdata FIFO and R_data reg In this paper, an advanced DDR3SDRAM controller architecture was designed.Design is made using Verilog and verified using System Verilog OVM.

***Keywords :-*** *SDRAM,DDR3,FSB,DIMM,CAS*

## 1. INTRODUCTION

DDR3 SDRAM or double-data-rate three synchronous dynamic random access memories is a random access memory technology used for high bandwidth storage of the working data of a computer or other digital electronic devices.DDR3 is part of the SDRAM family of technologies and is one of the many DRAM (dynamic random access memory) implementations. The primary benefit of DDR3 is the ability to transfer I/O data at eight times the data rate of the memory cells it contains, thus enabling higher bus rates and higher peak rates than earlier memory technologies. However, there is no corresponding reduction in latency, which is therefore proportionally higher. In addition, the DDR3 standard allows for chip capacities of 512 megabits to 8 gigabits, effectively enabling a maximum memory module size of 16 gigabytes[1][5]. The DDR3 SDRAM is not very much different from the previous generation DDR memory in terms of its design and working principles. In fact, it is true: DDR3 SDRAM is a sort of third reincarnation of DDR SDRAM principles. Therefore, we have every right to compare DDR3 and DDR2 SDRAM side by side here. The frequencies of DDR3 memory could be raised beyond those of DDR2 due to doubling of the data prefetch that was moved from the info storage device to the input/output buffer. While DDR2 SDRAM uses 4-bit samples, DDR3 SDRAM uses 8-bit prefetch also known as 8n-prefetch. In other words, DDR3 SDRAM technology implies doubling of the internal bus width between the actual DRAM core and the input/output buffer[2][4]. As a result, the increase in the efficient data transfer rate provided by DDR3 SDRAM doesn't require faster operation of the memory core. Only external buffers start working faster. As for the core frequency of the memory chips, it appears 8 times lower than that of

the external memory bus and DDR3 buffers (this frequency was 4 times lower than that of the external bus by DDR2) So, DDR3 memory can almost immediately hit higher actual frequencies than DDR2 SDRAM, without any modifications or improvements of the semiconductor manufacturing process. However, the above described technique also has another side to it: unfortunately, it increases not only memory bandwidth, but also memory latencies. As a result, we shouldn't always expect DDR3 SDRAM to work faster than DDR2 SDRAM, even if it operates at higher frequencies than DDR2. DDR3 SDRAM offers a few other useful improvements that will encourage not only the manufacturers but also the end users to make up their minds in favor of the new technology.

### 1.1 DDR3 ADVANTAGES

- Lower power
- Higher speed
- Master reset
- More performance
- Larger densities
- Modules for all applications

## 2.1 TYPES OF MEMORY CONTROLLERS

### 2.1.1 DDR1 SDRAM CONTROLLER

Double Data Rate-SDRAM, or simply DDR1, was designed to replace SDRAM. DDR1 was originally referred to as DDR-SDRAM or simple DDR. When DDR2 was introduced, DDR became referred to as DDR1. Names of components constantly change as newer technologies are introduced, especially when the newer technology is based on a previous e one. The principle applied in DDR is exactly as the name implies "double data rate". The DDR actually doubles the rate data is transferred by using both the rising and falling edges of a typical digital pulse. Earlier memory technology such as SDRAM transferred data after one complete digital pulse. DDR transfers data twice as fast by transferring data on both the rising and falling edges of the digital pulse[1].

### 2.1.2 DDR2 SDRAM CONTROLLER

DDR2 is the next generation of memory developed after DDR. DDR2 increased the data transfer rate referred to as bandwidth by increasing the operational frequency to match the high FSB frequencies and by doubling the prefetch buffer data rate. There will be more about the memory prefetch buffer data rate later in this section. DDR2 is a 240 pin DIMM design that operates at 1.8 volts. The lower voltage counters the heat effect of the higher frequency data transfer. DRR operates at 2.5 volts and is a 188 pin DIMM design. DDR2 uses a different motherboard socket than DDR, and is not compatible with motherboards designed for DDR. The DDR2 DIMM key will not align with DDR DIMM key. If the DDR2 is forced into the DDR socket, it will damage the socket

and the memory will be exposed to a high voltage level. Also be aware the DDR is 188 pin DIMM design and DDR2 is a 240 pin DIMM design[1][3].

### 2.1.3 DDR3 SDRAM CONTROLLER

DDR3 was the next generation memory introduced in the summer of 2007 as the natural successor to DDR2. DDR3 increased the pre-fetch buffer size to 8-bits an increased the operating frequency once again resulting in high data transfer rates than its predecessor DDR2. In addition, to the increased data transfer rate memory chip voltage level was lowered to 1.5 V to counter the heating effects of the high frequency. By now you can see the trend of memory to increase pre-fetch buffer size and chip operating frequency, and lowering the operational voltage level to counter heat. The physical DDR3 is also designed with 240 pins, but the notched key is in a different position to prevent the insertion into a motherboard RAM socket designed for DDR2. DDR3 is both electrical and physically incompatible with previous versions of RAM. In addition to high frequency and lower applied voltage level, the DDR3 has a memory reset option which DDR2 and DDR1 do not. The memory reset allows the memory to be cleared by a software reset action. Other memory types do not have this feature which means the memory state is uncertain after a system reboot. The memory reset feature insures that the memory will be clean or empty after a system reboot. This feature will result in a more stable memory system. DDR3 uses the same 240-pin design as DDR2, but the memory module key notch is at a different location[2][4].

**Table 2.1 :- Comparison of DDR1,DDR2 and DDR3**

| DDR1 | DDR2 | DDR3 |
|---|---|---|
| 184 pins | 240 pins | 240 pins |
| 333 FSB | 666 FSB | 1333 FSB |
| 2n prefetch architecture | 4n prefetch architecture | 8n prefetch architecture |
| Support 4 banks | Support 6 banks | Support 8 banks of memory |
| Memory acess speed is twice compared to SDRDRAM | Memory acess speed is four times compared to SDRDRAM | Memory acess speed is eight times compared to SDRDRAM |

## 3. ARCHITECTURE OF DDR3 SDRAM [9]

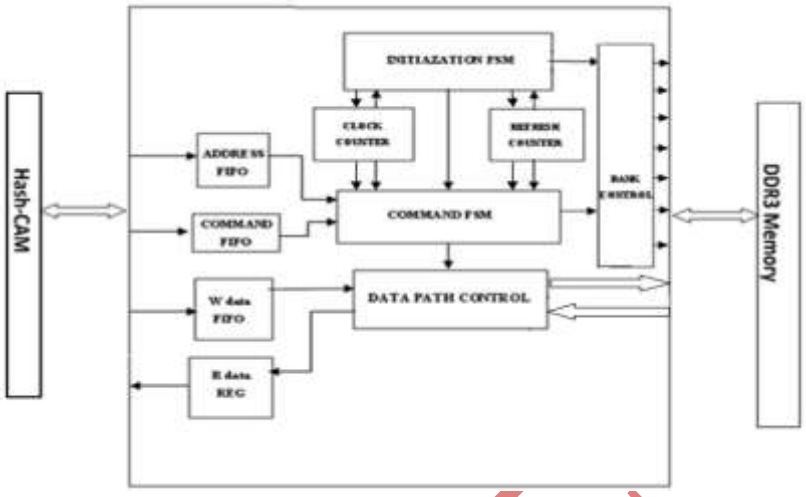


**Fig 3.1 Functional Block Diagram**

The architecture of DDR3SDRAM controller consists of Initialization fsm Command fsm, data path , bank control ,clock counter, refresh counter, Address FIFO, command FIFO ,Wdata FIFO and R_data reg . Initialization fsm generates proper i-State to initialize the modules in the design. Command fsm generates c-State to perform the normal write, read and fast write, read operations. The data path module performs the data latching and dispatching of the data between Hash CAM unit and DDR3SDRAM banks. The Address FIFO gives the address to the Command fsm so the bank control unit can open particular bank and address location in that bank. The Wdata FIFO provides the data to the data path module in normal and fast write operation. The R_data reg gets the data from the data path module normal and fast read operation.The DDR3 controller gets the address, data and control from the HASH CAM circuit in to the Address fifo. Write data fifo and control fifo respectively[8][9].

### 3.2.1 ADDRESS FIFO

DDR3 SDRAM controller gets the address from the Address fifo so that controller can perform the read from the memory or write in to the memory address location specified by the Address fifo. Here the Address fifo width is 13 bit and stack depth is 8.

### 3.2.2 WRITE DATA FIFO

DDR3 SDRAM controller gets the data from the Write data fifo in write operation into the memory address location specified by the Address fifo. Here the Address fifo width is 64 bit and stack depth is 8.

### 3.2.3 CONTROL FIFO

DDR3 SDRAM controller gets the command from the Control fifo controller can perform the read from the memory or write in to the memory address location specified

by the Address fifo. Here the Control fifo width is 2 bit and stack depth is 8. If the control fifo gives the "01" DDR3 controller performs the Normal read operation. If the control is "10" DDR3 controller performs the Normal read operation and if control is "11" DDR3 controller performs the Fast read operation[6].

### 3.2.4 READ DATA REGISTER

When DDR3 controller performs Normal read or Fast read operation Read data register gets the data send to the Hash Cam circuit.

## 4. FINITE STATE MACHINE

### 4.1 DIFFERENT STATES OF INITIAL FSM:

### 4.1.1 IDLE:

When reset is applied the initial fsm is forced to IDLE state irrespective of which state it is actually in when system is in idle it remains idle without performing any operations.

### 4.1.2 NO OPERATION (NOP):

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

### 4.1.3 PRECHARGE (PRE):

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks as shown in Figure 3.3. The value on the BA0, BA1 inputs selects the bank, and the A10 input selects whether a single

bank is precharged or whether all banks are precharged[4][7].

### 4.1.4 AUTO REFRESH (AR):

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

### 4.1.5 LOAD MODE REGISTER (LMR):

The mode registers are loaded via inputs A0–An. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

### 4.1.6 READ/WRITE CYCLE:

The Figure 4.1 shows the state diagram of CMD_FSM which handles the read, write and refresh of the SDRAM. The CMD_FSM state machine is initialized to c_idle during reset. After reset, CMD_FSM stays in c_idle as long as sys_INIT_DONE is low which indicates the SDRAM initialization sequence is not yet completed. Once the initialization is done, sys_ADSn and sys_REF_REQ will be sampled at the rising edge of every clock cycle. A logic high sampled on sys_REF_REQ will start a SDRAM refresh cycle. This is described in the following section. If logic low is sampled on both sys_REF_REQ and sys_ADSn, a system read cycle or system write cycle will begin. These system cycles are made up of a sequence of SDRAM commands [7].

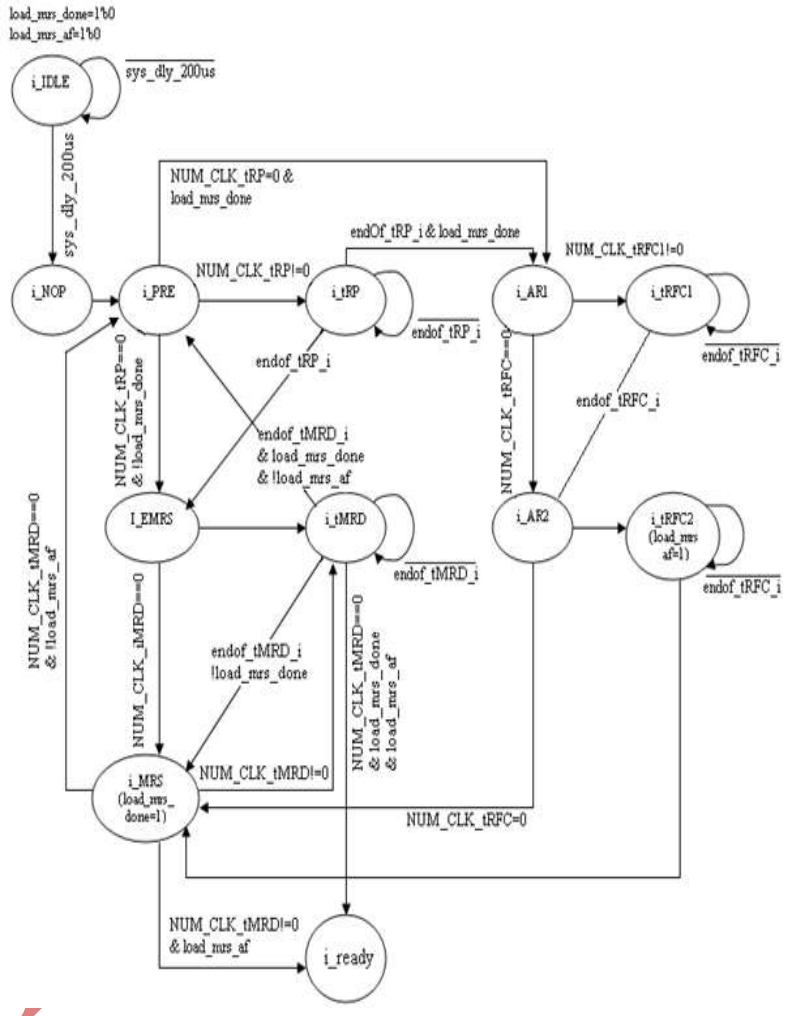


**Fig. 4.1 : Initial FSM State Diagram.**

### 4.2 COMMAND FSM STATE DIAGRAM:

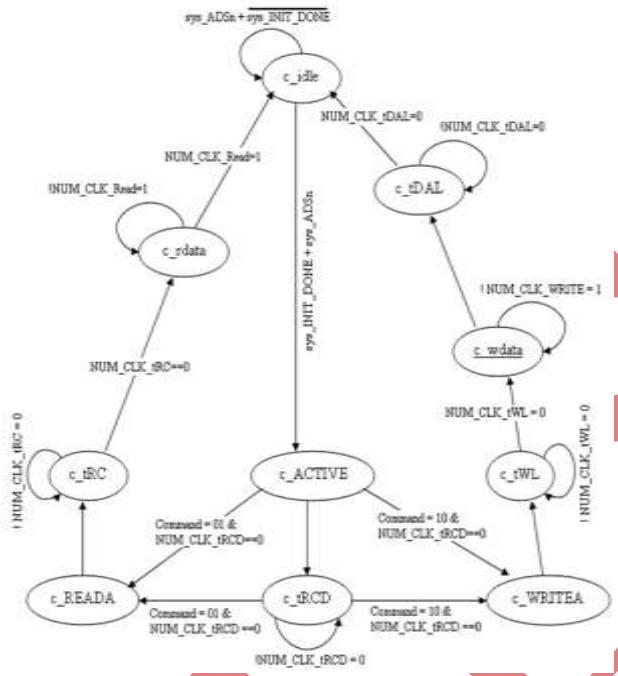


**Fig. 4.2: Command FSM State Diagram for Normal write and read.**

## 5. RESULTS

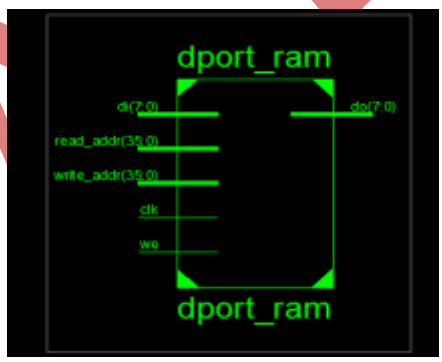


**Fig 5.1 Block diagram of dport ram**

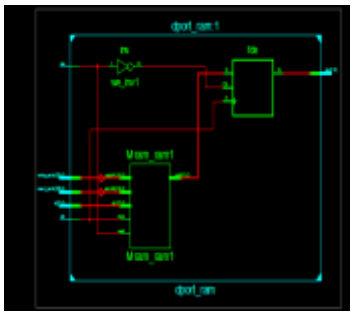

**Fig 5.2 Synthesis report of dport ram**


**Fig 5.3 Simulation report of dport ram**

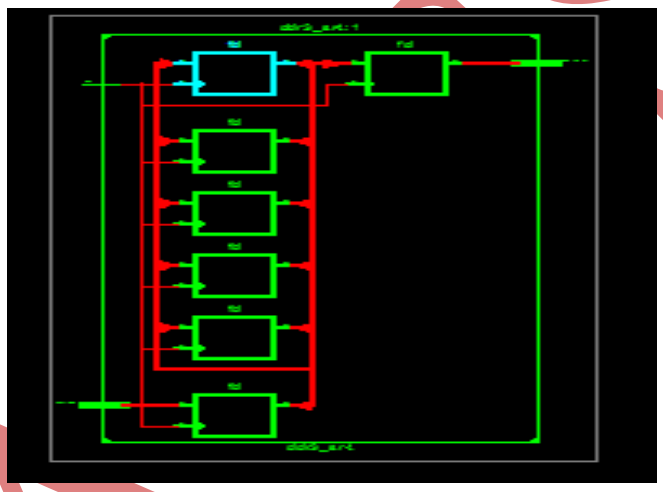

**Fig 5.4 Synthesis report of Multibits Shift Register**

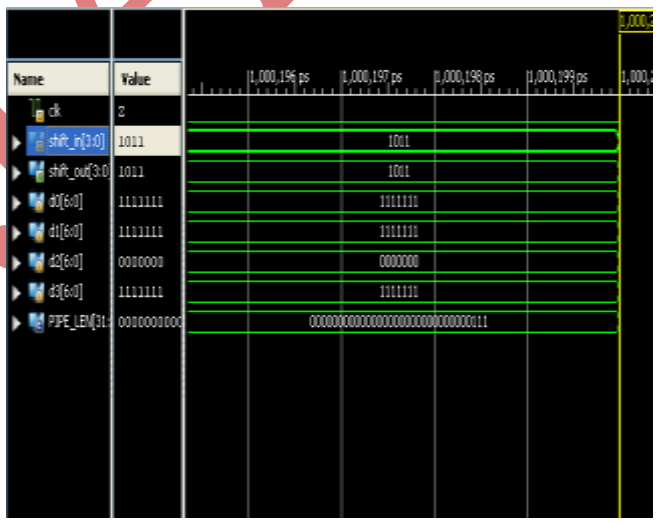


**Fig 5.5 Simulation report of Multibits Shift Register**

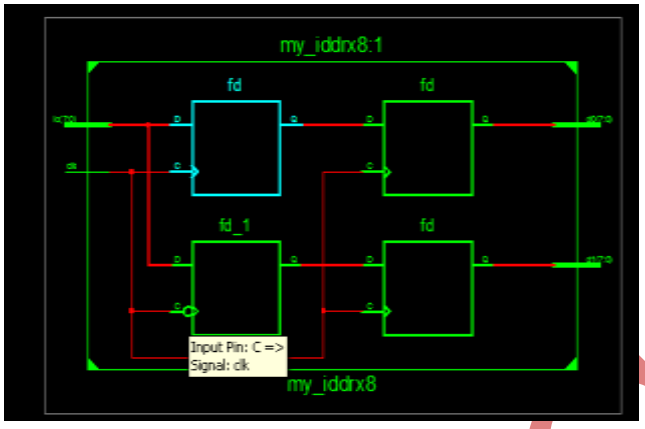


**Fig 5.6 Synthesis report of Single Data Rate Input Register**

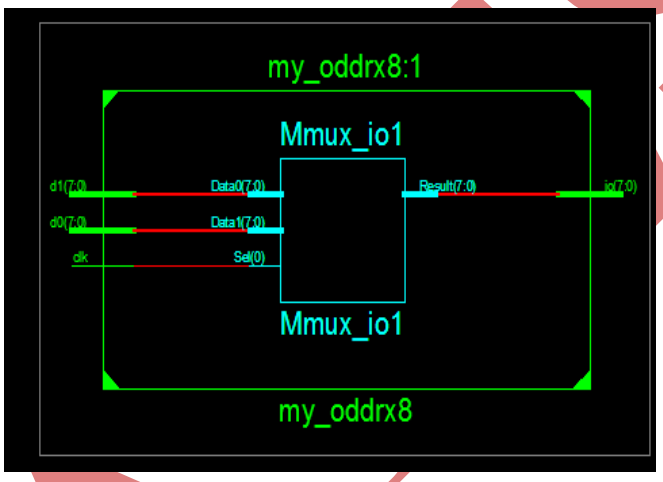


**Fig 5.6 Synthesis report of Single Data Rate to Double Data Rate Output Register**

## 6. CONCLUSION AND FUTURE SCOPE

DDR3 SDRAM achieves nearly twice the bandwidth of the preceding single data rate DDR2 SDRAM by double pumping (transferring data on the rising and falling edges of the clock signal) without increasing the clock frequency. Compared with DDRSDRAM the voltage of DDR3 SDRAM was lowered from 2.5V to 1.5V. This improves power consumption and heat generation, as well as enabling more dense memory configurations for higher capacities. Enhanced low power features with improved thermal design (cooler).Higher bandwidth performance increase, effectively up to 2400MHz. DDR SDRAM is a particularly expensive alternative to DDR3 SDRAM, and most manufacturers have dropped its support from their chipsets. DDR4 SDRAM is the 4th generation of DDR SDRAM. DDR3 SDRAM improves on DDR SDRAM by using differential signaling and lower voltages to support significant performance advantages over DDR SDRAM. DDR3 SDRAM standards are still being developed and improved.

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