OPTIMIZATION OF COMPARATOR FOR HIGH SPEED FLASH ADC

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ABSTRACT

In this paper we present an optimization of comparator parameters for high speed Flash ADC by individually optimizing its various components so that the overall performance of the resulting Flash ADC is improved over tradition0al Flash ADC's.Together with high speed as a parametrer,components are designed so that they operate with sampling frequency as high high as 70- 75MHz with lowest power consumption and operate on power supply voltage down to 2V for compatible with low power digital portion of the design as well as occupy less chip area. All the components are designed using the 0.18µm CMOS technology.

Keyword- Comparator,* ADC, *CMOS Technology

I. INTRODUCTION

In this paper, Flash analog to digital converters, also known as parallel ADC'S are used because they are the fastest way to convert an analog signal to digital signal. They are suitable for systems requiring very large bandwidths. However flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that cannot be addressed in any other way. Examples include Data Acquisition, satellite communications, radar processing, sampling oscilloscope and high density disk drives. Two Step approach is the preferred design as it reduces area as well as power. High resolution with low area is achievable however at the expense of speed. The speed of the A/D and D/A interfaces must scale with the speed of the digital circuits in order to fully utilize the advantages of the advanced technologies. Recently low power, compact size and high resolution ADC interface circuits have been in great demand for portable system such as camcorders, cellular phones and personal digital assistance etc.High integration analog to digital interfaces for portable battery powered system require A/D converters and other interface elements that dissipate the lowest possible power and operate on supply voltages compatible with the digital parts of the system.

Also the cost and performance makes it desirable to achieve high levels of integration on a single chip for mixed signal processing systems. In the previous years some of the high speed ADC's have been designed using bipolar technology, but the fabrication of these devices become very complex and large chip area and power. The motivation for CMOS is that higher levels of integration and low power are possible then in the bipolar implementation

II. FLASH ADC ARCHITECTURE WITH TWO- STEP APPROACH

However, we have various architectures of Flash ADC'S as stated in the literature, but to achieve our main goals that is high speed and low power, Two-Step architecture is used. Firstly, this architecture improves the speed of our ADC, may be a little bit, but the optimized components enhance the speed to a significant level.

In many applications it is necessary to have a smaller conversion time. ADC's designed for such applications are the high speed ADC's that use the parallel techniques to achieve the shorter conversion times. One way of achieving this is to increase the speed of the individual components, which will increase the speed of the complete system. Sample time due to the sample and hold circuit may be a limiting factor for the speed. We proceed to design a system without sample and hold circuit.

The potential of two-step flash architectures for realizing fast, high resolution analog to digital converters are demonstrated in a number of designs [4] [6][7]. With the conversion rates approaching half those of fully parallel (flash ADC) these architectures provide relatively small input capacitances together with the low power dissipation and can be used to achieve resolutions in the range of 10 to 14b which is well above that obtained in the single stage flash design.

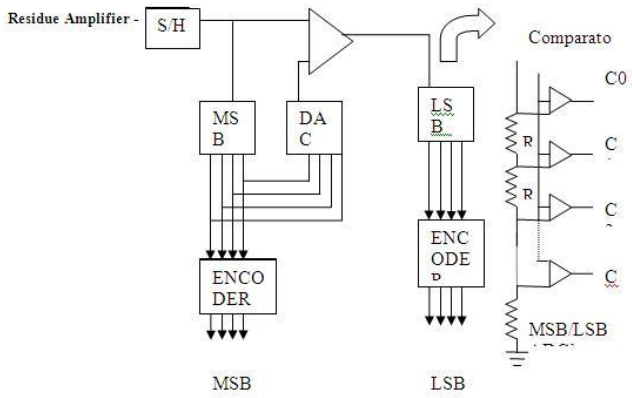

Figure 1 Two-Step Flash ADC Architecture

The basic structure of the two-step converter is shown in Fig. 1.The first converter generates a rough estimate of the value of the input, and the second converter performs a fine conversion. The advantage of this architecture is that the number of comparators is greatly reduced from that of the flash converter from 2^N-1 comparators to 2 (2^N-1) comparators. For example, an 8 bit flash converter requires 255 comparators, while the step requires only 30. The tradeoff is that the conversion process takes two step instead of one, with the speed limited by bandwidth and settling time required by the residue amplifier and the summer. regenerative comparators the open loop comparators are operational amplifiers without compensation. Regenrative comparators use positive feedback, to accomplish the comparison of the magnitude between two signals necessary to understand which converter algorithms or architectures to choose for the specific application. For example when the conversion bandwidth is relatively small, it could be advantageous to use a high sampling ratio and some overlapping technique to reduce the noise energy within the signal band. However the trade off in the converter design is normally between resolution and bandwidth. The higher the bandwidth the lower the resolution and so on. One of the most suitable candidate for high speed and high resolution is the current steering DAC.The Single Cell of our DAC has the structure as given in Fig.3.Single cell of the DAC corresponds to 1-bit DAC.To design a full

functional DAC we have to combine these cells together with the regulator circuitry. The comparator design used for the A/D application is based on [2][5][6] .This is shown in Fig. 2.Operating analysis of the comparator is as given by [5][2].Finally, by further reducing and solving the inequalities we obtain the relation $W_{12}>1/3W_{4.}$Similarly other relations are calculated at node c & d.

III. COMPARATOR OPTIMIZATION

To improve the speed we optimize the different components of the ADC individually and independently. The architecture of the different components of ADC are chosen so that when they are cascaded together they enhance the speed significantly.

3.1 Comparator Design

In high speed analog to digital converters, comparator design has a crucial influence on the overall performance that can be achieved. Converter architecture that incorporate a large number of comparators in parallel to obtain a high throughput rate impose stringent constraint on delay, resolution, power dissipation, input voltage range that accompany the integration of comparator circuits in low-voltage scaled VLSI technologies, severely compromise the precision that can be obtained.

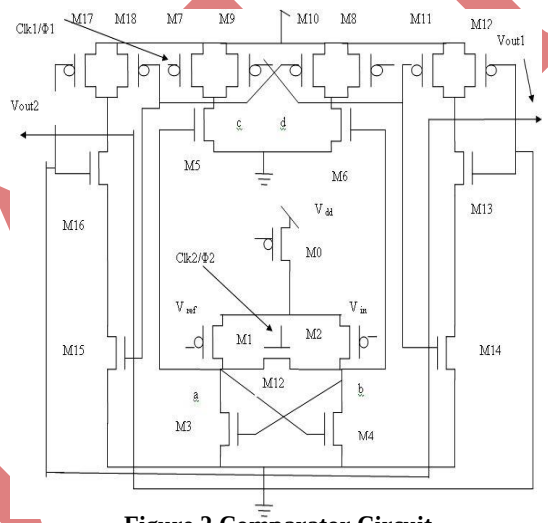

Figure 2 Comparator Circuit

This is shown in Fig. 2. Operating Analysis of The comparator is as given by [5][2]. Finally, by Further reducing and solving the inequalities we obtain The relation $W12>1/3W_{4.}$Similarly other relations are calculated at node c&d. A high performance comparators need to amplify a small input voltage (the difference between the input voltage and the reference voltage) to a level large enough to be detected by the digital logic circuits within a very short time. In its simplest form, the comparator can be considered as a 1 bit analog to digital converter. Comparators can be divided into open loop and Single Cell DAC Circuit Design: Digital to analog converter is the integral part of an ADC.There is a number of means of converting a digital signal into an analog signal representation. The approaches differ in speed chip area, power efficiency, and achievable accuracy etc. It is therefore necessary to understand which converter algorithms or architectures to choose for the specific application. For example when the conversion bandwidth is relatively small, it could be advantageous to use a

high sampling ratio and some overlapping technique to reduce the noise energy within the signal band. However the trade off in the converter design is normally between resolution and bandwidth. Higher the bandwidth the lower the resolution and so on. One of the most suitable candidates for high speed and high resolution is the current steering DAC. The Single Cell of our DAC has the structure as given in Fig.3.Single cell of the DAC corresponds to 1-bit DAC. To design a full functional DAC we have to combine these cells together with the regulator circuitry.

3.2 Differential Amplifier/Residue Amplifier Design

The last circuit of our ADC is Differential amplifier .It is used as a subtracted amplifier. Simple circuit of differential amplifier is used as shown in Fig. 4.

IV RESULT AND DISSCUSSION

The main purpose of our design is to achieve high speed with low power. . To achieve this .T-Spice code of the individual components has been made using Tanner tools .The W/L ratios of all the transistors of the components design are calculated using the design relations developed as mentioned and using the model parameters of 0.18 µm technology of Tanner tool. The output waveforms obtained of different components are shown in Fig.5, Fig. 6, Fig.7. Reference voltage is taken constant. Parameters specification obtained are shown in Table 1.1.

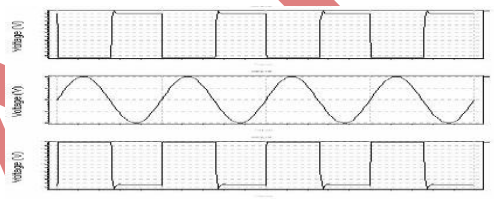

Figure 5 Comparator output for Vref=0.125V

Table 1.1 Parameter Specification for complete ADC

Resolution	8-bits
Input Signal Frequency	2MHz
Sampling Frequency	150MHz
Technology Used	0.18µm
Analog Input	0-1V(P-P)
Supply Voltage	2 V

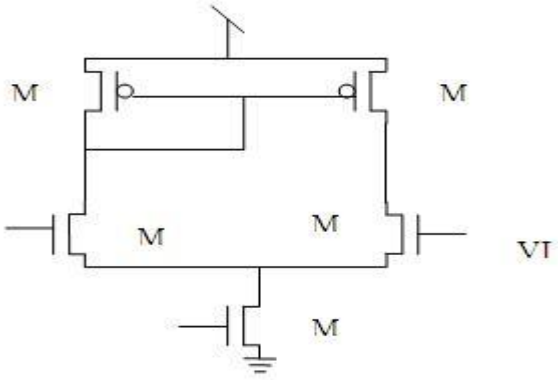

Figure 4 Residue Amplifier

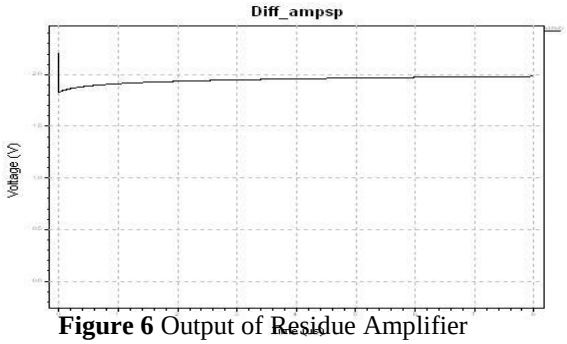

Figure 6 Output of Residue Amplifier

Table II. The 6-bit and 8-bit ADC simulation results For Comparator

Feature	6 bit	8 bit
Speed	1.1 GSPS	0.15 GSPS
Area	0.043mm^2	0.228 mm^2
Power	59.91mW	24.8mW/ 0.44 mW
Vref. (Revised)	0.8 mV	0.8 mV to 1.3mV

Table III. Comparisons to other high speed ADCs

ADCs	Technology	Speed	Power
6 bit TIQ	CMOS0.25	1.1GSPS	59.91
8 bit TIQ	CMOS0.25	1GSPS	256.09
6 bit Flash	GaAs 0.5	2GSPS	970
6 bit Flash	CMOS 0.6	0.2 GSPS	380
4 bit Flash	GaAs 0.8	1.18GSPS	185.6
6 bit Flash	CMOS 0.4	0.5 GSPS	400
8bitpipeline	CMOS 0.6	0.15GSPS	395
6 bit Flash	CMOS 0.6	0.5 GSPS	330
8 Bit Flash	CMOS0.18	0.15GSPS	24.8/ 0.44mW
8 Bit Flash	CMOS0.18	0.15GSPS	24.8/ 0.44mW

V CONCLUSION

The work presented in this paper is to optimize the performance characteristics of the comparator for ADC components. For this design technique are developed for individual components of the ADC. Based on the scheme developed wider range of reference voltage (i.e- 0.8V to 1.3 V), W/L ratios for all the transistors are calculated using the model parameters of the 0.18µm CMOS technology. Individual components are implemented independently. The preferred technology as with the scaling of operating voltages to low values down to 2V, it ensures a high performance circuit. The designed components are best suited for a complete flash ADC. The table 1 shows the parameter and their values for our 8 bit adc. The table II displays the simulation result for 6 bit & 8 bit ADC.

The table III crates a comparison between Speed and power with different ADC.

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