OPTIMIZED POWER, DELAY AND LOGIC PERFORMANCE IN POWER GATED CASCADED INVERTERS DESIGN

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ABSTRACT

This work introduces the concept of power gating on differently scaled technologies and finally getting results which are best for the further work. The different analyses of power are done on the base design and the same analyses are also done on the power gating approach. It was found that the 90nm length technology is giving optimized power dissipation which is transmitted from V_{dd} to main logic circuit as compare to other technologies e.g. 250nm, 120nm etc. It was also found that we are providing the weak one from the power supply during the transistors are in the not working state. One more effect is caused by ground bounce noise that the current back itself toward the transistors when it go toward the ground, so this ground bounce noise effect is also reduced by again using some concept which we were using to reduce the power transmitted from V_{dd}. Here from the ground we are providing weak zero to the logic circuit, so the during not working condition the transistor consumes low power, so the overall power is reduced. The logic and the delay performance is also optimized in our work.

Keywords: Base Design, Cascaded Inverters, Power Gating Design, 90nm Length Technology

I. INTRODUCTION

The technology is scaled down day by day, but as the scaling of technology has more demand so the voltages also have to be scaled down which brings a lot of other design and the performance issue e.g. power reduction in the scaled down version of voltage and length technology, but as we reduce the power the logic level of the design is disturbed. So power becomes the main issue here that it has to be reduced.

The power in any circuit plays the very important role, here we are dealing with the microelectronics circuits they consumes power in the range of 10^{-6} or less, so this is the basic objective of this report to reduce the power of integrated circuits in scaled down version of the technology and also to check the delay performance on the same technology.

Figure: 1 is showing the exponential components increment per chip, and exponential length per chip, so this becomes the main issue what will be power dissipation when transistors are fabricated so close to each other and the which lead us to the topic which we are working that the issue of power gating is becoming very critical as the technology is scaled down, this topic deals with the 90nm length scaling technology [1].

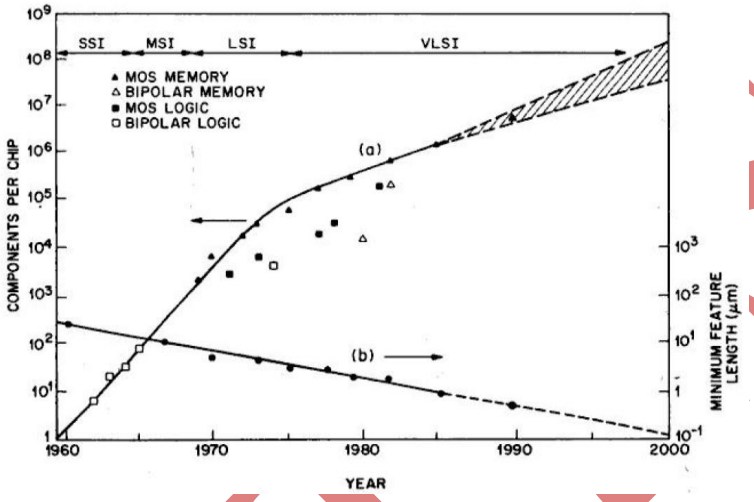


Figure: 1 (a) Exponential growth of number of components per IC (b) Exponential decrease in length [1]

As we are doing the power gating it means we are going to change the basic design, when the design change take place one have to worry about the logic performance and time delay other than the power reduction. So in our design we keep all these things in our mind.

II. POWER GATING

Power-gating which is based on transistors is implemented when we place sleep transistors between the circuit and the Vdd or the ground. The first one we call headers (Vdd) and the second one ground we call it footers. Footers are more area efficient generally it is because as we need the high n-type mobility which means less number is needed. Mostly commercials designs implement headers because of its easier design and analysis, notably when multiple power domains or an external switchable voltage regulator is used [2]. But header has its limitation the two limitation of header shown in Figure: 2. First limitation of the headers is that they themselves leak, so we cannot say that leakage is eliminated. Second limitation of the headers, is the current flowing though them creates a voltage drop on the power-gated circuit which reduces the performance of the circuit [3].

This reduces the performance of the main circuit because small variation in voltage leads to very big change in the performance. The trade-off between delay increase and off-state leakage reduction is the width of the headers. But in industry the size of the headers is selected such that the supply voltage drop is less than 10%, but large area overhead is the consequence of this, the sleep-mode leakage reduction is only around 90% [4].

This leakage can lead to worst performance during the long idle period. Here we need to achieve large reduction in off state leakage without effecting the main performance of the circuit like we don't want to disturb the main logic of the circuit, the optimized delay, and the power, all these things are mainly focused in this work.

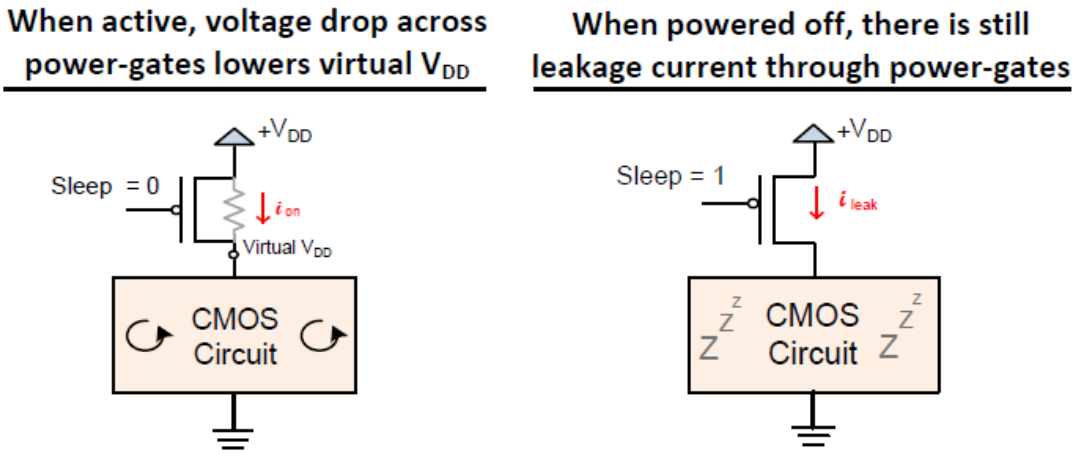


Figure: 2 The Limitation In Power Gating.

III. THE BASE DESIGN ANALYSIS

The base design is shown in figure: 3, this design represents the cascading scheme in which we have connected the four inverter in cascaded manner, so the resultant waveform obtained from this design will be the original waveform which we have applied on the input. The working principle of an inverter we have seen that in our text available in [5]. The fabrication process of inverter can also be seen [2]. Let's only focus to the design which we have used as the base design which is given in figure: 3.

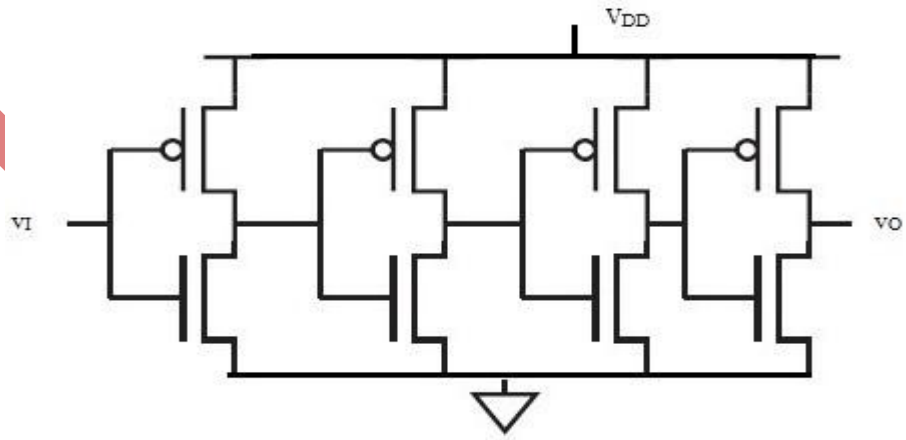


Figure: 3 The Cascaded Inverters

In figure: 3 the voltage V_{DD} which is applied to the base design which will transmit the power to the design and then all inverters will come into the active mode and they will behave like individually as single inverter which is found in text [5], v_I is the input signal and v_O is the output signal. The ground potential is applied at the source terminal of each inverter. The three figures of the base design are shown in figure: 4,5 and 6, in these figures we have used the different technologies e.g. .25 um, 180nm and 90nm respectively.

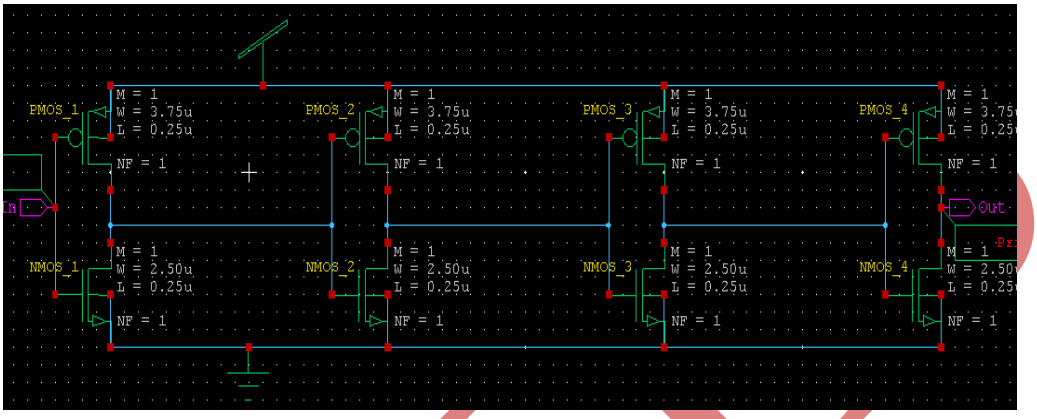


Figure: 4 The Base Design Using .25um Technology

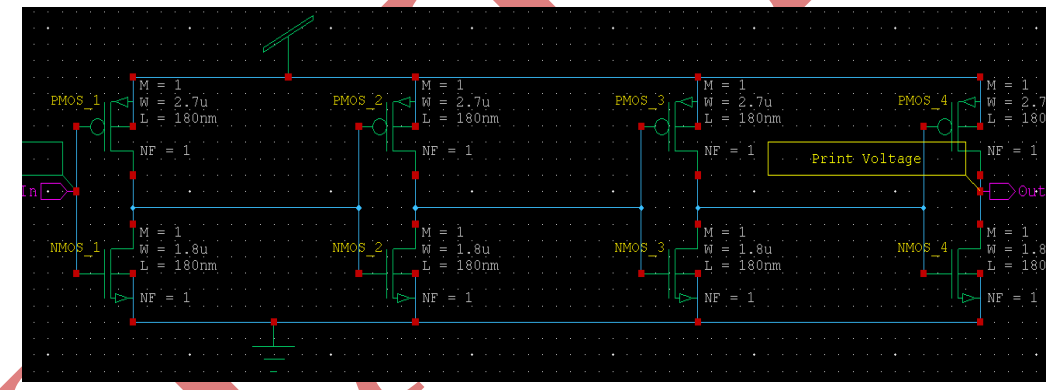


Figure: 5 The Base Design Using 180nm Technology

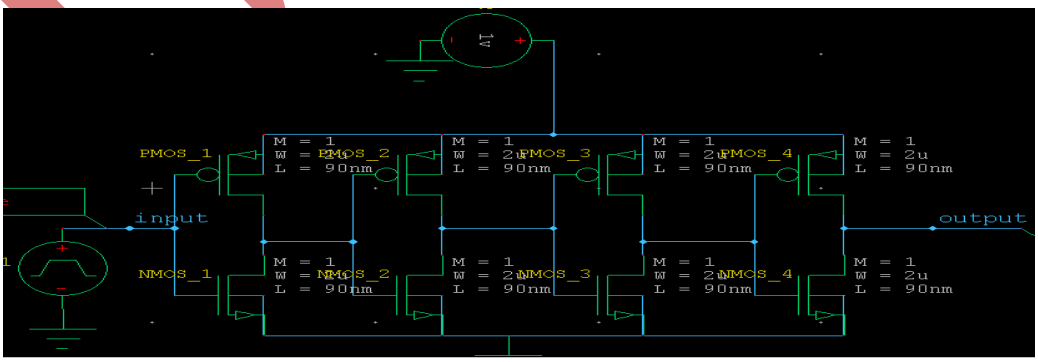
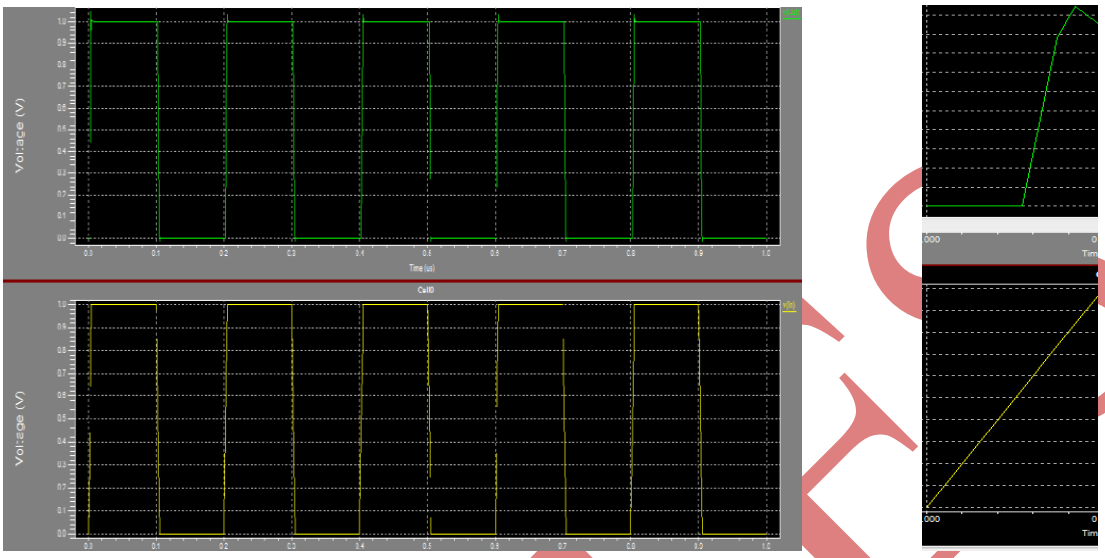


Figure: 6 The Base Design Using 90nm Technology

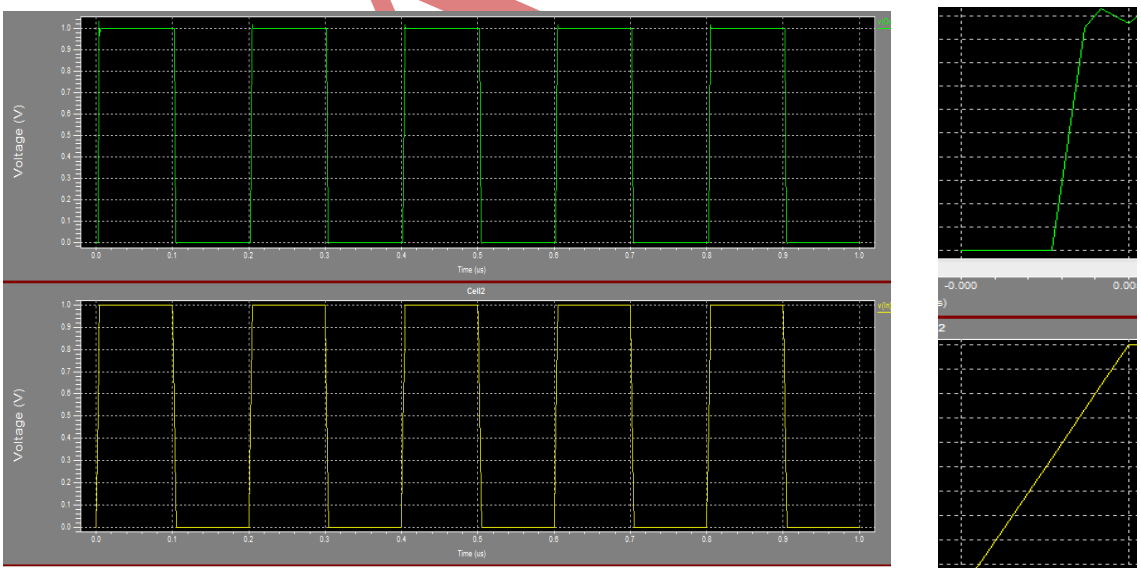
The results of figure: 4 which is using .25um technology is shown in waveform shown in figure: 7. The delay and power performance will be shown in table: 1.



(a) (b)

Figure: 7 The Base Design Output at .25um (a) The Whole Waveform, (b) Zoomed Portion

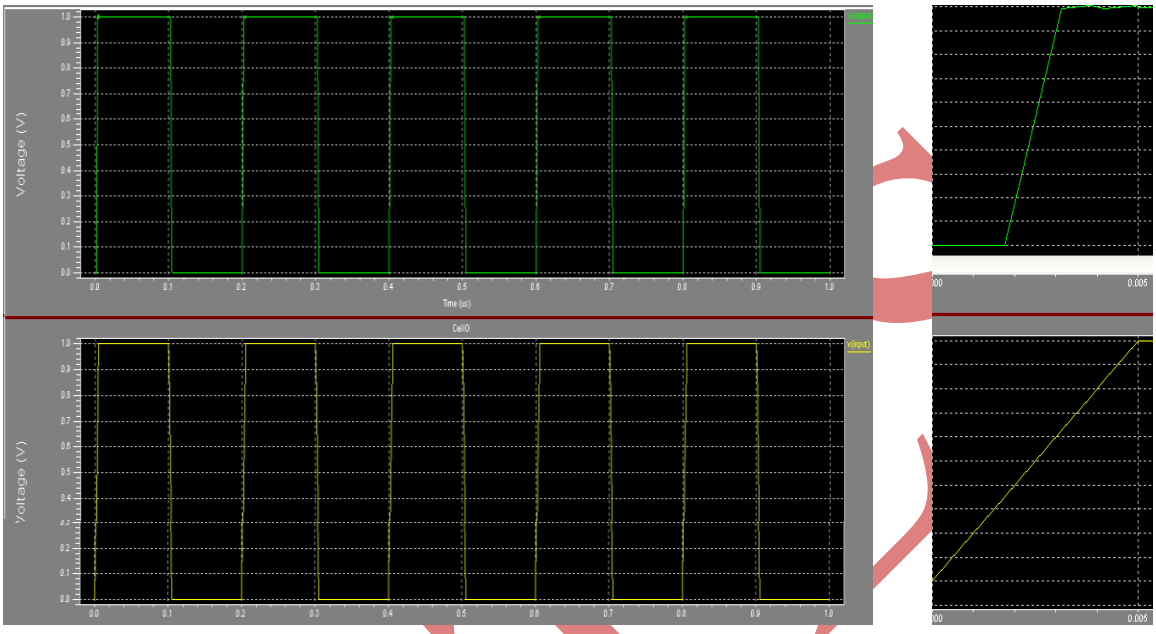
The results of figure: 5 which is using .180nm technology is shown in waveform shown in figure: 8. The delay and power performance will be shown in table: 1.



(a) (b)

Fig. 4.3 The Base Design Output at 180nm (a) The Whole Waveform, (b) Zoomed Portion

The results of figure: 6 which is using 90nm technology is shown in waveform shown in figure: 9. The delay and power performance will be shown in table: 1.



(a) (b)

Figure: 9 The Base Design Output at 90nm (A) The Whole Waveform, (B) Zoomed Portion

Table: 1 Comparative Study of Power and Delay in Base Design Using Different Technologies

V_{DD}	Length Technology	Consumed Power	Time Delay
1V	.25um	.585uW	.77ns
1V	180nm	.437uW	.07ns
1V	90nm	3.95uW	.7ns

IV. POWER GATING ANALYSIS ON CASCADED INVERTERS

The power gating design is shown in figure: 10, in this design we have considered all the parameters that we have discussed in previous section. The main problem we have discussed is leakage problem of the header switches, and also there is some problem found footer switches as found in [30]. So we have used both type of the sleep transistors in our design as found in [33]. The advantage of using such design will be found in the table: 2. In our analysis we check our design at different technologies as shown in table: 2.

The basic design of our scheme is shown in figure: 10. This design is further shown in different figures but in each we will be using the different length technologies. So we can do the comparative study. In this work we have basically taken the 90nm technology of length.

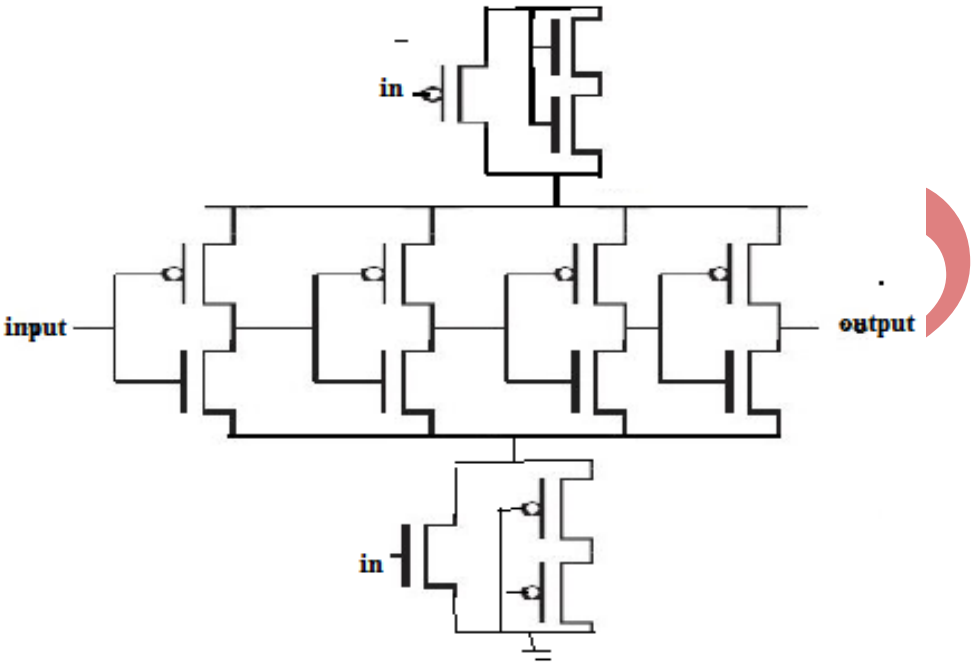


Figure: 10 Power Gating Design [10]

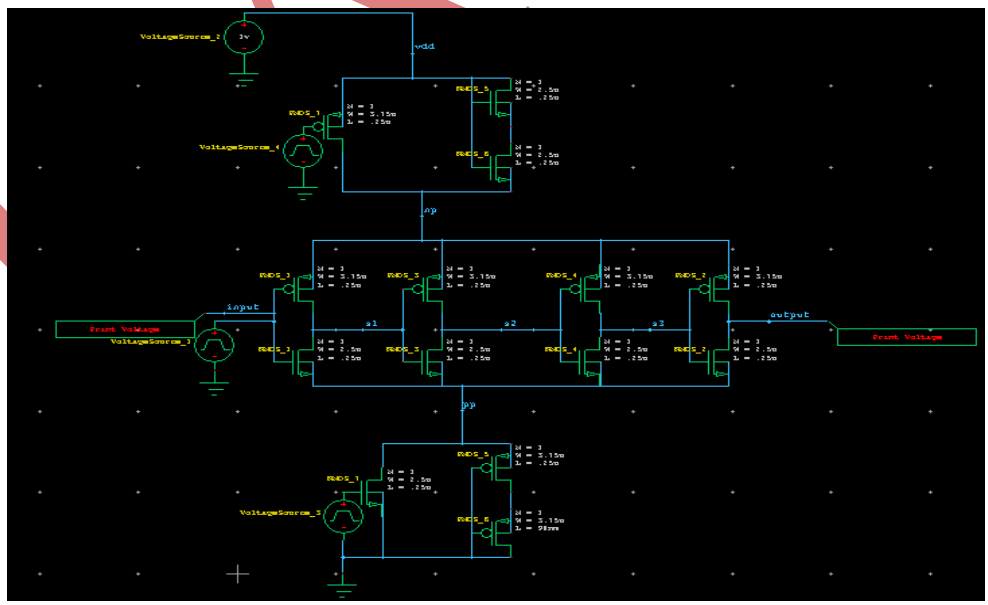


Figure: 11 Power Gating Design Using .25um Technology

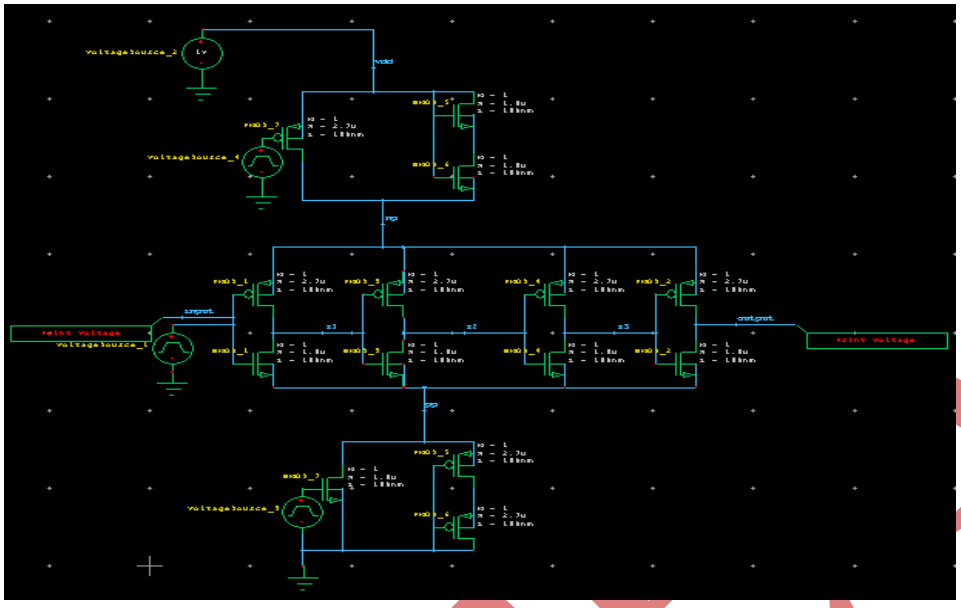


Figure: 12 Power Gating Design Using 180nm Technology

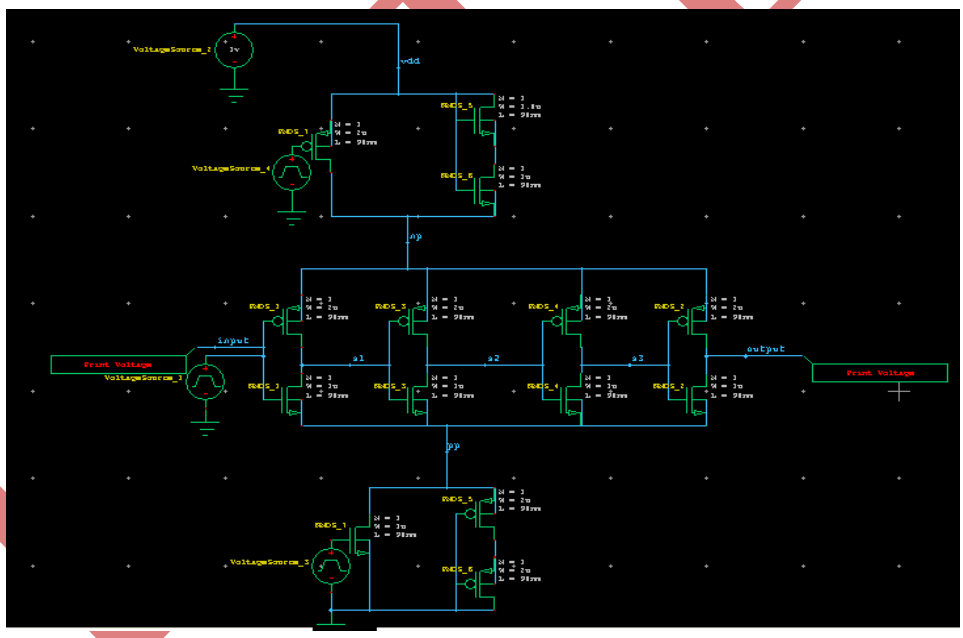


Figure: 13 Power Gating Design Using 90nm Technology

In figure: 11, 12, and 13 we are showing the different simulated version of cascaded inverters, the different thing in these design is that we are using the different technologies in each design. The different technologies we used are .25um, 180nm, and 90nm respectively in fugures: 11, 12, and 13. The result obtained from these design is shown in table: 2

Table 2: Comparative Study of Power and Delay in Power Gating

V_{DD}	Length Technology	Consumed Power	Time Delay
1V	.25um	.356uW	90.12ns
1V	180nm	.232uW	1.54ns
1V	90nm	.96uW	2.15ns

V. CONCLUSION

The conclusion of this work is that we have obtained the various results at different technologies on the two designs, in which one we called the base design and the other we called the power gating design. This work is basically performed to calculate the power and the delay performance of the base design and the power gating design, so we have done the comparative study at different levels. The tables we are showing for different designs in table: 1, and 2. One thing is noticed here that the power consumption in table: 1 is more than the power consumption in the power gating design shown in table: 2. So the power gating becomes the choice of electronics engineers for low power design. As from the previous discussion have seen the output waveforms in which we saw that the logic was not retained in most of the power gating scheme, but at 90nm the output waveforms are more suitable they are providing the weak 0, so we are gating the reduced power. One more thing is noticed in table 5.2 that the delay performance of power gating is more than base design. But in the 90nm design these two performances are also found improved. So at last we can say that the 90nm technology is satisfying all of the criteria, in this we are getting some reduced power and improved logic performance, and improved delay performance. The trade offs in 90nm are done in power and delay performance but as they both combined are the smallest results, so these tradeoffs giving us the better results at this technology.

The future work is to improve the delay performance and to get the logic again to original state. And also to improve the power performance even to more lower level.

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