DESIGN AND IMPLEMENTATION OF SLEEP TRANSISTOR BASED LOW POWER CMOS DESIGN FOR SUBMICRON VLSI TECHNOLOGIES

P. Nagarani[1], B. Prasannajyothi[2], D.Naga Poornima[3]

[1]Reasearch Scholar, Dept of ECE Aurora's Research and Technological Institute, Hyderabad, (India)
[2]Asst. Prof, Dept of ECE, Aurora's Research and Technological Institute, Hyderabad, (India)
[3]Application Engineer at UNI String Tech Solutions Pvt Ltd, Hyderabad, (India)

ABSTRACT

In today's world mobile technology is a currently growing technology. So that the concentration of mobile battery is increasing in level (power consumption). When a mobile phone is in standby mode, certain portions of the circuitry are shut down. Even though de-activated, these circuits have some leakage current flowing through them. Even if the leakage current is much smaller than the normal operating current of the circuit, it depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. In this paper leakage power and the ground bounce noise is reduced by the use of sleep transistor in CMOS full adder design. Size of the sleep transistor is determined by transistor resizing approach. 4 bit ripple carry adder is implemented using 1 bit adder as a reference by using 130 nm CMOS technology.

Tools Used: ***Electric, LT-SPICE.***

Keywords: ***Full Adder, Ground Bounce Noise, Schematic, Layout, Leakage, Sleep Transistor.***

I. INTRODUCTION

Addition is one of the primary operations in arithmetic circuits. These adder cells commonly aimed to reduce power consumption and delay. These studies have also investigated different approaches realizing adders using CMOS technology. The designer's concern for the level of leakage current is mainly aimed at minimizing the power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call). When a mobile phone is in standby mode, some part of circuitry is off position. Even though de-activated, these circuits have some leakage current flowing through them. Even if the leakage current is much smaller than the normal operating current of the circuit, it depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only

depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30x increase in gate leakage. There are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further reduction of peak of ground bounce noise is possible with used novel technique.

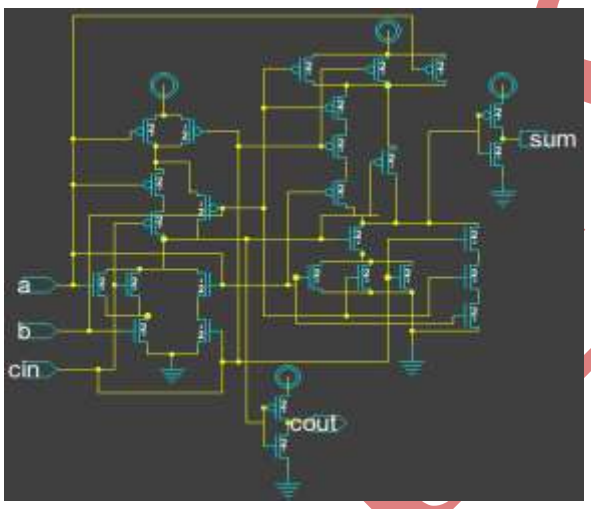

Fig.1. Full Adder Conventional Design

II. LEAKAGE CURRENT AND ITS IMPORTANCE

Leakage [1] current is the current that flows through the protective ground conductor to ground. In the absence of a grounding connection, it is the current that could flow from any conductive part or the surface of non-conductive parts to ground if a conductive path was available (such as a human body). There are always extraneous currents flowing in the safety ground conductor. Electrical equipment commonly includes a grounding system to provide protection against a shock hazard if there is an insulation failure. The grounding system usually consists of a grounding conductor that bonds the equipment to the service ground (earth). If there is a catastrophic failure of the insulation between the hot (power) line and touchable conductive parts, the voltage is shunted to ground. The resulting current flow will cause a fuse to blow or open a circuit breaker; preventing a shock hazard. Obviously, a possible shock hazard exists if the grounding connection is interrupted, either intentionally or accidentally. The shock hazard may be greater than supposed because of the leakage currents. Even if there is no insulation failure, interruption of the leakage currents flowing through the ground conductor could pose a shock hazard to someone touching the ungrounded equipment and ground (or other grounded equipment) at the same time. This possibility is of much more concern in medical applications, where a patient may be the recipient of the shock. A fatal shock could result if the patient is in a weakened condition or unconscious, or if the leakage current is applied to internal organs through patient contacts. The double insulation provided in non-grounded equipment provides protection by using two separate layers of insulation.

The protection in this case is ensured because both layers of insulation are unlikely to fail. However, the conditions that produce leakage currents are still present, and must be considered.

2.1. Types of Leakage Current

Ac leakage and dc leakage, Dc leakage current usually applies only to end-product equipment, not to power supplies. Ac leakage current is caused by a parallel combination of capacitance and dc resistance between a voltage source (ac line) and the grounded conductive parts of the equipment. The leakage caused by the dc resistance usually is insignificant compared to the ac impedance of various parallel capacitances. The capacitance may be intentional (such as in EMI filter capacitors) or unintentional. Some examples of unintentional capacitances are spacing's on printed wiring boards, insulations between Semiconductors and grounded heat sinks, and the primary-to-secondary capacitance of isolating transformers within the power supply.

III. RIPPLE CARRY ADDER

A ripple carry adder is a digital circuit [2] that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded (series), with the carry output from each full adder connected to the carry input of the next full adder in the chain. Figure 2 shows the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder. Notice from the below figure input is from the right side because the first cell traditionally represents the least significant bit (LSB). 4 bit ripple carry adder layout with the proposed design is mentioned in below fig.9.

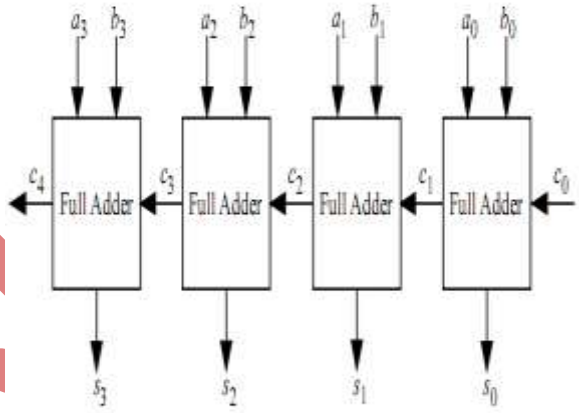

Fig.2. 4 Bit Ripple Carry Adder

VI. Sleep transistor

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit: Static power Includes sub threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub threshold leakage is the most prominent. Dynamic power: Includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Techniques for

leakage power reduction can be grouped into two categories: state preserving techniques; where circuit state is retained and state destructive techniques; where the current Boolean output value of the circuit might be lost. A state preserving technique has an advantage over a state destructive technique in that with a state preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. The most well known traditional approach is the sleep approach. In the sleep approach, a "sleep" PMOS transistor is placed between Vdd and the pull up network of a circuit and a "sleep" NMOS transistor is placed between the pull down network and Gnd. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

V. PROPOSED FULL ADDER'S

The conventional CMOS adder has been shown in Fig. 1. As told earlier, it is the base adder Implementation of Power Gating Technique in Cmos full Adder Cell to Reduce Leakage Power and Ground Bounce Noise for Mobile Application and all simulation results comparison has been done with it. It consists of 28 number of transistors as PMOS pull up and NMOS pull down networks to produce desired outputs. Here the sizing of transistors plays a vital role. Here, the transistor ratio of PMOS to NMOS has been kept 2 for an inverter and on considering the remaining blocks as equivalent inverters also follows the same ratios. The adder circuit was modified with proper sizing using power gating technique of 1 bit cmos full adders and has been shown in Fig.3 and Fig.4. In Fig.3 power gating technique has been shown to reduce the leakage power by placing a sleep transistor between actual ground rail and circuit ground (virtual ground). Here low leakage NMOS is used as a sleep transistor. Estimation of the ground bounce noise is done when circuit is connected to the sleep transistor. Sub threshold current is directly proportional to W/L ratio of transistor. So the sizing of the transistor reduces the standby leakage current to a very great extent. Pseudo NMOS and Pass transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Mux's and XOR based circuits are advantageous when we implement by the pass transistor logic. The dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. Usually, none of the mentioned styles can compete with CMOS style in robustness and stability. This is considered as a Base case throughout this paper. All comparisons are done with Base case. The CMOS structure having combination of PMOS pull up and NMOS pull down networks to produce considered outputs. Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a main role in static CMOS [3] style. It is observed in the conventional full adder circuit that the transistor ratio of PMOS to NMOS is double for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio does not give good results with respect to noise margin and standby leakage power. Modified adder circuits with sizing are proposed in full adder design1 and full adder design2 targeting the ground bounce noise. Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with a proposed novel technique. Modified sizing are shown in fig respectively.

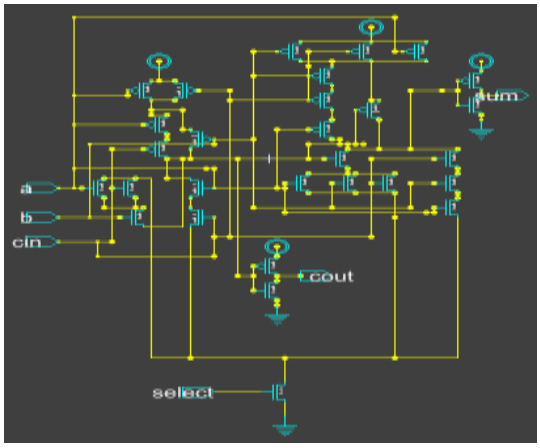

Fig.3. Design 1 with sleep transistor (with sizing)

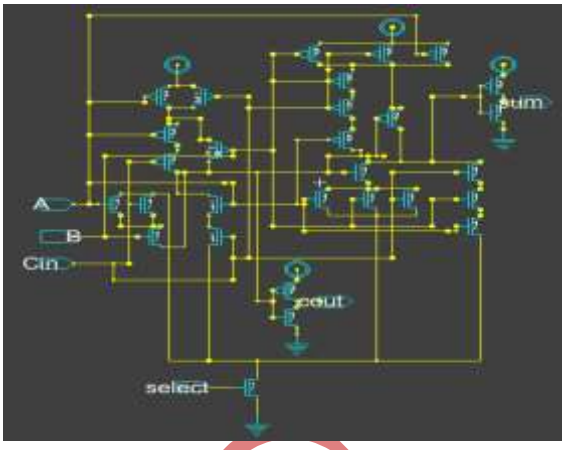

Fig.4. Design 2 with sleep transistor (with sizing)

VI. GROUND BOUNCE NOISE REDUCTION TECHNIQUE

Here, we have presented different ways to reduce the leakage power of one bit full adder circuits. The same full adder circuit designs i.e., sleep method with little modifications as discussed below can be used to reduce the ground bounce noise and further may also reduce the leakage power. During last one decade various alternatives and improvements of conventional power gating has been proposed to reduce the ground bounce noise [4] during mode transition. In staggered Phase Damping technique during standby to active power mode transition, staggered Phase damping delays the activation time of one of the two sleep transistors relative to the activation time of the other one by a time that is equal to half the resonant oscillation period. As a result, noise cancellation occurs once the second sleep transistor turns on due to phase shift between the noise induced by the second sleep transistor hence reduction in settling time. But it is not very effective in reducing the peak noise due to the initial spike. And in another scheme there will be a two stage procedure. In first stage sleep transistor working as diode by turn on the control transistor which is connected across the drain and gate of the sleep transistor. Due to this, drain to source current of the sleep transistor drops in a quadratic manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wakeup time. In second stage control transistor is off so that sleep transistor works normally. This method is not effective to suppress the overall fluctuations in the ground bounce noise. Therefore, the technique must be adopted to reduce both peak of ground bounce noise and reducing the overall fluctuations in the ground bounce noise. The idea is to combine both the above techniques to further reduce the peak of ground bounce noise and overall power mode transition noise in the proposed technique fig.5. and the below table I shows the power comparisons of the designs.

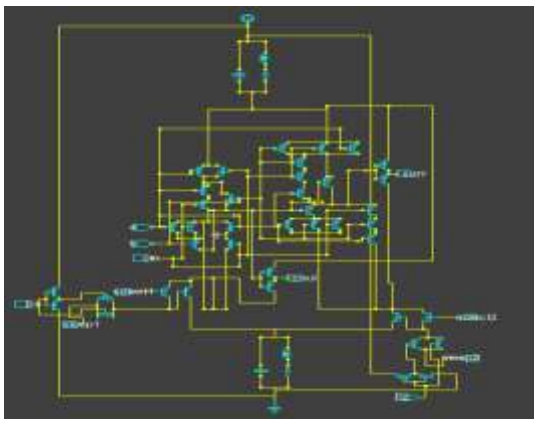

Fig.5. Ground Bounce Noise Reduction Circuit

TABLE I

Power comparisons

S. No	Design	Average power	Leakage power
1	conventional	10.135uW	666.13pW
2	Desin-1	7.623uW	266.45pW
3	Desin-2	5.967uW	186.27pW
4	Ground bounce noise design	1.386uW	156.21pW

VII. SIMULATION RESULTS

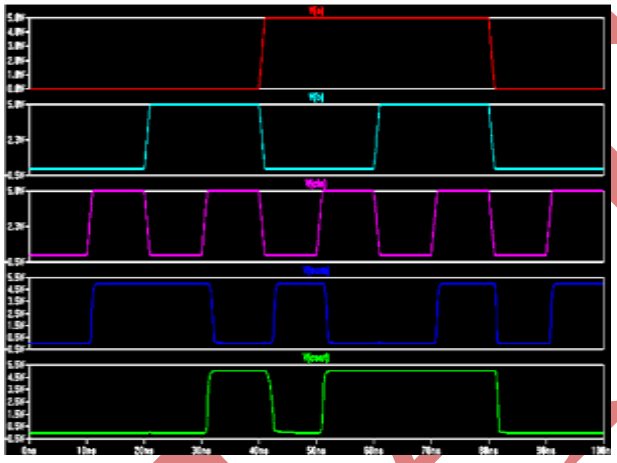

Fig.6. Conventional CMOS full adder Results

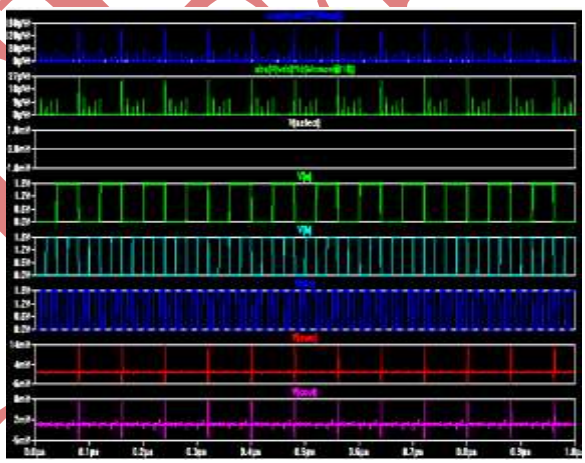

Fig.7. Design circuit 1 with sleep transistor logic 0

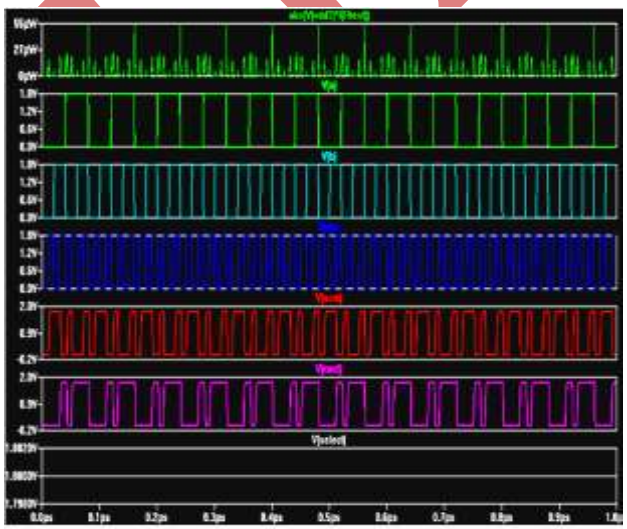

Fig.8. Design circuit 2 with sleep transistor logic 1

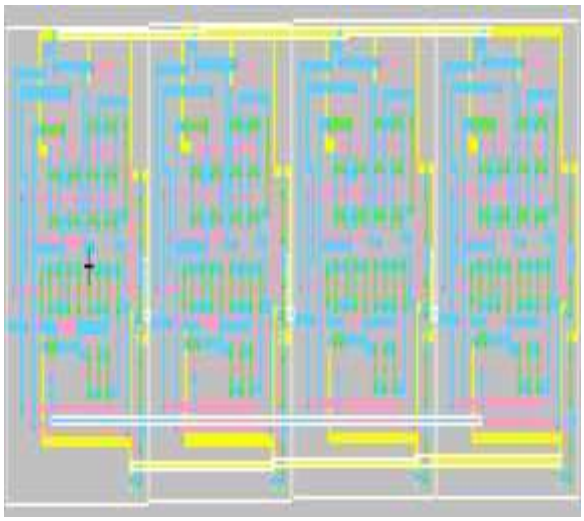

Fig.9. Layout of 4 bit ripple carry adder

VIII. CONCLUSION

In this paper, the analysis is performed on ground bounce noise and leakage power reduction for conventional and modified 1 bit proposed full adder circuits of design1 and design2 full adders with different sizing in 65nm technology. 4-bit Ripple carry adder is designed as application based on the 1-bit proposed design 2 full adder design and the adders are analyzed for active and standby power in 65nm technology. Standby power or leakage power of full adder design1 and full adder design2 is almost reduced than the conventional full adder design, respectively. Ground bounce noise is reduced by about 25% and 45% with adder design1 and adder Design2 respectively, compared to conventional design. By the use of power gating technique, especially the sleep transistor, and by transistor resizing, power dissipation and ground bounce noise is minimized.

REFERENCES

[1] S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006.

[2] Rabaey J. M., A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, A Design Perspective, 2nd Prentice Hall, Englewood Clifs, NJ, 2002.

[3] N.West. K.Eshragian, Principles of CMOS VLSI Design: A systems Perspective, Addison-wesley, 1993.

[4] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition, " in ICCD07, pp. 388-394, 2007.