CONSTRAINT RANDOM VERIFICATION OF NETWORK ROUTER FOR SYSTEM ON CHIP APPLICATION

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ABSTRACT

Multiprocessor system on chip is emerging as a new trend for System on chip design Router accept data packets to send the information in terms packet packet consist of data analog with IP adress SOC system on chip are two different types of system are integrated with single chip is known as SOC a new design methodologies.Network on Chip the integration of soc consist of better supports for custom network chip in there packet switched network. The design consist of registers FSM and FIFO the first bytes contains header which contains address &width of the packet the width of the packet can be a minimum of one and maximum of 63 bytes . the need of router whenever information transfer we have place this router borrowed from large scale multiprocessors and wide area network on chip routers based network. The packet forwarded to destination and interfaces through multichip routing path. In order to implement a competitive netwok on chip architecture, the router should be efficiently design the central component of NOC synchronization of input and output transper the information 3 fifos that are adding one are more fifo that act as five port router .Design and simulation of 5 Port Router was designed and its simulation was done with ModelSim6.5e and synthesis using Xilinx Ise

Keyword: FIFO, FSM, Network –On-Chip, Register Blocks, Simulation Router

I. INTRODUCTION

The routers exchange information about destination addresses using a dynamic routing protocol each router the router has interfaces for different physical types of network . The new methods that makes easy to functional verification this the recent years have been proposed the advance of process technology keeps on reducing device size several strategies with less effort. This goal is towards methodologies recent advancements thing about it is free one such methodology is best This is built on system Verilog and used effectively to achieve maintainability, reusability, speed of higher performance etc ASIC to the functional bugs, As the functional verification decides design the quality we spend response the design cycle time only for the verification And simulation In order to avoid the delay and meet we use the latest verification methodologies and technologies and accelerate the verification process.In this document the use of system Verilog to verify a reusable test bench is explained as step by step design and to develop The test different components and each component is again composed of subcomponents, This project helps one to understand

the complete functional verification process of complex ASICs an SOC'S and it gives opportunity to try the latest verification methodologies. programming of hardware verification languages and sophisticated EDAtools for the high quality verification,

1.2 Need of A Router

The bus based architecture creates communication bottleneck in terms on the giga bit communication various functional element are used in system on chip, that explicit modularity and parallelism custom network on chip was needed posses many such attractive property solve the problem of communication. Network on chip is carried out by means of router the communication so for implementing better. NOC efficient What defines a router is not its shape, color, size or manufacturer but its job function of routing data packets between computers A cable modem which routes data between PC and ISP can be considered a router broad band ICS router .will look a bit different depending on the manufacturer or brand but wired router a wired either net broad band router will typically have built in Ethernets switch to allow for expansion. these router also support network address translation which allows to allows all computer internet connection sharing the routers will also to provide users with much needed features such as an SPI firewall or serve as a DHSP server the output channel it is forwarded by other port which the input channel moves the data packet. it is forwarded to the output channel of other port. Decode logic which increases the each input and output channels the performance of which increase the router,

1.3 Back Ground of a Router

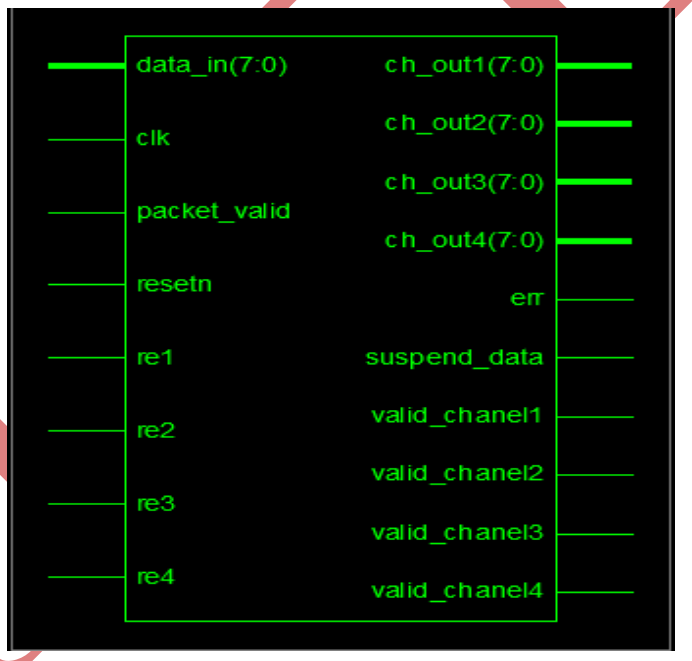
The router used here is it avoid congestion and communication bottleneck. Although there are number of router implementation has already been done. Some of the related works are included here.J.nurmi presented the implementation of router for NOC based system which has 2D torus network toplogy. Packet size was 8 bits and 2 control bits. The main drawback here was it was a 2D torus formed using 1D router which creates a serious bottleneck in traffic. B.s feero and .p.pande presented a soft core router for NOC; the problem with this router implementation was it uses 4 flit buffers having 8 bit implementation which is quite high. Its input and output channel has four distinct blocks and uses a large decoding logic. Morgan presented its work but the drawback with it was that its packet has two headers which are quite expensive. The buffer here is present only with input channel. The absence of output buffer creates a serious problem in the implementation of router. as it increases the problem of congestion. Our paper removes most of the problems cited above and improves the performance of router.

1.4 Application of Router

When multiple routers are used in interconnected networks, the routers exchange information about destination addresses, using a dynamic routing protocol. The preferred routes between any two systems Each router builds up a table listing on the interconnected networks. Different physical types of network connections, A router has interfaces for It is also contains firmware for different networking standards this specialized computer software to enable data packets to be forwarded from one protocol, each network interface uses transmission system to another. Logical groups of computer devices known as subnets router may also be used to connect two or more, each with a different sub-network address to The router do not necessarily map directly to the physical connections the subnet address,

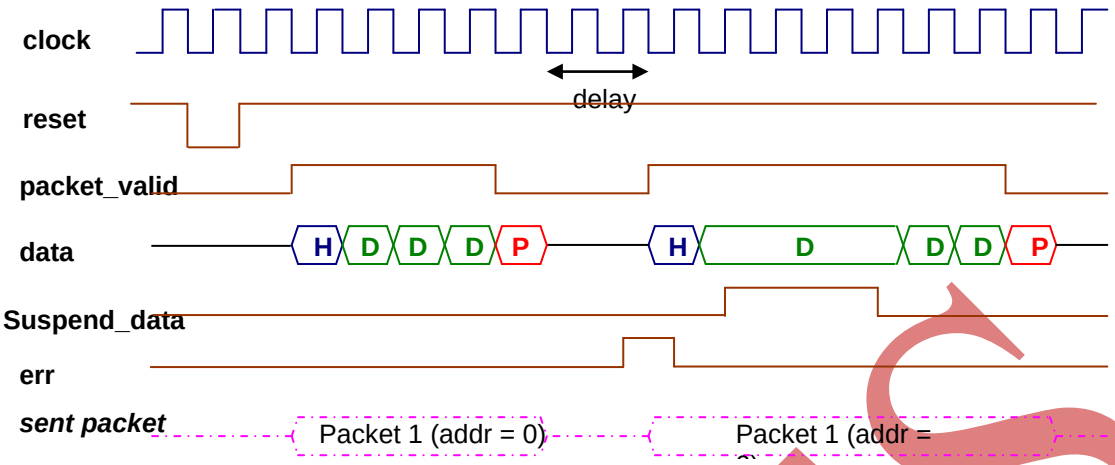
II. ROUTER DESIGN PRINCIPLES

Given the strict contest dead line and the short implementation window we adopted a set of design principles to spend the available time as efficiently as possible. This document provides specifications for the router is a packet based protocol. router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet. The router is a "Five Port Network Router" has one input port from the packet enters. It has four output ports, where the packet is driven out. Three parts packet contains they are data frame check header ,8 bits width of the packet and packet the length of the packet can be between 1 bytes to 64 bytes. Packet header contains three fields DA and length. Is the Destination address (DA) of the packet is of 8 bit. Port based on this address of The switch drives the packet to respectively of the packets. Port address 8-bit address port each output. If the destination address of the packet matches the port address, then switch drives the packet to the output port, bits and from measured length of bytes in terms Length is measured of bytes . in terms data should be can take anything the security check of the packet contains frame check sequence length is measured in terms of bytes data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calcuted over the header and data.



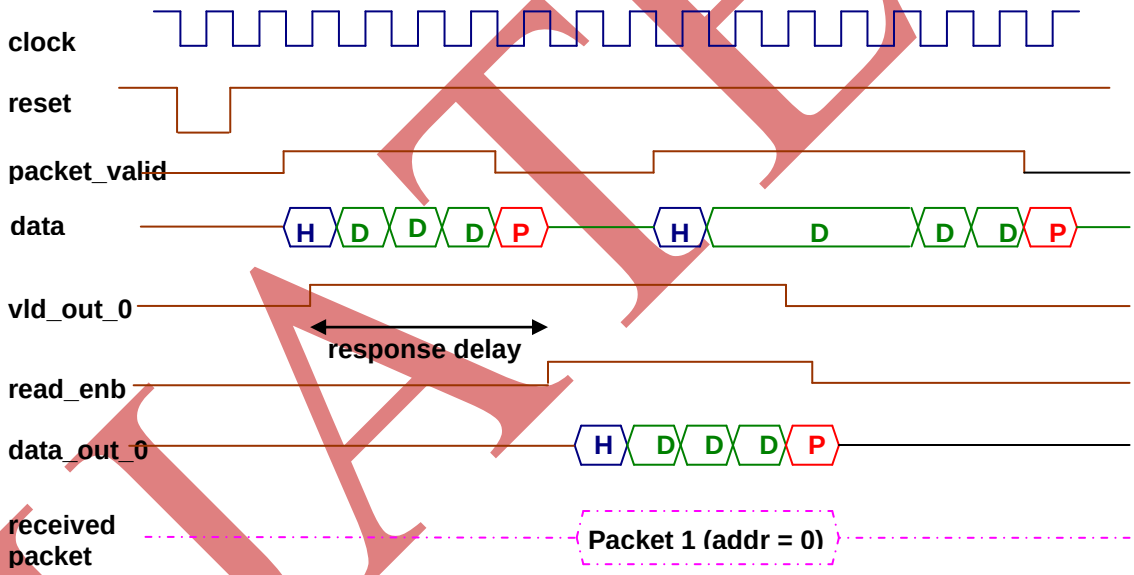
"Fig 1" Diagram of Five Port Router

All input signals are active high and synchronized to the falling edge of the clock. the packet valid signal is to be asserted on the same clock edge when the first byte is sent after the pay load byte is driven. the packet valid is made low Output signals are synchronized to the falling edge of the clock. the read enable signal is asserted at the falling edge of the clock when read enable signal is high the data flow when read enable signal is high the data flow happens at the next positive edge clock



H = **H**eader, D = **D**ata, P = **P**arity

"Fig2" Router Input Protocol

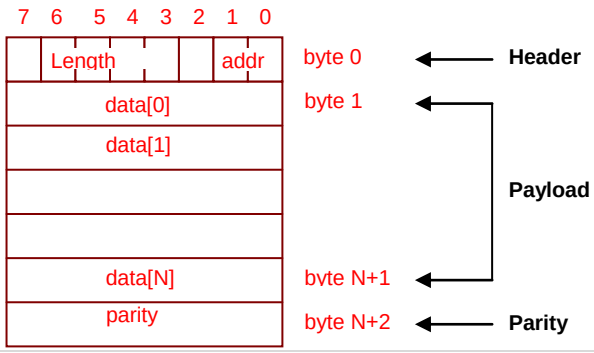


"Fig 3"Router Output Protocol

III. PACKET FORMAT

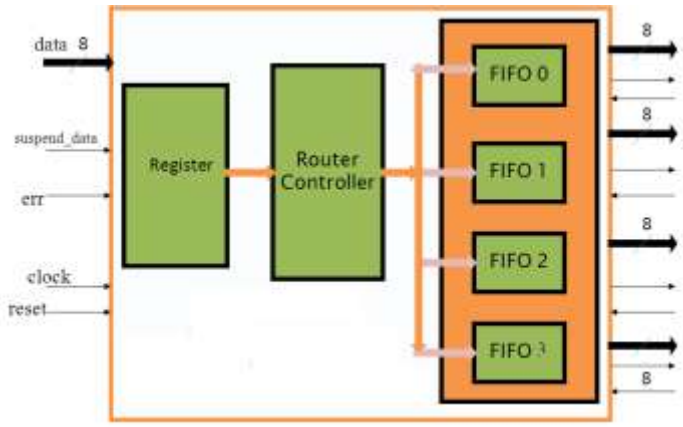
They are header, payload and packet parity contains there is a three parts are the packet format

Packet width is 8 bits and the length of the packet can be between 1 bytes to 63 bytes.



Router accepts data packets of one byte length on a single 8 bit port the first byte contains header which contains address &width of the packet the packets are routed to one of three channel.

IV. FIVE PORT ROUTER ARCHITECTURE



4.1Router Architecture

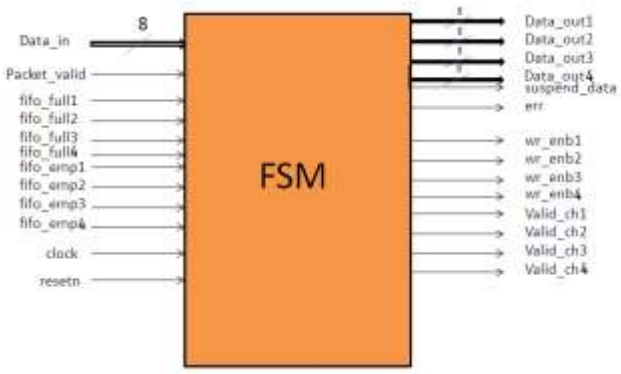
The Five ports Router Design is done by using of the three blocks .the blocks are 8-Bit Regiter, Router controller and output block. the router controller is design by using FSM design and the output block consists of four FIFO's combined together the FIFO's are store packet of data and when u want to data that time the data read from the FIFO's. In this router design has three outputs that is 8-Bit size and one 8bit data port it using to drive the data into router we are using the global clock and reset signals, and the err signal and suspended data signals are output's of the router .the FSM controller gives the err and suspended_data_in signals .this functions are discussed clearly in FSM description.

4.2 Register block

This module contains status, data and parity registers required by router. On rising edge of the clock all the registers in this latched are modules .The data from input based on state and status control signal latches the data register, and this latched data is sent to the FIFO for storage the parity registers for parity calculation apart from it data is also latched. And it is compared with the parity byte of the packet. If packet parity is not equal to the calcuted an error signal is generated.

4.3 Router Controller (FSM)

This module generates all the control signals when new packet is sent to the router. These control signals are used by other modules FIFOS input data is sent FSM controller along with packet valid signal. it decodes the address of the channel to which the data is to be sent checks the status of the FIFOs and loads the data to the respective one suspended the data if FIFO is full checks the parity match error signal if mismatch occur.



"Fig4" FSM Router Controller Block

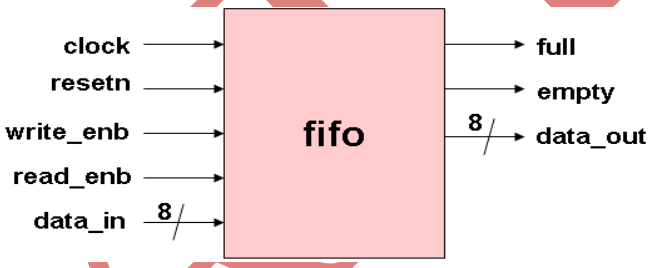
4.4 Router Output Block

There are four FIFOS used in the router design. 8-bit width and 16 bit depth of each FIFO

The works on FIFO system clock. It has synchronous input signal reset.

- Write Operation
- Read operation
- Read and Write Operation

The functionality of FIFO explain below



"Fig5" Five port router FIFO

Write operation

The FIFO write operation is done by when the data from input data is sampled when input wire enable is high and FIFO is not full at the rising edge of the clock .in this condition only with write operation of FIFO

Read Operation

The FIFO Read Operation is the data when read en is high at the rising edge of the clock data out read from output and FIFO is not empty FIFO. Simultaneously read and write operation. Full – it indicates that all the locations has been written inside the FIFO .FIFO Empty – it indicates that all the locations of the FIFO are empty.

V. EDA TOOLS AND METHODOLOGIES

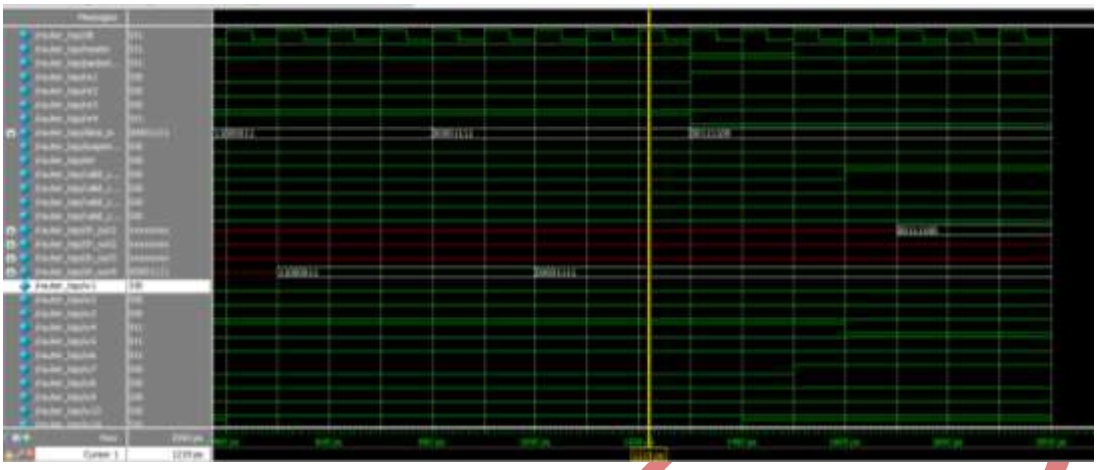
HDL; verilog

Verification methodology; constrained random coverage driven Assertion Based verification

EDA Tools; Modelsim- A verification platform Mentor graphics

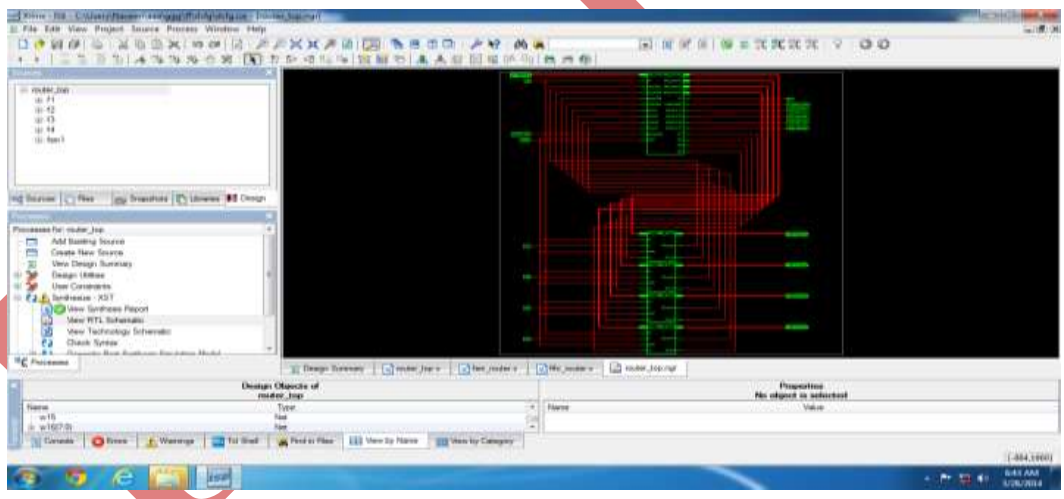
XILINX-synthesis

VI. SIMULATION RESULTS



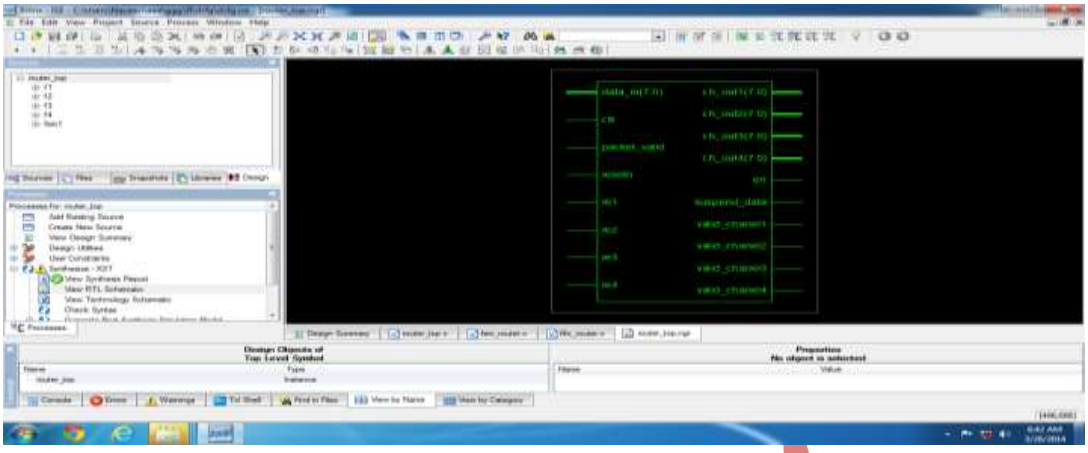
"Fig6" Simulation of Five Port Router

The simulation five port router are four readable channel and four writeable channel four output channel the data are sent to the packet validity condition must be one the data condition input data is sent to data in condition reset condition is enable output condition reset is enable condition some slaves are require the falling edge high to low transition condition read enable signal is required from the master for each slave device.



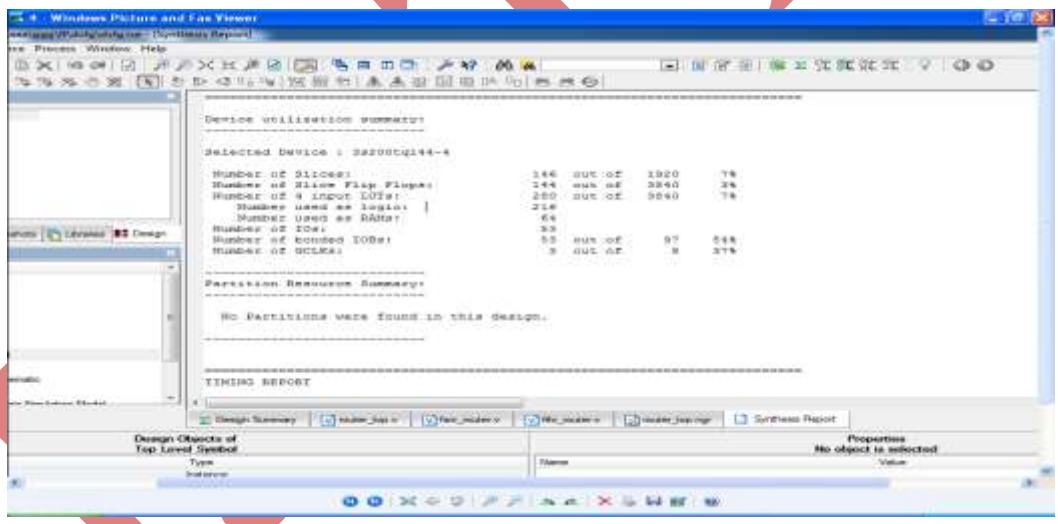
"**Fig7'' View RTL Schmatic Result**

The five port router RTL schematic result are used In four readable channel CLK packet valid channel data in 8 bits reset and packet valid channel error signal. the FIFO's are store packet of data in this state neither new data is accepted nor any data is latched. so Suspended signal is made high and write enable register signal is made low FIFO full state no new data is accepted so suspended data is kept high last data is latched FIFO full.



"Fig8" View Technology Schmatic

The view technology schematic result are used in four valid channel CLK , packet valid channel suspended channel and four readable channel data in 8 bit reset and packet valid channel error signal asserts when a packet with bad parity is detected in the router. the clock signals are active high and are synchronized to the falling edge of the clock. the signals can also be driven on the rising edge of the clock when valid channel data appears on the valid output bus this is a signal to the packet receiver that valid data is available on a particular data.



"Fig9" Device Utilization Summary

Device utilization summary are selected devices are number of slices are used and 146 and available slices are 1920 slices are utilization 7%number of slice flip-flops are used 144 and available flip flops are used 3840 flip flops are utilization 3% number of four input look up tables are used 280 available are 3840 are utilization of LUTS 7% number used logic s and RAMS are bonded IOBS 54%number of 33% GCLKS 37%ROUTERwas improved by reducing the usage of number of look up tables thus the constraint coverage of router we have to reduce design summary total frequency and memory.

VII. ADVANTAGES

1. Full duplex synchronous serial data
2. Variable length of transfer word up to 62 bytes
3. Header is the first data transfer
4. Both rising and falling edge of serial independently
5. Four receiver select lines
6. Fully static synchronous design with one clock domain

VIII. CONCLUSION

In this paper we proposed a 5 Port router design for effective data transfer IST simulation and synthesis was done using the verilog coding with the latest design methodology verilog and system verilog and observed the code coverage and functional coverage of router by using cover point cross and different test case improved functional coverage of router used in one master and the four slaves to monitor the router thus constraints coverage of router was improved by reducing the usage of number of look up tables.

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