DESIGN OF A LOW POWER MICRO UART DESIGN WITH ASYNCHRONUS DATA TRANFER FOR DATA ACQUISITION RELEVANCES

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ABSTRACT

In this paper presenting a low power UART which was developed by using clock gated scheme and asynchronous techniques. UART is communication protocol which establishes communication between the periperals to the remote embedded systems. UART will operate based on the fixed frequencies with sampling the data. Clock gated UART will consume considerable amount of power , asynchronous UART will consume small portion of power consumed by the clock gated UART. We have developed UART using Verilog hardware description language. This design is synthesised in Xilinx ISE 13.2.

Key Words: Asynchronous UART, Synchronous And Clock Gated UART.

I. INTRODUCTION

Universal asynchronous receiver and transmitter refferd to as UART. It is a communication protocol which will make conversion from the parallel tream of data to serial stream of data over a communication link.This protocol reveals that communication will occur at predefined frequency. The devices on the communication link will generate its own frequencies independently. Any new events may occur asynchronously with the local clock. This needs that an input data stream has to be sampled even though the devices on link has slight difference in the frequency from the predefined frequency. Sampling can be achieved by having local clock signal which is having frequency greater than the chanel sampling rate.UART is a communication protocol uauallu used for the communication with slow peripherals. This design includes that full duplex asynchronous serial communication system used mostly to realize general serial bus protocols like RS485. RS 232, and RS422. The synchronous design is built from the this clocked design by making control modification to the clocked data path.

This work provides whether the simple clocked UART hardware protocol can be advantageously implemented using asynchronous design techniques. Power reduction is the aimed advantage because performance reveald by the protocol. By providing clocked design , the receiver has to contigeously sample the serial input line at high frequency internal clockto identify start of new transmission. The asynchronous design does not need to sample the incoming serial input line, instead it will reactively respond to the arrival of new transmission intiation.this was the basis for the expected advantage study. The second section deals with the existing synchronous clocked design. Section iii deals with the design of asynchronous design of UART

II. LITERATURE REVIEW

In this sectionwe will see how the synchronus design of UART is changed to asynchronus UART here we discuss about synchronus UART .

2.1 Relative Timing

Tining is the basic difference in both clocked and asynchronous designs. The impact of time on a system is to arrange and sequence orders. In this paperwe have taken real time methodology into consideration to represent the sequencing that timing imposes on circuits. A this timing methodology comprises of common timing reference and apair of events that are prprorely orderd in time for exact circuit operation. we refer that common reference point as point of divergence POD, orderd events called point of convergent poc.

2.2 Asynchronus Design Flow

The asynchronous design flow is similar to that of vlsi design flow. It starts with the specification , which is synthesised by the hand or asynchronous tools. The result of synthesis is circuit description which represents a gate level. So that circuit description has to be mapped to the gates of standard cell library. For proper operation of a device we may add an extra signal calle reset.

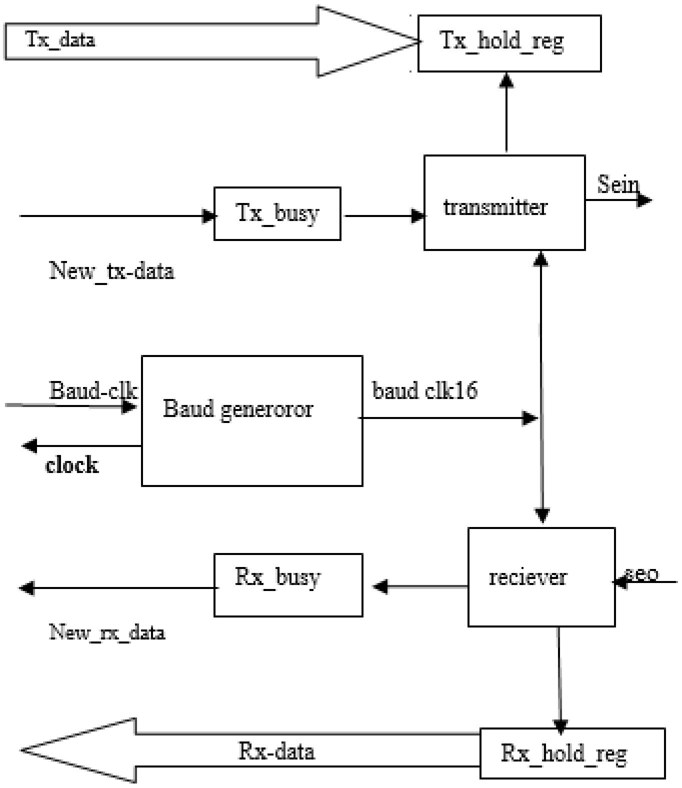


Figure 2.1 Synchronous UART

2.3 Synchronus UART Implementation

This design consist of 3 main blocks are ransmitter, receiver, baud rate generator and 3 status registers tx_busy, rx_busy. The baud generator generate baud signals from the input stream to the transmitter and receiver. The transmitter and receiver which performs data transmission between them independently. This allows them to work in full duplex communication.

2.3.1 Baud Generator

Baud generator generate baud pulses with 16* to the baud rate specified by the communication link to the transmitter and receiver to generate their internal baud pulses. The faster the baud rate receiver to align sampling pulse and faster response. Baud generator having baud rate, baud limited are desined as follows

2.3.2 Transmitterblock

Transmitter is used to transmit the data. In this incoming data intiated by the signal new_tx_data. This signal indicates that parallel data is available on the new_data signal. This data is stored in the register tx_hold_reg during next clock cycle. The parallel data is converted to serial by using shift operations. The starting of shift operation sets the status register transmitter busy. The transmitter busy indicates that intiation new transmitter signal. The tx_busy signal will also indicates that valid data signal for the transmitter block. The shift operation allows at the baud clock frequency to transmitter data on ser_out data line. The 16 bit counter is used for generating rising edge of the baud clock signal which is generated by the 16* baud clock generator. The status registers are used to maintain status of the data transfer and to indicate valid /invalid data signals by interrupt signals.to rest the tx_busy signal we use a 10 bit counter which indicates the number of bits being transmitted.

2.3.3 Reciever Block

The receiver block which performs reverse operation like seial data to be converted into parallell. UART having communication format one start bit followed by 8 bits and one more stop bit. Start bit used to indicate arrival of new data and stop bit indicates that end of the format. Whenever start bit is recognised rec_busy signal is set. This recievr block operates at two edges of the clock generated by the 16* baud clock generator. Sampling and shifting of the shift register occur at the middle of the incoming data at the falling edge of the clock which was generated by the count of 8 from counter. Whenever this block receives end bit of the ser_in data it stores the recievd signal in rec_hold _data register at the rising edge of the clock which was generated count of16 from counter. A counter of 3 bit is used to monitor the number of bits received.

III. PROPOSED ASYNCHRONOUS UART DESIGN

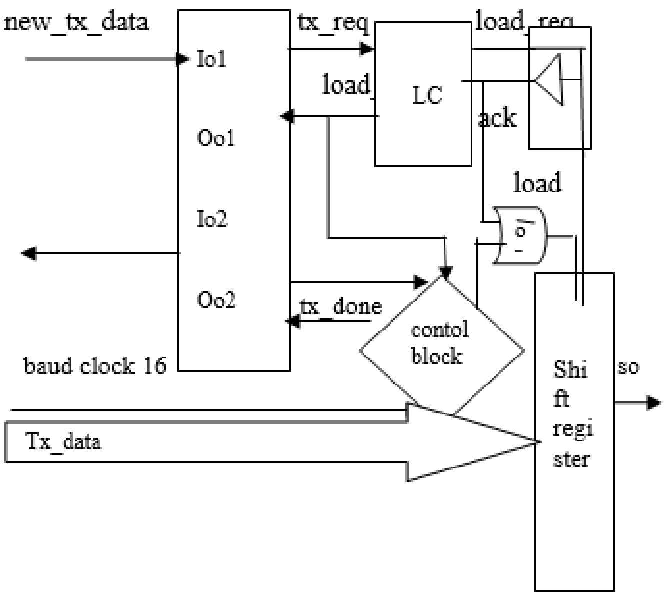


Figure 3.1 Asynchronous UART Transmitter

Asynchronus design of UART adds additional advantage over the synchronous design. Asynchronous design adds handshake signals to the UART which enables and steers the local clock. In the asynchronous design data path design is similar to the clocked design. Because of that asynchronous design is larger than clocked design. This design power benefit derives from substsnstial idle times of communication format and reactive nature of the design. This implementation LC controller is as shown in below figure. The aim of the controller is generate timing reference to determine frequency of operations. Second is to produce high power clock to drive latches and flip flops in the data path , ther by freeing of its design. There are teo separate control protocols were proposed for eac transmitter and receiver.we will see the operation of each block individually as follows

3.1 Baud generator

The baud generator generates specified baud frequency. This is similar to that baud generator is synchronous design. The UART needs the baud generator since data to be transmitted and received at specified single frequency. The baud generator is active only during data transfer in become inactive in idle stages. This inactive is done by gating the global clock signals at an input based on presented handshake signal network.

3.2 Transmitter Block

It is similar to the synchronous design having shift register but Clock control network is replaced by the hand shake circuitary. The hand shake circuitary consist of a generic fork element, LC circuit, and control block. the new incoming data signal is intiated by the new_tx_data signal to be set. The fork broad casts incoming signal from the sender to the two out going channels. The acknowledge signals associated with these two requests are synchronised with C-element bfrore passing it as tx_done_ack. The c- element output changes only when both inputs are identical . the upper chanel goes to LC block which generates clock signal to load the parallel tx_data in the shift register, this is controlled by the load_req signal. The load_req signal also determines the mode of operations of the shift register. The load_ack signal indicates latching of data. The separation between the loading the parallel data and shifting on the ser-out chanel is achieved making load_ack signal the enabling the signal along with the start_req for the control block. this ensures thw generation and supply of baud clockto shift register is preceded by the loading operation. The OR gate allows the shift register to be clocked either by the baud clock or asynchronous handshake request but it shifts data only when the load signal is set low.

When load_ack signal was asserted new data will be shifted after 16 naud clock _16 ticks. The need to maintain number of bits transmitted is accomplished by the 4 bit counter clocked by the baud clock rate. The tranmisssion having 8 bits with one stat bit and one stop bit is equal to 10 bits. The tx_done signal generated by the count of 10 for indicating that ending of the transmission.The tx-done signal makes tx_done_ack will be generated sothat active part of handshake signal will be completed. The resetting of handshake will results in resetting the counters in the control block.

3.2 Reciever Block

whenever a new data is arrived at the receiver it was indicated by identifying the start bit set. This enables new communication in UART. The reset of rx_done is low and ser_in signal low indicating that control block c-eelement and counter will be enabled to store in coming data signal at the shift register. The another counter is used to count number of bits to be transmitted. Those counter wiil be reset after the completion of 10 bits reception. The rx_done signal indicates that completion of reception. This resets the c- element output so that completeing the four cycle hand shke. The clock signal for the hold register is generated generated at the end of handshake cycle, converting the serial stream to parallel 8bit data. Reception of new data is indicated by the new_rx_data signal

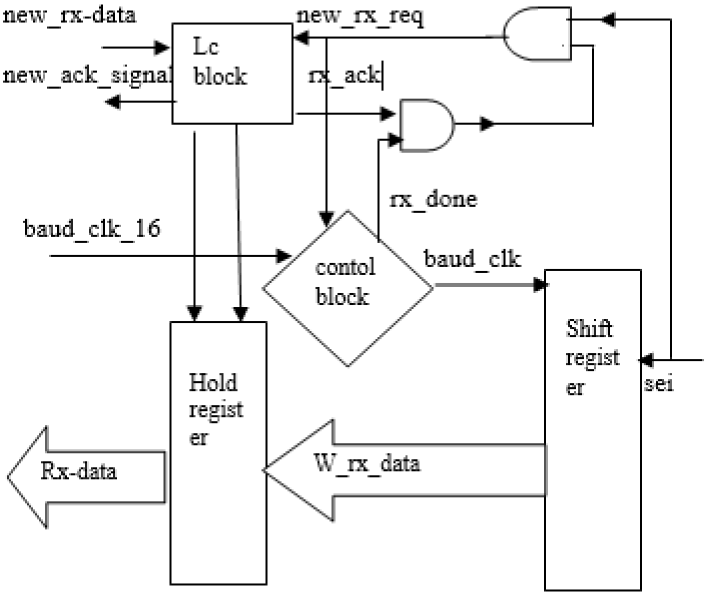
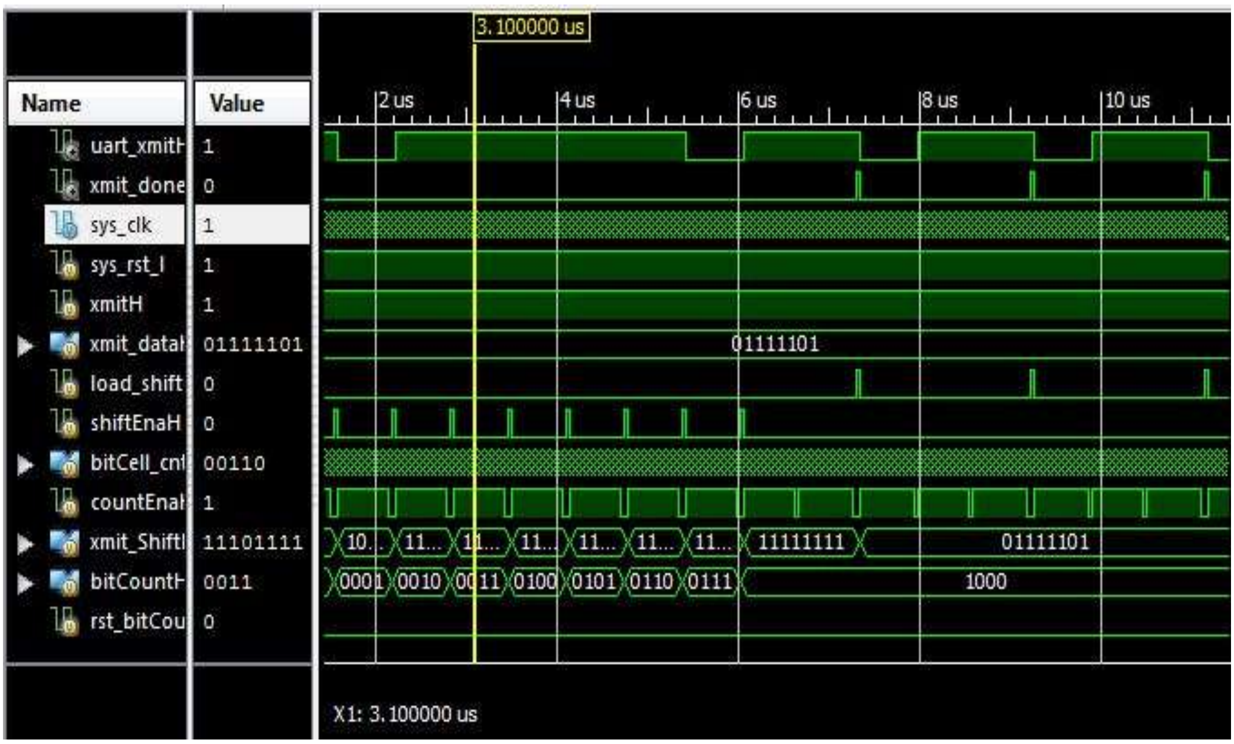


Figure 3.2 Asynchronous UART Transmitter

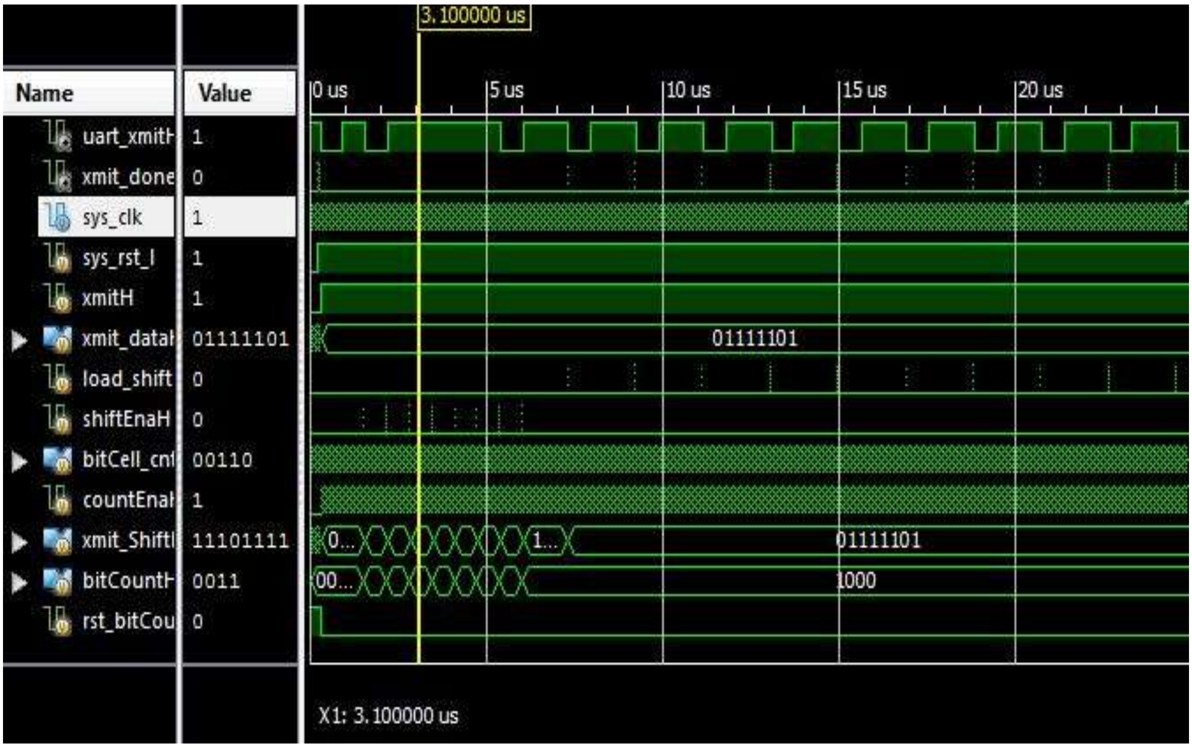
IV.SIMULATION RESULTS

In this paper we are presenting asunchronous UART which is designed using Verilog. This is synthesised in Xilinx ISE 13.2 i. Synthesised reports are shown below

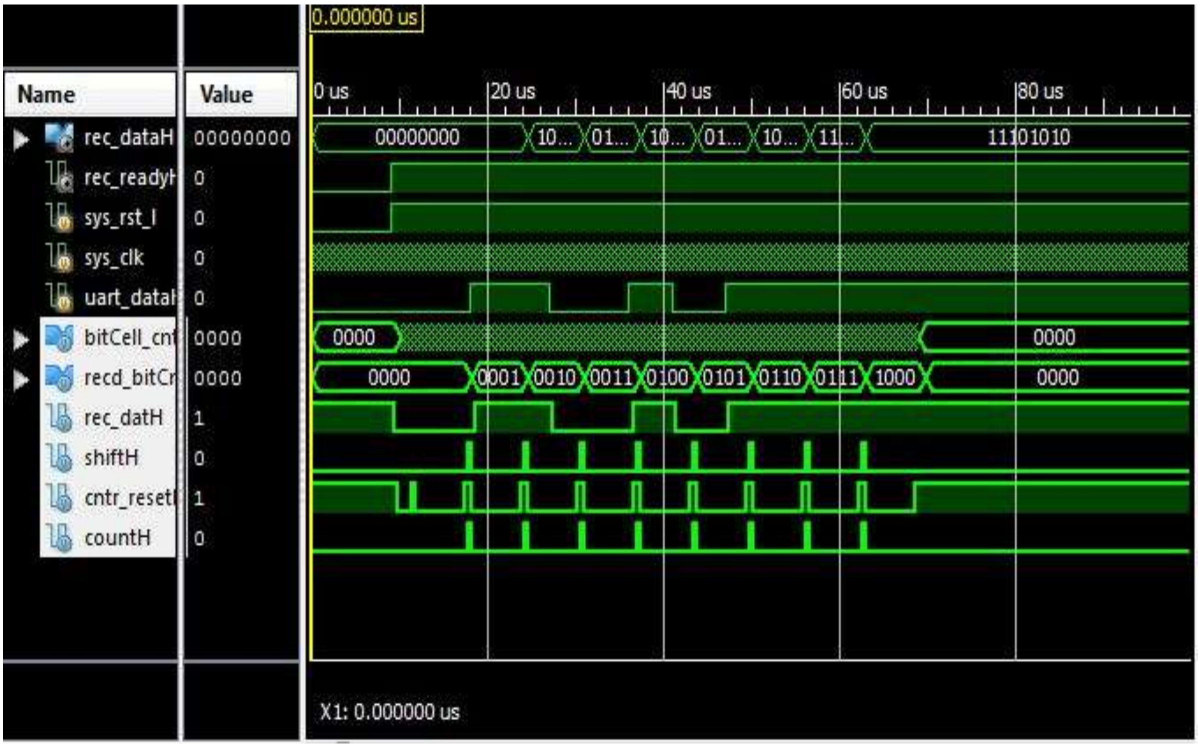
4.1Transmitter



Name	Value
uart_xmitH	1
xmit_done	0
sys_clk	1
sys_rst_l	1
xmitH	1
xmit_datal	01111101
load_shift	0
shiftEnaH	0
bitCell_cnt	00110
countEnal	1
xmit_ShiftI	11101111
bitCountH	0011
rst_bitCou	0



4.2 Receiver



V.CONCLUSION

In this paper we are presenting a novel design of UART. This UART as designed using asynchronous and clocked. We made small modifications to the control block in synchronous design to take advantage of asynchronous designs. The asynchronous which is having reactive nature to respond the intiation new transmission or reception. Due to reactive nature it does not required to sample continusly the incoming data. This asyncronus UART was designed using Verilog HDL. This design is synthesised in Xilinx ISE 13.2 i. the synthesis reports will give us that better performance.

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