VERTICAL SILICON NANOWIRE GATE-ALL-AROUND TUNNELING FIELD EFFECT TRANSISTOR WITH LOW THRESHOLD SWING

Md. Riyaj[1], Nazia Abdullah[2], Pooja Sharma[3]

[1]Assistant Professor, [2]B.tech Scholar, [3]Assistant Professor
SBCET Jaipur, (India)

ABSTRACT

In this work, we report a high performance Field-effect transistor on vertical Nanowire with silicon drain source contacts and scaled metallic gate length, which is fabricated by simple process. Silicon Nanowire (SNWs) is the best on tunneling field effect transistor (TFET). Which is uses a CMOS vertical gate all around and compatible in nature. When the temperature reduces then the segregated silicon oxidation for the sources occurs. The threshold is calculated on room temperature when examine three of drain current, and then there would be an excellent characteristics is being show by field effect transistor (FET) without as bipolar behavior and with high I_{on} /Io_{ff} ratio. Moreover, an SS of 50 mV/decade is maintained for three orders of drain current. This demonstration completes the complementary pair of TFET (Tunneling field-effect transistors) to implement CMOS- like circuits.

***Keywords*: Vertical Silicon Nanowire (SiNWs), Gate-all-around (GAA), Tunneling field effect transistor (TEFT), sub-threshold swing (SS), top-down**

I INTRODUCTION

We know that our several years the performance of metal oxide semiconductor Field effect transistor (MOSFET) has been degraded due to the excessive scaling Process. CMOS technology is the driving for the increasing integrated circuit (IC) chip speed and functionality. Nanowire replaced electronic equipment in almost all application because of its much advantage that is smaller in size, light in weight longer life, high efficiency, more mechanical strength and smaller power consumption. The sub threshold is carried out by the one of the most important characteristics and denoted by ‘sub-threshold’ .The sub threshold is defined as the change in gate voltage is required for a change of an order of magnitude of current from OFF to ON state.
Thermionic emission–carrier diffusion process plays a vital role to carry out the ‘SS’ of MOSFET. When we increase the current in OFF state then we can prepare to
Find the scaling down of MOSFET supply voltage. Semiconductor Nanowires can be prepared in High-yield with reproducible electronic properties as required for large-scale integrated systems and compared with “top–down” nanofabricated device structures, “bottom–up” synthesized Nanowire materials offer well controlled size in at least one critical device dimension, channel width that is at or beyond the limits of lithography.

In silicon Nanowire FET that is generated by pattern on the SOI wafer coated with light sensitive liquid and removes the material from wafer surface is used etching process.

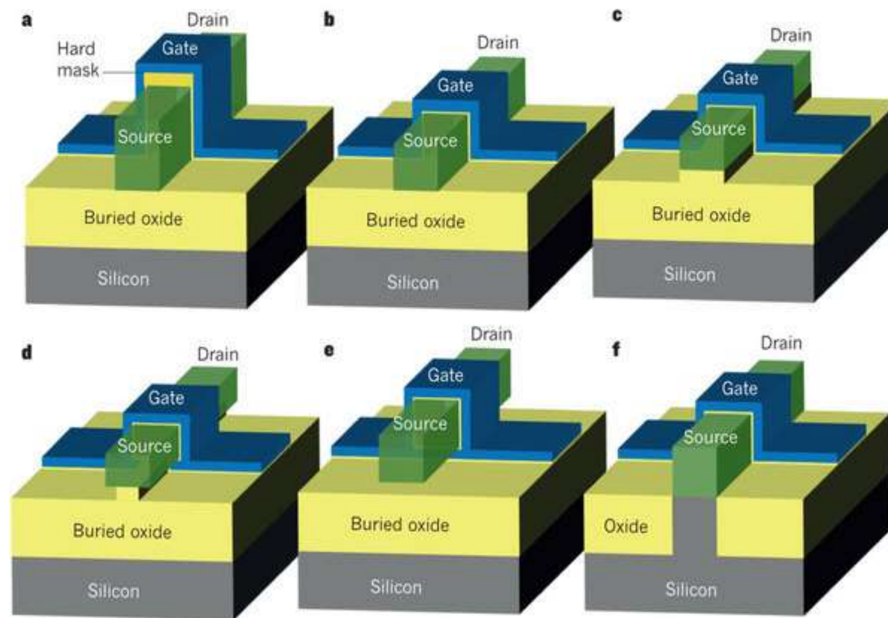

Fig 1: Vertical Silicon nanowire TFET process flow schematic. (a) Vertical pillar etch and As implantation to form the drain region, (b) isolation oxide deposition and gate stack formation, (c) the top amorphous-Si etched to expose source side of TFET, (d) source implanted with BF2, (e) dopant segregated Ni silicidation, (f) contact opening and Al metallization.

This is the promising constraints for various applications because TEFT can provide low OFF linkage and the 'sub-threshold swing' (SS) below the 60mv/molecules.

Tunneling through barrier is the process by which the carrier transport takes place in TEFT.

The vertical gate All-Around (GAA) Nanowire transistor (NWs) will be more valuable in the future because it's

i. Excellent to gate channel coupling.
ii. High integration for circuit functionality.
iii. And the compatibility with the existing CMOS.

II PURPOSED GAA NANOWIRE

GAA Nanowire will increase on the chip device density and show the good gate controllability process of integration of TEFT. The GAA Nanowire based devices to for SONOS type of memory applications, that's gate dielectrics has to be necessarily thicker.

Fig 2: Progration of device structure from conventional single gate planner device to GAA structure

III DEVICE FABRICATION

Top-down CMOS technology is the introduced for the fabrication of N-channel gate all-around (GAA) Si-Nanowire based TEFT, TEFT device used for ultra low power and energy efficient applications.

These are the graphs which are the plotted by hard mask of silicon nitride (SiN) using deep RIE to form vertical SiNWs. Thermal oxidation is controlled at 1000c for half an hour by using BF2 (10^{15} cm$-^{2}$/10 keV) and activated at 1000^0C for 5 second.

The gate is vertically positioned. In this processing this loss to pay attention that only tip of the Nanowire should be exposed. The isolation of HDP oxide takes place and again it gate deposited over there.

There are two steps of Ni-deposition (sputtering).

i. Rapid thermal annealing at 220^0c for 30 sec.
ii. 440^0c/30s in N_2 ambient condition.

There is dying of 1500nm and a fabricated TEFT device along with the gate length 170nm.

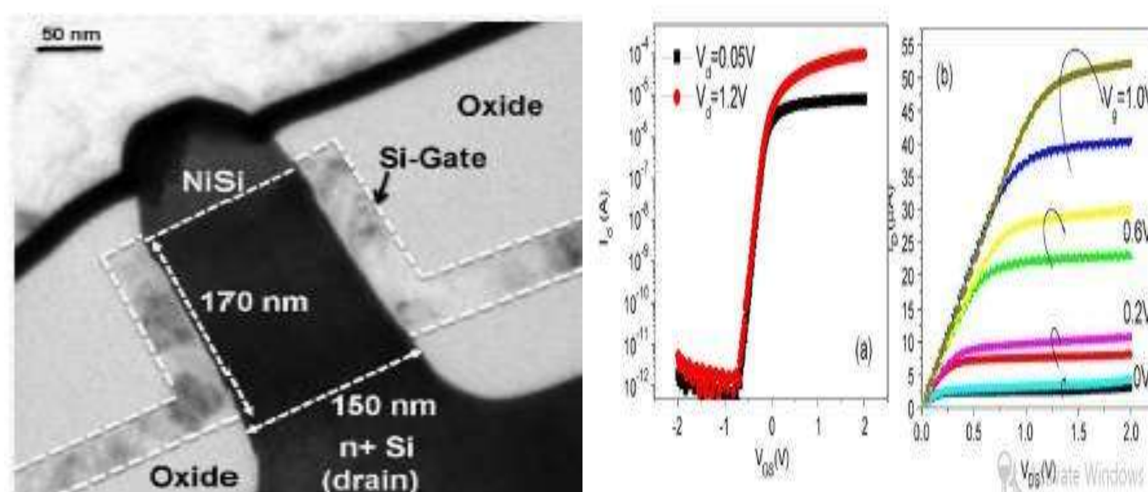

Fig 3 (a):- Cross-sectional TEM image of a vertical SiNW TFET device with a Diameter of 150 nm and a gate length of 170 nm(b) ***Id–Vg*** **characteristic of a vertical SiNW TFET with a low SS of 30 mV/ decade.**

CMOS device scaling, which has continued for more than the last four decades is facing severe as a result of excessive increase in power consumption caused by increasing OFF-State leakage and non scalability of the operating voltage (Vdd). Vdd scaling requires simultaneous scaling of threshold voltage for maintaining a certain ON-to-OFF ratio of the device currents, which however leads to a substantial increase in the sub-threshold leakage (OFF state) current, owing to the non scalability of the sub-threshold swing (SS) of MOSFETs. The Sub-threshold in MOSFET is governed by thermal diffusion of carriers over a potential barrier and has theoretical lower limit 60mV/decades at room temperature. Tunneling field-effect transistors (TFETs) employ a fundamentally different injection mechanism in the form of band-to-band.

Sub-threshold swing in tunnel FET is given by

$$SS= [d \log I_D]^{-1}/dv_{GS} \, [mV/decade]$$

And room temperature is given by

$$SS_{MOSFET}= \ln (10)\, KT/q[mV/decade]$$

Sub-threshold swing is band to band tunneling current process.

And Tunneling is given by

$$I = xV_{eff}\, \varepsilon \exp(-y/\varepsilon)$$

Where,

$X=Bq^3\sqrt{2m^*Eg}/4\prod^2h^2$

$y=4\sqrt{m^*Eg^{3/2}}$

V_{eff} -bias tunneling TEFT

ε- Electric field

Final resultant will be given

$$SS_{TFET} = \ln [1/vr*dvr/d_{vgs}+\varepsilon+b/ \varepsilon^2*d\, \varepsilon/d_{vgs}]^{-1}$$

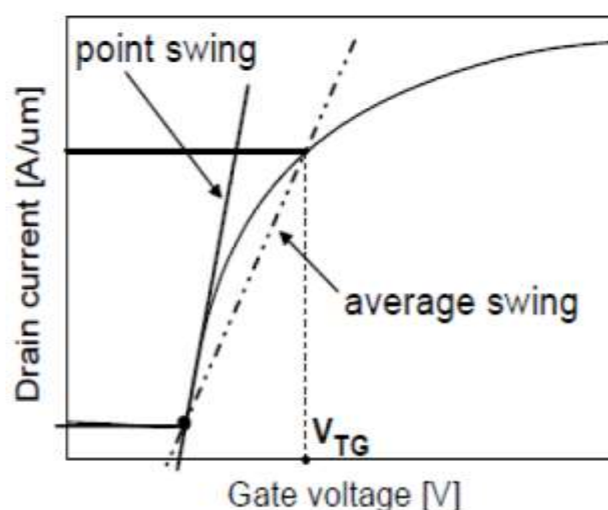

Fig 4: Point Swing and Average Swing of the I_d V_g Curve

IV RESULTS AND DISCUSSION

a. TEFT shows following characteristics are a gated p+i-n+ diode which words under reveres bias in OFF state. And in the ON state, gate voltage pulls down the energy band of the channel region and reduces the width of the tunneling barrier.
b. There are large potential barrier in between the source and channel.
c. The energy band in channel region diminished by the gate voltage in the ON-state.
d. Shows the input transfer condition if a silicon NW TFET with small dimension and the gate length of 170nm.
e. In the ON state the voltage also reduces the width of the tunneling barrier.
f. Retains the sub-threshold swing (SS) value is of 30mv/decade.
g. 70mv is achieved as a result of excellent gate control by gate all-around (GAA).

V CONCLUSION

In concise, there are few records which have been depicted when we demonstrated a SiNWs Based p-type TEFT device that is a record of low sub-threshold swing with 30mv/decade at a room temperature, when applied the voltage in low quantity.

The I_{on}/I_{off} has been achieved almost by three decade change in drain current and an Ion/Ioff ratio of >10^5. In addition, a sub-50- mV/decades value was observed for three orders of drain current. This work substantiates TFET in vertical GAA Nanowire architecture as a potential candidate for future energy-efficient electronics. Moreover, by using other known designs like hetero structure-based TFETs with smaller band gap material at the tunneling interface[6] as well as high-k gate dielectrics [6],[8].one can achieve further enhancement in ON current. Vertical SiNW-GAA structures also provide excellent gate electrostatic control, high integration density for circuit functionality and compatibility with existing CMOS technology.

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