ENHANCING POWER QUALITY WITH IMPROVED DYNAMIC VOLTAGE RESTORER BASED THREE PHASE FOUR WIRE SYSTEM

S.M.Rahaman[1], T.Rupesh Reddy[2], M.Venkateswara Reddy[3]

[1]*PG Student, Department of EEE, Vikas Group of Institutions, Nunna, Vijayawada, AP, (India)*

[2, 3]*Assistant Professor, Dept. of EEE, Vikas Group of Institutions, Nunna, Vijayawada, AP, (India)*

ABSTRACT

This paper deals with a evaluates an auxiliary control strategy for downstream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR) 3-leg VSC (Voltage Source Converter) with a zigzag transformer as a DVR (Dynamic Voltage Restorer) for load compensation in 3-phase 4-wire distribution system using ISCT (Instantaneous Symmetrical Component Theory) based control algorithm which is modified for the voltage regulation and used with indirect current control technique. The DVR is controlled to compensate the reactive power, harmonics currents, the neutral current and balance the unbalanced loads in the distribution system. Simulations are performed for the various load conditions such as the conventional control scheme: 1) can limit the fault current to less than the nominal load current and restore the point of common coupling voltage within 10 ms; 2) can interrupt the fault current in less than two cycles. 3) limits the dc-link voltage rise and, thus, has no restrictions on the duration of fault current interruption; 4) performs satisfactorily even under arcing fault conditions; and 5) can interrupt the fault current under low dc-link voltage conditions. A reactive linear load, an unbalanced load and a non-linear load in PFC (Power Factor Correction) as well as in ZVR (Zero Voltage Regulation) modes in MATLAB environment using SIMULINK and SIMPOWERSYSTEM TOOLBOX.

Index: DVR, ISCT, ZVR, PFC, PCC,

I. INTRODUCTION

Presently, the power quality is a big issue at the load end in the distribution system. As the majority of loads in the power distribution system are linear/ nonlinear and balanced/ unbalanced or combination in nature such as adjustable speed drives in fans and pumps, variable frequency drives and power converters with poor power factor used in industries as well as in home appliances. These loads increase the burden on the system by drawing reactive power and injecting harmonics which influence the performance of other loads connected to the same utility end. Moreover, unbalanced loads cause unbalanced voltages at the utility end. The DVR (Dynamic Voltage Restorer) is used to mitigate such power quality problems at the point of common coupling (PCC).

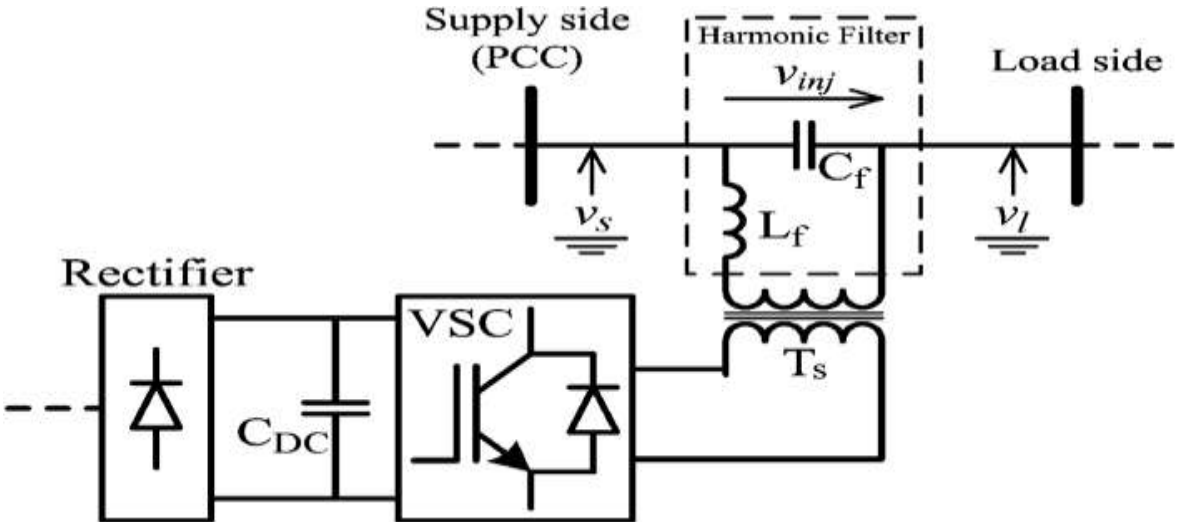

Fig. 1. Schematic Diagram of A DVR with A Line-Side Harmonic Filter

A three phase four wire DVR is used to compensate the neutral current along with voltage regulation or power factor correction with harmonics elimination and load balancing. The zigzag transformer is used to compensate the load neutral current by providing a path for zero sequence current. Moreover, the application of a zigzag transformer with the active compensation techniques has less complexity. The performance of the conventional control scheme is evaluated through various simulation studies The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltage conditions. In this paper, modified ISCT (Instantaneous Symmetrical Components Theory) based control algorithm is used to control the DVR in voltage regulation without a major change in the program and hardware of controller. As the supply currents are slow varying currents, the modified control algorithm is implemented with indirect current control scheme to control the current of the DVR. A 3-leg VSC with a zigzag transformer as DVR is implemented with modified ISCT using DSPACE DSP (Digital Signal Processor). The DVR with the proposed modified algorithm is found capable to compensate the load harmonics currents and load balancing along with PFC (Power Factor Correction) or ZVR (Zero Voltage Regulation). The dynamic as well as steady state performance of DVR is studied for both PFC as well as ZVR modes in a 3-phase 4-wire distribution system.

II. CONTROL ALGORITHM

The block diagram of modified control algorithm is shown in Fig. 2. PCC voltages (*va,*, *vb* and *vc*), supply currents (*isa*, *isb* and *isc*), load currents (*iLa*, *iLb* and *iLc*) and DC bus voltage (Vdc) of the DVR are sensed as feedback signals to extract reference supply currents. The control algorithm is based on primary objective to obtain the balanced supply currents. For that, the positive sequence quantities of the voltages and currents are considered like in conventional ISCT (Arindam Ghosh, 2000). Therefore reference supply currents are considered as:

$$Isa + Isb + Isc = 0 \qquad (1)$$

From the power factor consideration, the phase angle between *vsa* and *isa* is ø then:

$$\angle\{v_a + av_b + a^2v_c\} = \angle\{i_{sa}^* + ai_{sb}^* + a^2i_{sc}^*\} - \phi \quad (2a)$$

$$\tan^{-1}\{K_1/K_2\} = \tan^{-1}\{K_3/K_4\} - \phi \quad (2b)$$

where

$$K_1 = \sqrt{3/2}(v_b - v_c)\,;\; K_2 = (3/2)v_a\,;$$

$$K_3 = \sqrt{3/2}(i_{sb}^* - i_{sc}^*)\,;\; K_2 = i_{sa}^* - i_{sb}^*/2 - i_{sc}^*/2$$

Defining $\beta = \tan\varphi/\sqrt{3}$

After solving eqns. (2a, 2b and 2c), it results in:

$$(v_b - v_c + \beta v_a)i_{sa}^* + (v_c - v_a + \beta v_b)i_{sb}^* + (v_a - v_b + \beta v_c)i_{sc}^* = 0 \quad (3)$$

For β=0, the supply currents are to be in phase of PCC voltages. It implies that the reactive power demand of the load is supplied by the DVR. For nonzero value of β, the source supplies/absorbs the reactive power corresponding to the β. Therefore, in this paper β is used to regulate the voltage at PCC. The objective of the compensator is that the source must supply the load active power and the losses of the DVR in

PFC mode:

$$v_a i_{sa}^* + v_b i_{sb}^* + v_c i_{sc}^* = p_{lavg} + p_{loss} \quad (4)$$

where p avg *is* filtered average load active power using the moving average filter. The active load power is calculated by a moving average filter with averaging time of half cycle of the supply frequency.

$$p_{loss} = K_{pd}V_{dce} + K_{id}\int V_{dce}dt \quad (5)$$

P loss is the loss of the DVR which should be supplied from the AC mains for the self supporting DC bus and is estimated by the PI controller over the DC bus voltage as:

$$\beta = K_{pa}V_e + K_{ia}\int V_e dt \quad (6)$$

where * *Vdce* □*Vdc* □*Vdc* = error in DC bus voltage. *Vdc** and *Vdc* are the reference voltage and actual voltage of DC bus of DVR respectively. *Kpd* and *Kid* are the proportional and integral gain of the PI controller over the DC bus voltage of DVR. For voltage regulation, there might be phase difference (β) between the PCC voltages and supply currents corresponding to the required leading/ lagging supply currents to regulate the PCC voltage. Therefore, to regulate the voltage at PCC, this β can be estimated by using a PI controller over the amplitude of PCC

voltage as *Ve* =*Vt* □-*Vt* = error in PCC voltage. *Vt** and *Vt* are the reference voltage and actual voltage of PCC respectively. *Kpa* and *Kia* are the proportional and integral gain of the PI controller over the PCC voltage.

The amplitude of PCC voltage can be calculated as:

$$V_t = \sqrt{(2/3)(v_a^2 + v_b^2 + v_c^2)} \quad (7)$$

After solving eqns. (1),(3) and (4) the reference supply currents can be obtained as:

$$\begin{aligned} i_{sa}^{*} &= \{v_a - (v_b - v_c)\beta\}(p_{long} + p_{loss})/A; \\ i_{sb}^{*} &= \{v_b - (v_c - v_a)\beta\}(p_{long} + p_{loss})/A; \\ i_{sc}^{*} &= \{v_c - (v_a - v_b)\beta\}(p_{long} + p_{loss})/A; \end{aligned} \qquad (8)$$

where $A=\Sigma i=a,b,c\ V2i$

These extracted reference supply currents (*isa*, isb** and *isc**) are compared with the respective sensed supply currents (*isa*, *isb* and *isc*) and current errors after the amplification are used in the PWM current controller to generate the switching signals for the IGBTs of DVR.

2.1 Three Phase Downstream Fault When DVR Is Inactive

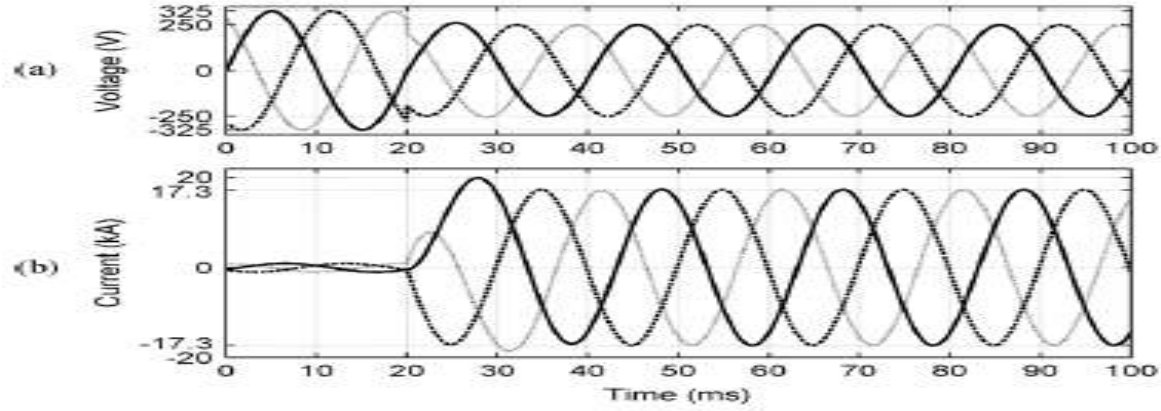

Fig. 2(A) Voltages at Bus3 (B) Fault Currents, During Downstream

Three-phase fault when the DVR is inactive (bypassed). The system is subjected to a three-phase short circuit with an eligible fault resistance at t = 20 ms at Bus5. Prior to the fault inception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about 17 times the rated load current (Fig).

2.2 Phase-To-Phase Downstream Faults When DVR Is Inactive

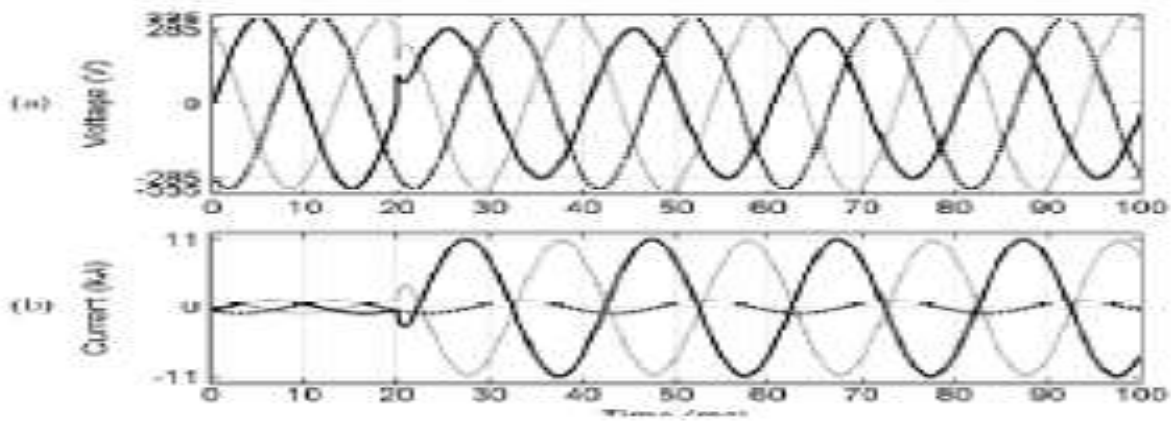

Fig.3 (A) Voltages at Bus3, (B) Fault Currents, During Downstream Phase-To Phase Fault When the DVR Is Inactive (Bypassed)

The system of Fig. 2 is subjected to a phase-A to phase-C fault with the resistance of 0.05Ω at 10% of the cable length connecting Bus4to Bus5, at t = 20 ms. When the DVR is inactive (bypassed) during the fault (Fig. 5), the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11times the rated load current.

2.3 Single-Phase-To-Ground Downstream Fault When DVR Is Inactive

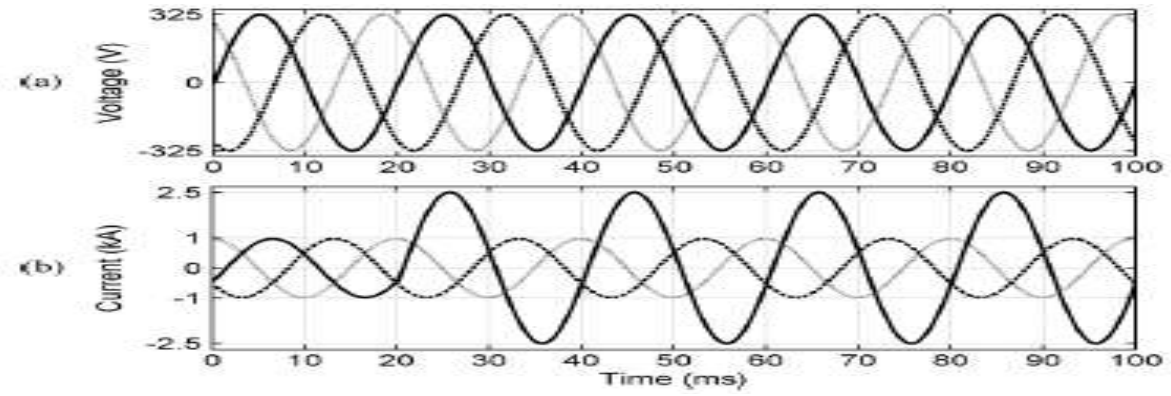

Fig.4.(A)Voltages At Bus3. (B) Fault Currents, During the Downstream Single Phase-To-Ground Fault When the DVR Is Inactive (Bypassed)

Phase-A of the system of Fig. 3 is subjected to a fault with the resistance of 0.2Ω at 10% length of the cable connecting Bus4to Bus5, at t = 20 ms. If the DVR is inactive (Fig. 2), the PCC voltage does not considerably drop and the fault current is about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted

by the relays. The reason is that the operation time of the over current relays is considerable for a fault current of about 2.5p.u

III. SIMULATION RESULTS

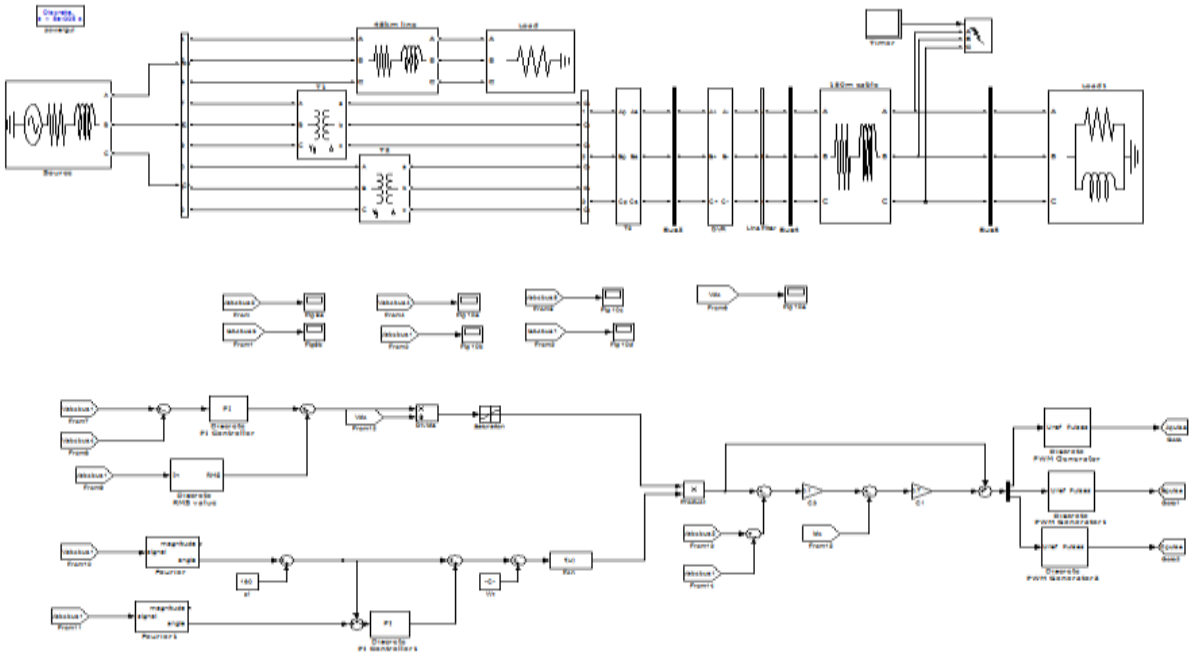

Fig.5.Simulation Block Diagram of Three Phases Downstream Fault Interruption with DVR

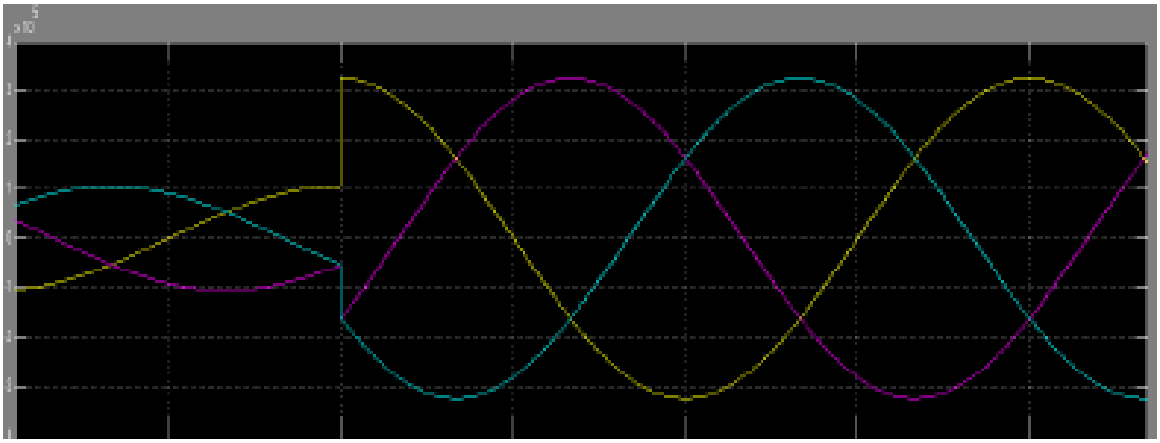

Fig.5 (A) .Injected Voltage with Time on X-Axis and Voltage on Y-Axis

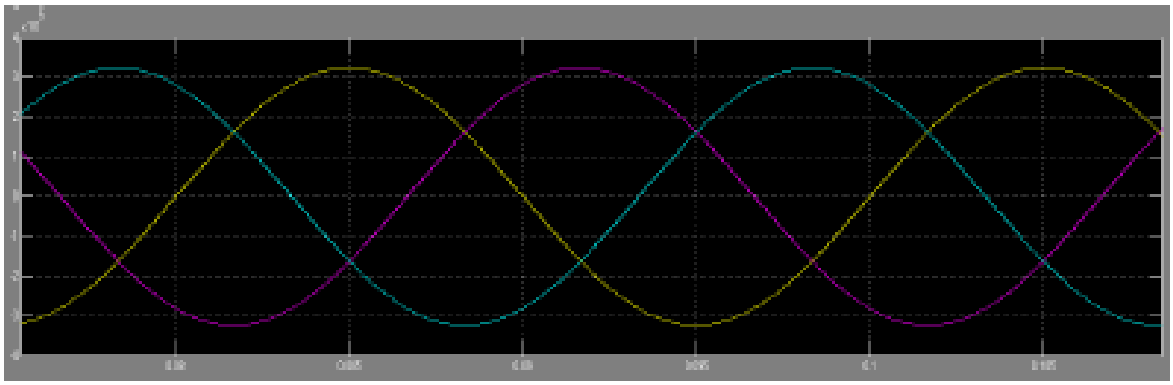

Fig.5 (B) Supply Voltage with Time on X-Axis and Voltage on Y-Axis

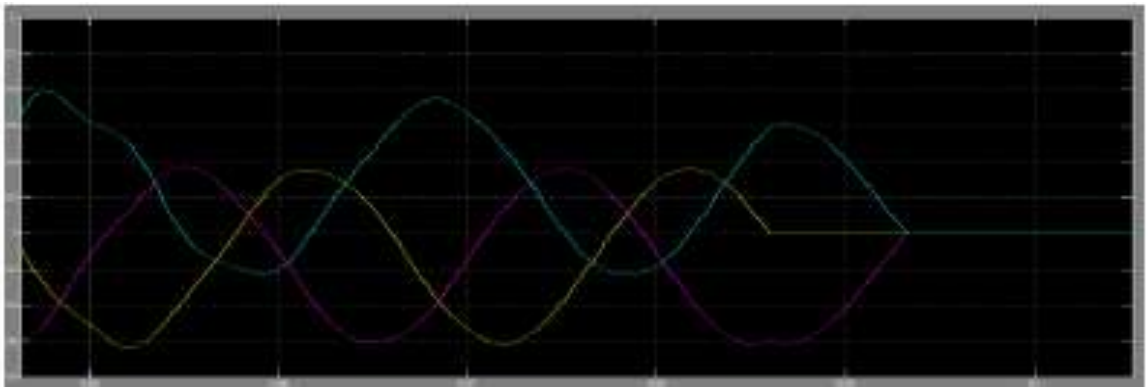

Fig 5(C) Line Current with Time on X-Axis and On Y-Axis

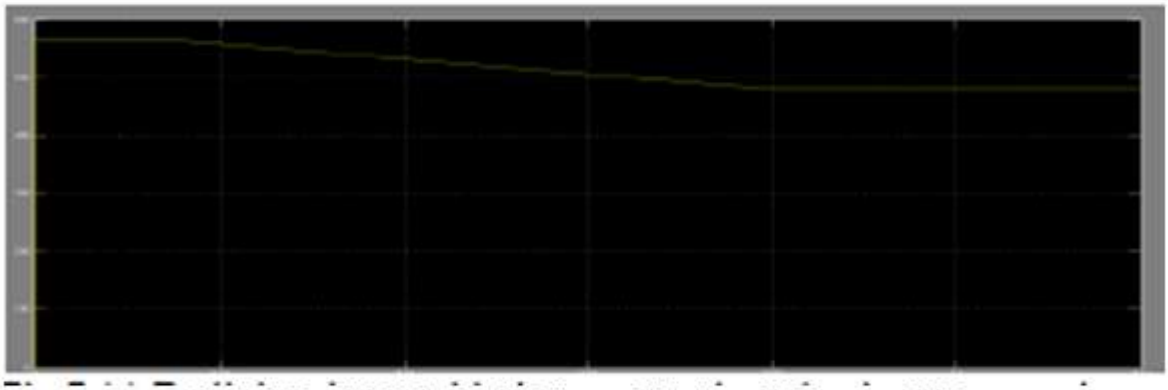

Fig.5 (D) Dc Link Voltage with Time on X-Axis and Voltage on Y-Axis

3.1 Phase to Phase Downstream Fault Current

3.1.1 Interruption with DVR

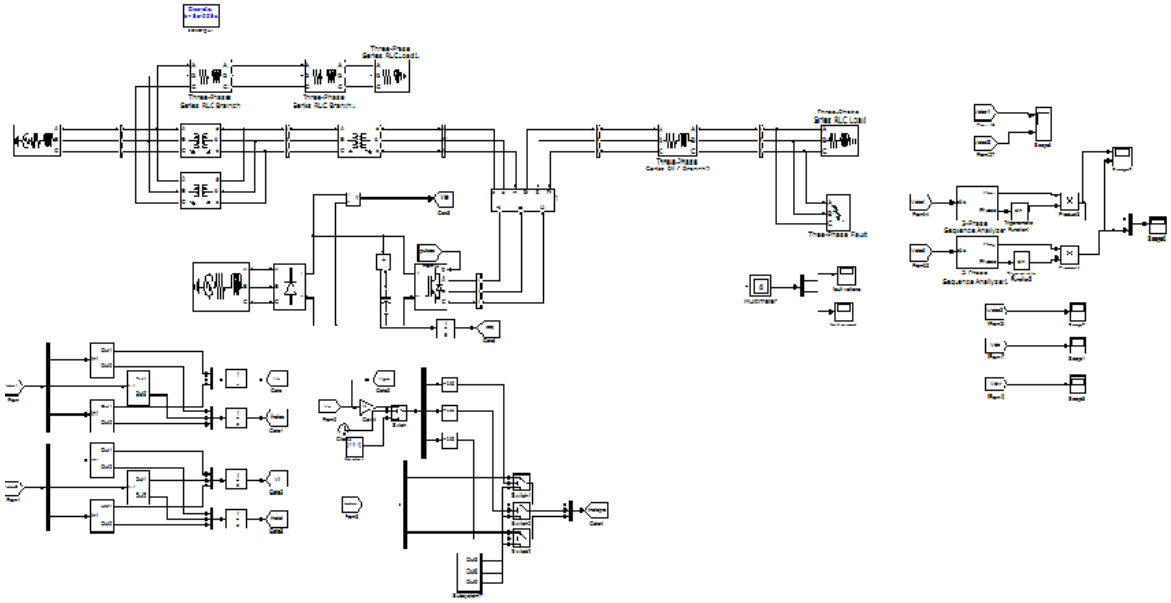

Fig.6.Simulation Block Diagram of Phase To Phase Downstream Fault Interruption with DVR

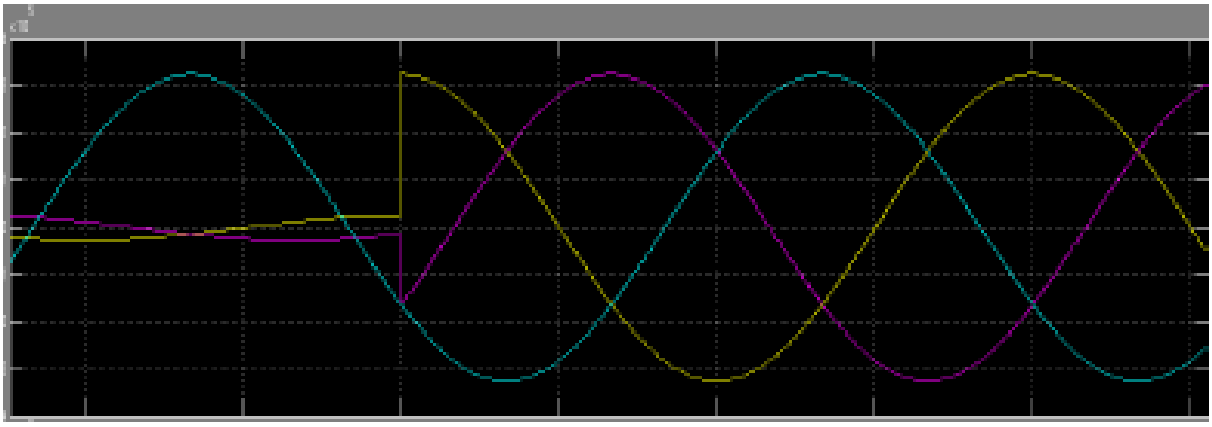

Fig.6 (A) Injected Voltage with Time on X-Axis and Voltage on Y-Axis

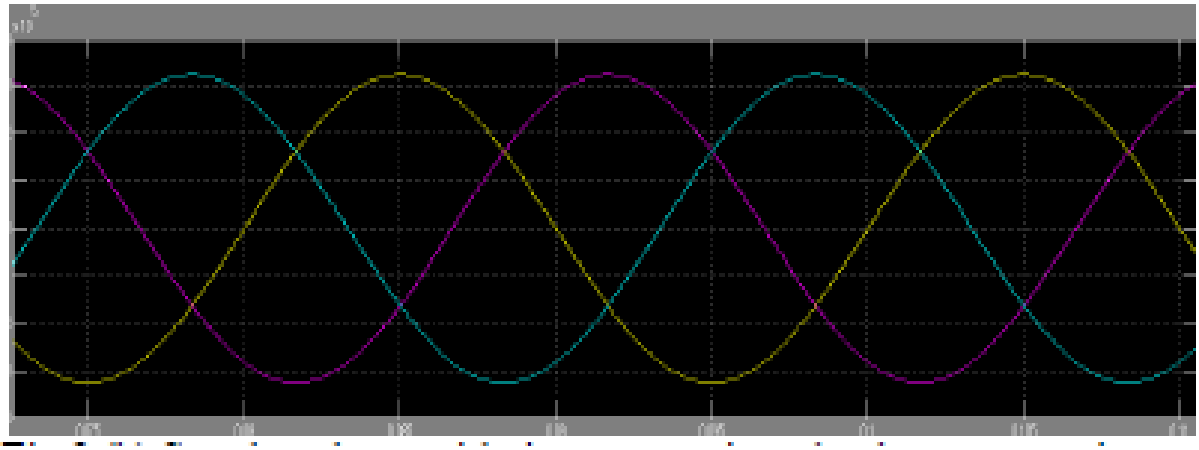

Fig.6 (B) Supply Voltage with Time on X-Axis and Voltage on Y-Axis

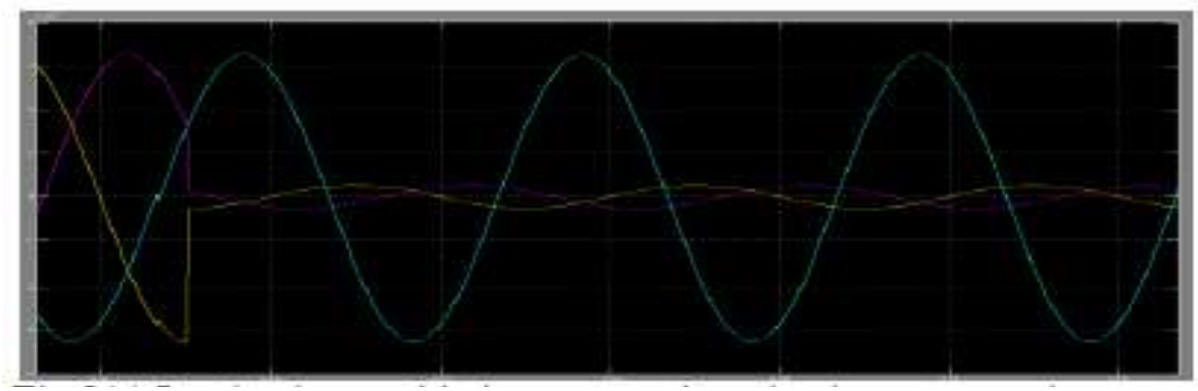

Fig.6(C) Load Voltage with Time on X-Axis and Voltage on Y-Axis

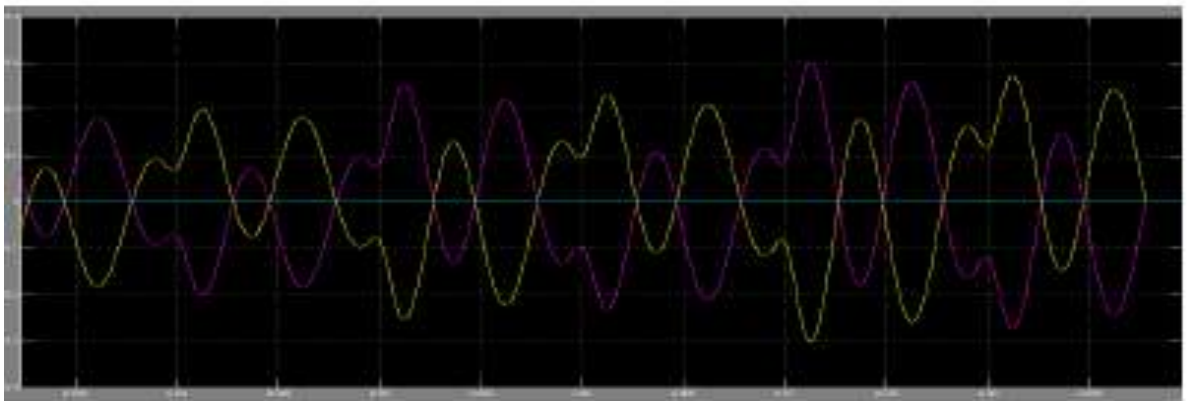

Fig.6 (D) Line Current with Time on X-Axis and Current on Y-Axis

3.2 Single Phase to Ground Downstream Fault

3.2.1 Interruption with DVR

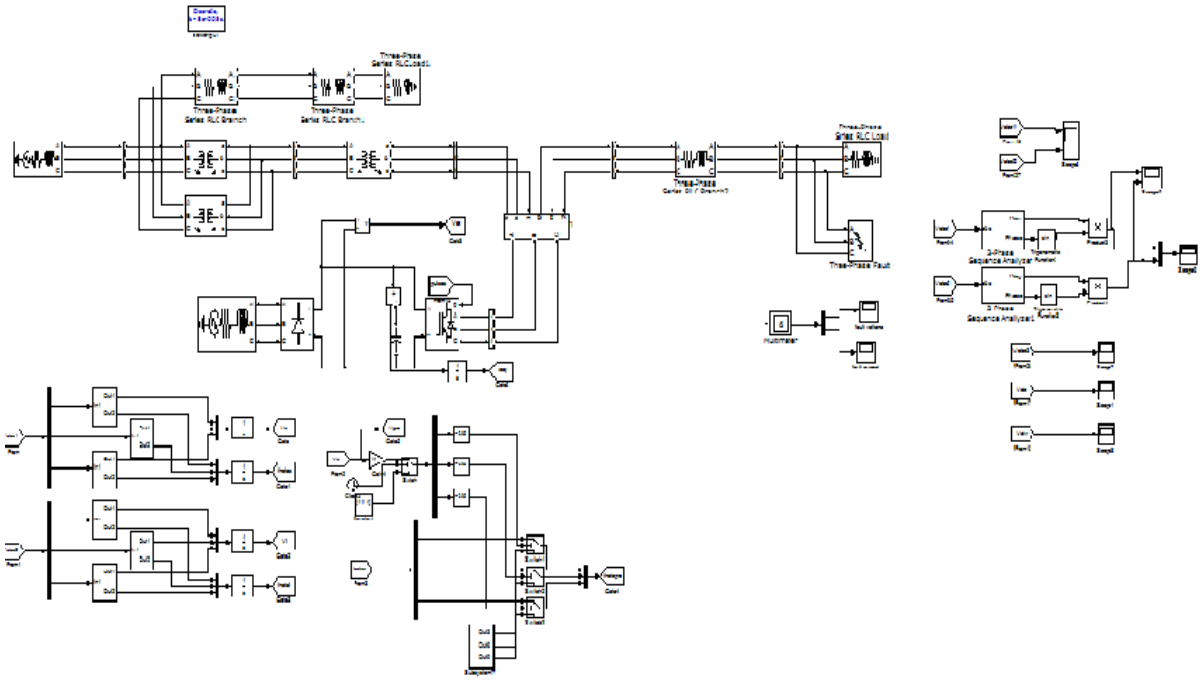

Fig.7.Simulation Block Diagram of Phase to Ground Downstream Fault Interruption with DVR

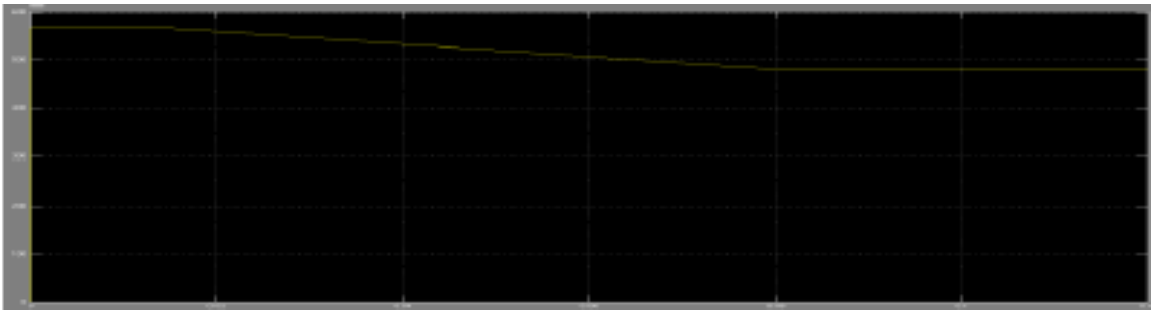

Fig.7 (A) Injected Voltage with Time on X-Axis and Voltage on Y-Axis

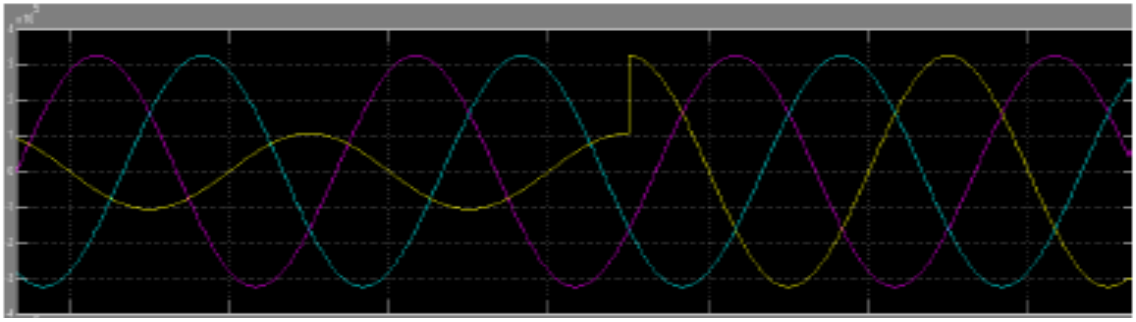

Fig.7 (B) Supply Voltage with Time on X-Axis and Voltage on Y-Axis

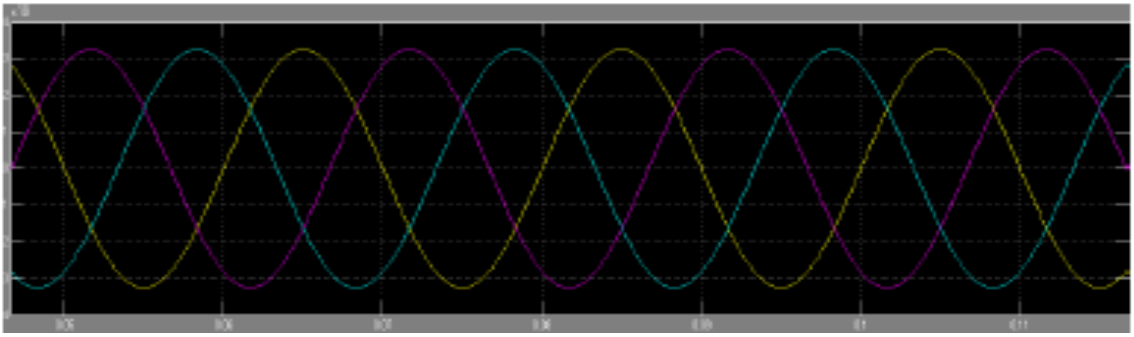

Fig.7(C) Load Voltage with Time on X-Axis and Voltage on Y-Axis

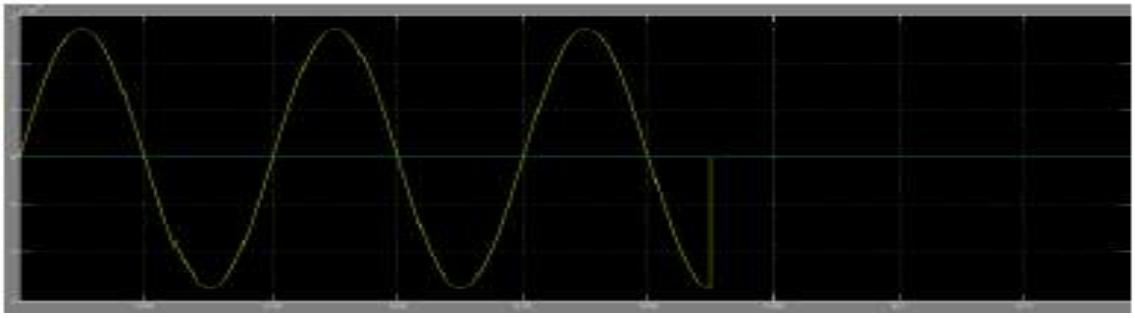

Fig.7 (D) Line Current with Time on X-Axis and Current on Y-Axis

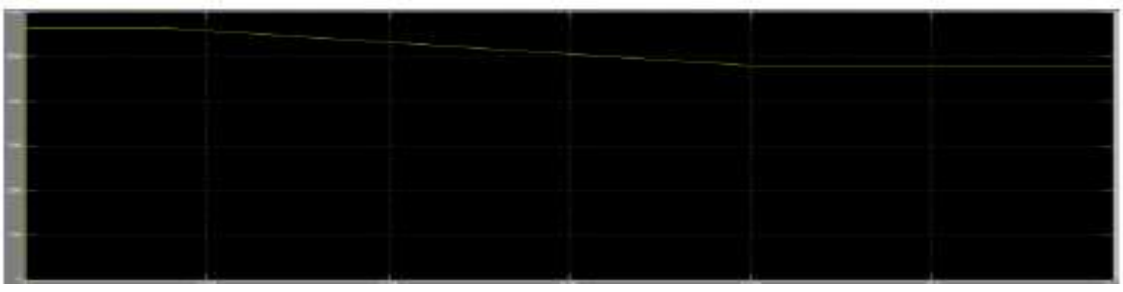

Fig.7 (E) Dc Link Voltage with Time on X-Axis and Voltage on Y-Axis

IV. PROPOSED CONTROL OF 3 LEG VSC BASED 3-PHASE 4- WIRE DVR USNG MODIFIED INSTATANEOUS SYMMETRICAL COMPONENT THEORY

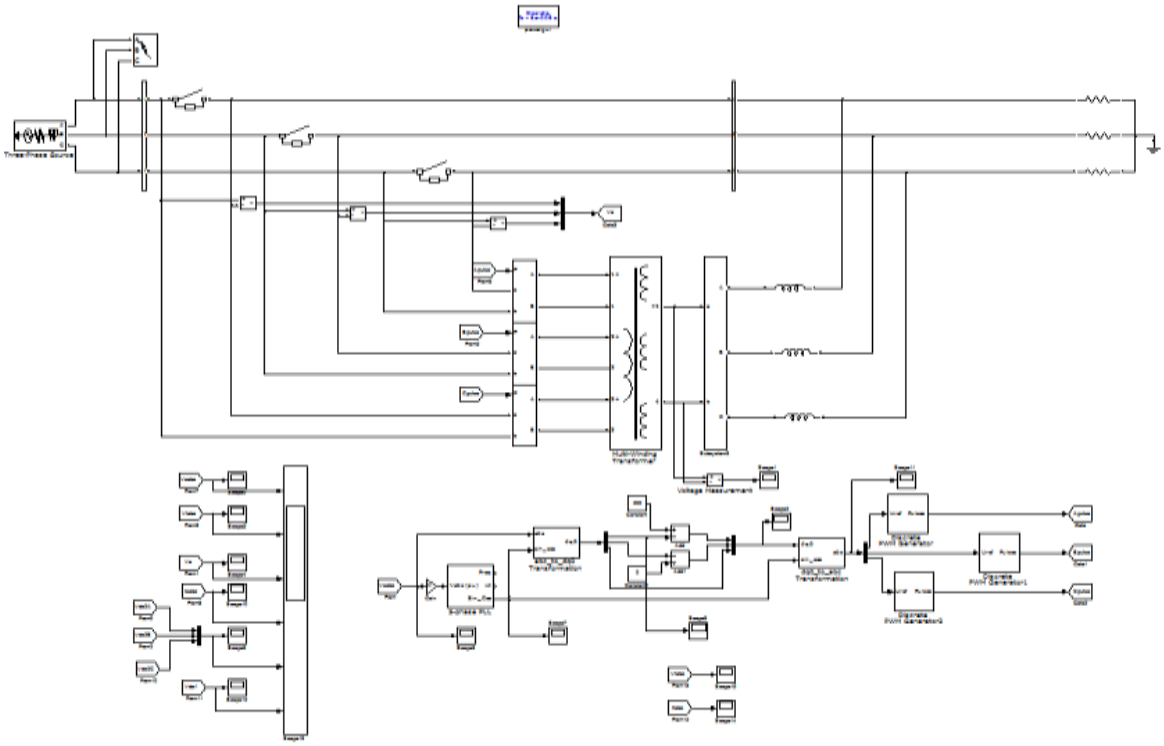

Fig: 8 Simulation Block Diagram of 3-Phase 4-Wire Modified DVR System

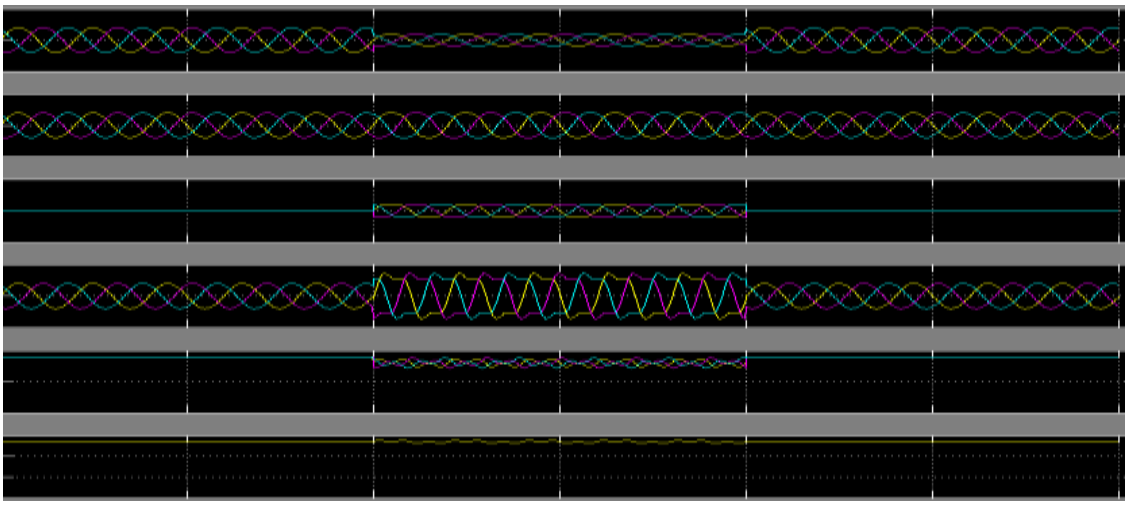

Fig. 8 (A) Performance DVR in PFC Mode for Linear Loads

V. CONCLUSION

The proposed multi loop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter. The proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50

Hz). In future enhancement simultaneous operation of Fault current interruption and voltage sag compensation can be obtained by Dynamic voltage restore.

REFERENCES

[1] Firouz Badrkhani Ajaei, StudentMember, IEEE, Shahrokh Farhangi, and Reza Iravani, Fellow, IEEE, "Fault Current Interruption by the Dynamic Voltage Restorer", IEEE Transactions on Power Delivery, Vol. 28, No. 2, April 2013.

[2] N. G. Hingorani, "Introducing custom power," IEEE Spectr., vol. 32, no. 6, pp. 41–48, Jun. 1995.

[3] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in Proc. IEEE APEC', 2001, pp. 1267–1273.

[4] G. J. Li, X. P. Zhang, S. S. Choi, T. T. Lie, and Y. Z. Sun, "Control strategy for dynamic voltage restorers to achieve minimum power injection without introducing sudden phase shift," Inst. Eng. Technol. Gen. Transm. Distrib, vol. 1, no. 5, pp. 847– 853, 2007.

[5] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Design and analysis of the inverter-side filter used in the dynamic voltage restorer," IEEE Trans. Power Del., vol. 17, no. 3, pp. 857–864, Jul. 2002.

[6] B. H. Li, S. S. Choi, and D. M. Vilathgamuwa, "Design considerations on the line-side filter used in the dynamic voltage restorer," Proc. Inst. Elect. Eng., Gen. Transm. Distrib., vol. 148, no. 1, pp. 1–7, Jan. 2001.