

DESIGN OF A VERIFICATION TECHNIQUE FOR QUADRATURE PHASE SHIFT KEYING USING MODEL SIM SIMULATOR FOR BROADCAST COMMUNICATION RELEVANCE'S

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ABSTRACT

This article presents the design of modulator for Quadrature phase shift keying (QPSK). QPSK also one type of phase shift keying which is under the digital modulation. The digital modulation is more efficient in transmission and more secure compared to other. The noise detection and correction are better in digital techniques over analog techniques. Convert the input data in digital and transfer over analog channel is defined the digital modulation. In these days, main factor to be considered is low power and less time. Shift keying techniques defines as the carrier bit stream changes in one or more parameters depending on the input bit stream, which we need to send. This present technique is designed in Verilog HDL and synthesized on XILINX ISE tool.

Keywords: *Quadrature Amplitude Modulation, Amplitude Phase Shift Keying, Binary Phase Shift Keying.*

I. INTRODUCTION

Digital techniques have replaced analog techniques in present growing world. Modulation is the process of changing the carrier signal. Digital modulation is defined as the processing of digital data transmission from transmitter to receiver over the analog informational channel (medium). In this process of modulation, the message signal changes the parameters of carrier signal. Usually we consider that amplitude, frequency and phase are the parameters for any signal or sequence. The digital modulation is classified depending on the basis of parameters of carrier signal. In digital modulation, three different techniques have present. These are:

1. Amplitude shift keying
2. Frequency shift keying
3. Phase shift keying

In digital technique, changing in the phase of the carrier is defined as Phase Shift Keying. The digital modulators are required to generate these signals depending on the technique we need. QPSK principle is often used in phase shift keying modulators. Both the accuracy and the stability of the generated signals must generally be addressed in the main factors of accuracy and stability. In real time, these are particularly when the parameters of interest have to be modified.

This digital transmission system has proved that it is more efficient than analog transmission because of the advancements in the fields of Digital Signal Processing (DSP) and Very Large Scale Integration (VLSI). In digital transmission, noise immunity, multiplexing different forms of information, security has improved and advantage over analog transmission. Phase shift keying uses a finite number of phases unlike all other digital modulation techniques, which uses finite number of distinct signals to represent the data.

II. LITERATURE SURVEY

2.1 Quadrature Amplitude Modulation

For high speed digital signals the dominant modulation mechanism is this QAM. This QAM becomes our daily usage system as wireless protocols, modems to military for personal communications. In QAM, the two carriers are of 90 degrees out of phase and makes change in the amplitude of the carrier signals.

Implementation of QAM has done in three stages i.e., modulation, transmission and demodulation. In this article, we are focusing on modulation itself. The modulation involves two stages:

1. Serial to parallel conversion
2. Digital to analog conversion

In serial to parallel conversion, it changes the bit stream into $\log_2 M$ streams, where M is number of symbols. The bit rate is defined as $1/\log_2 M$.

In second digital to analog conversion, the input streams have index a look up table. One signal modulates quadrature Q, carrier and the other modulates in-phase I, carrier. Sampling rate of the system is greater than the symbol rate then it is called analog. Here we can't find true analog system. Finally add Q and I signal to form a QAM signal.

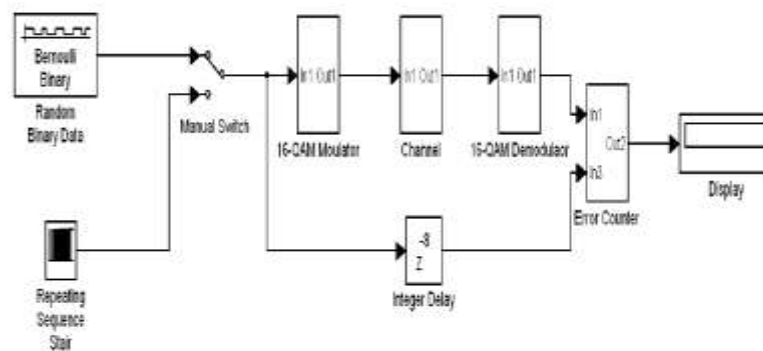


Fig 1: Example Diagram For 16-QAM

2.2 Binary Phase Shift Keying

BPSK also called as phase reversal keying (PRK) or two phase shift keying. It is simplest form of PSK. It takes two phases separated by 180 degrees. That's the reason why generally it is called as 2-PSK. We can't say where these points have located. It has many disadvantages like the highest rate of noise distortion, can able to transmit 1 bit/symbol. So, it is not suitable for high data transmission applications.

In BPSK, the term "binary" is indicating that it can transfer one binary valued quantity within bit duration. Phase shifting made by π . Keying comes back to the first electrical communication system. It is a method of transferring the message on carrier. That carrier signal may be base band signals or free- space transmissions otherwise large context of another signal. This provides carrier, for which phase is changes between 0 and 180

degrees. BPSK is popular in digital electronics and because of the immunity of noise makes demand in many fields.

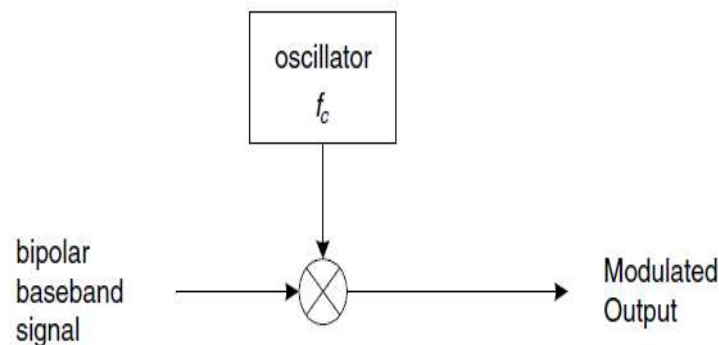


Fig 2: BPSK Modulator

The above figure shows the BPSK modulator. The output of the modulator is defined as

$$X(t) = I(t) + jQ(t)$$

III. PROPOSED METHOD

3.1 Quadrature Phase Shift Keying (QPSK)

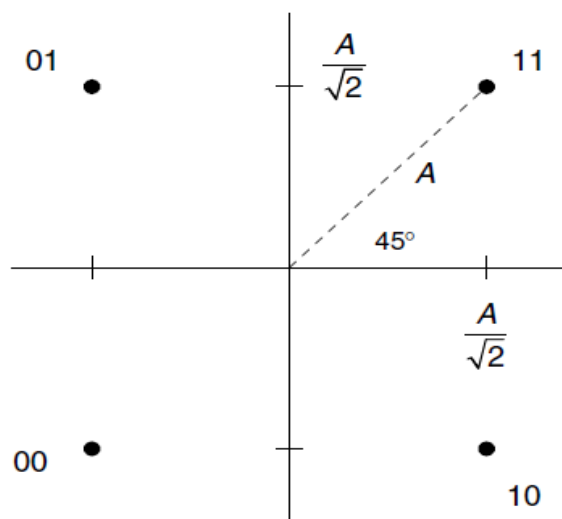


Fig 3: Ideal QPSK Constellation

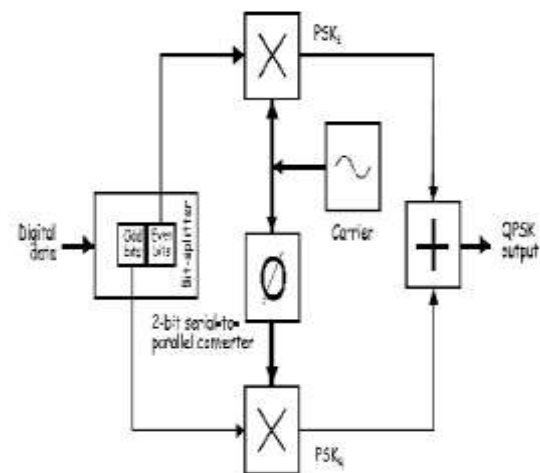


Fig 4: Block diagram of QPSK

QPSK is one of the types of phase shift keying. It is related with the BPSK. This scheme also uses double side band carrier suppression method as like BPSK but the difference is it can able to send two bits of digital stream at a time. This makes more amount of users can able to access on the channel.

The generation of QPSK is shown in fig 4. The input data is directly given to the bit splitter to split it as even (i.e., 0, 2, 4....) and odd (1, 3, 5.....) bits. These even bits are directly multiplied with the carrier signal in the multiplier block to generate a BPSK signal i.e., PSK_I as shown in figure. At the same time remaining odd bits are multiplied with the 90 degrees phase shifted carrier signal in the other multiplier block to generate another BPSK signal i.e., PSK_Q . Then the both BPSK signal simply added in adder block and transmits to output.

This structure has used the trigonometric identity as defined as below

$$I \cos \omega c t + Q \sin \omega c t = R \cos (\omega c t + \Theta)$$

Where $R = \sqrt{I^2 + Q^2}$ and

$$\Theta = \tan^{-1}(Q/I).$$

The modulated signal is defined as simple as

$$X(t) = I(t) + Q(t).$$

There the complex signal $X(t)$ is formed by using in-phase component as real part and Quadrature component as imaginary part. Now we are going to discuss about constellation part.

3.2 Constellation

There are four possibilities for transmission i.e., 00, 01, 10 and 11. At every possibility the modulator shifts the phase of carrier signal i.e., $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$ as shown in fig 3. Each output differs by one bit only. Hence, it is called as 4 PSK. QPSK has to maintain the data rate either double of BPSK data rate while maintain the bandwidth of the signal or at the time of half bandwidth needed, it uses same data rate of BPSK. QPSK results in two functions; these are in-phase component and Quadrature component of the signal.

3.3 Flow Chart for QPSK Process

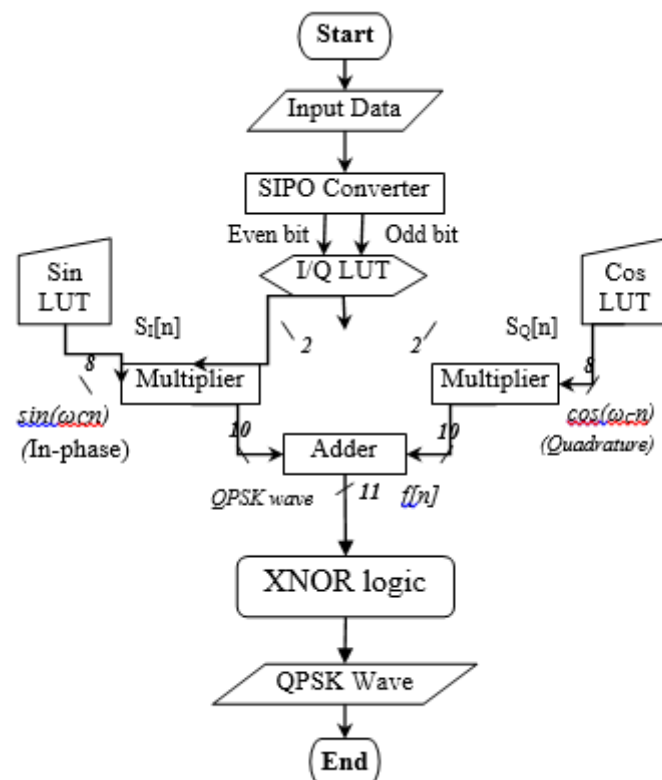


Fig 5: Flow chart of QPSK

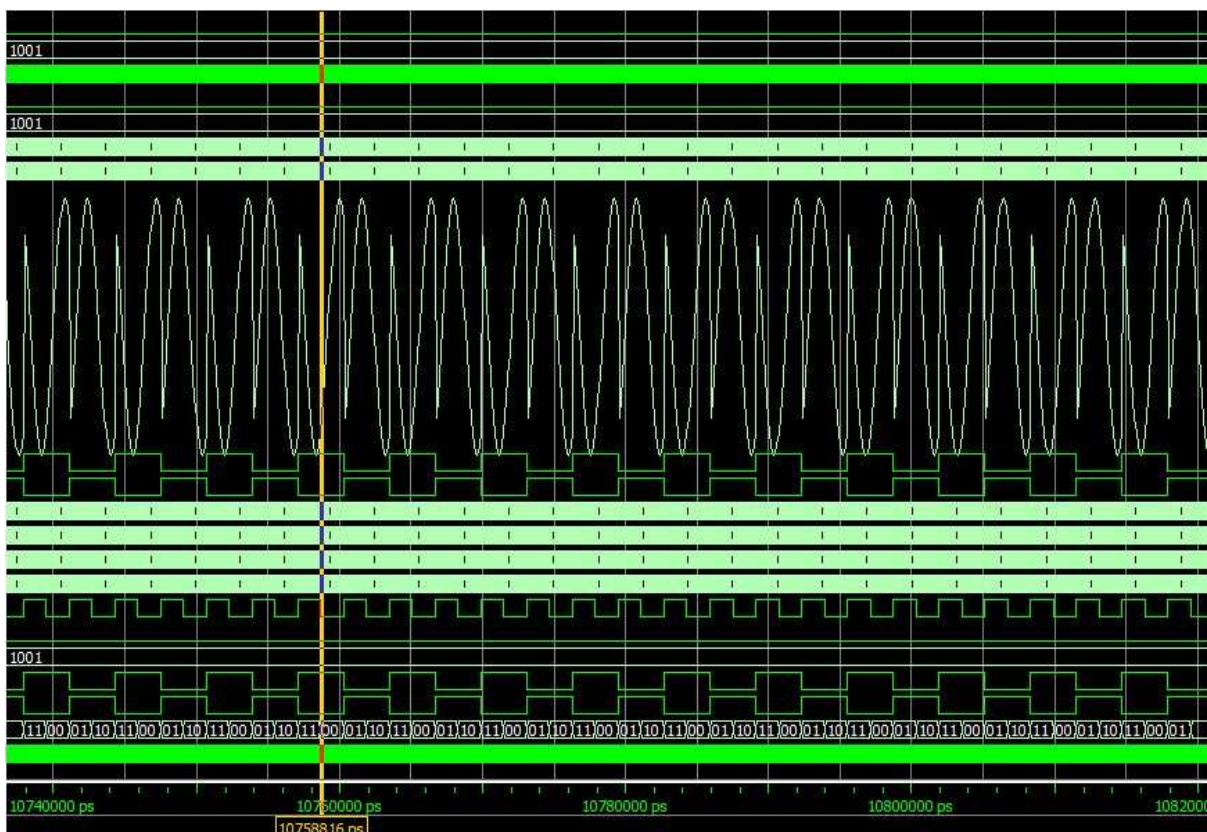
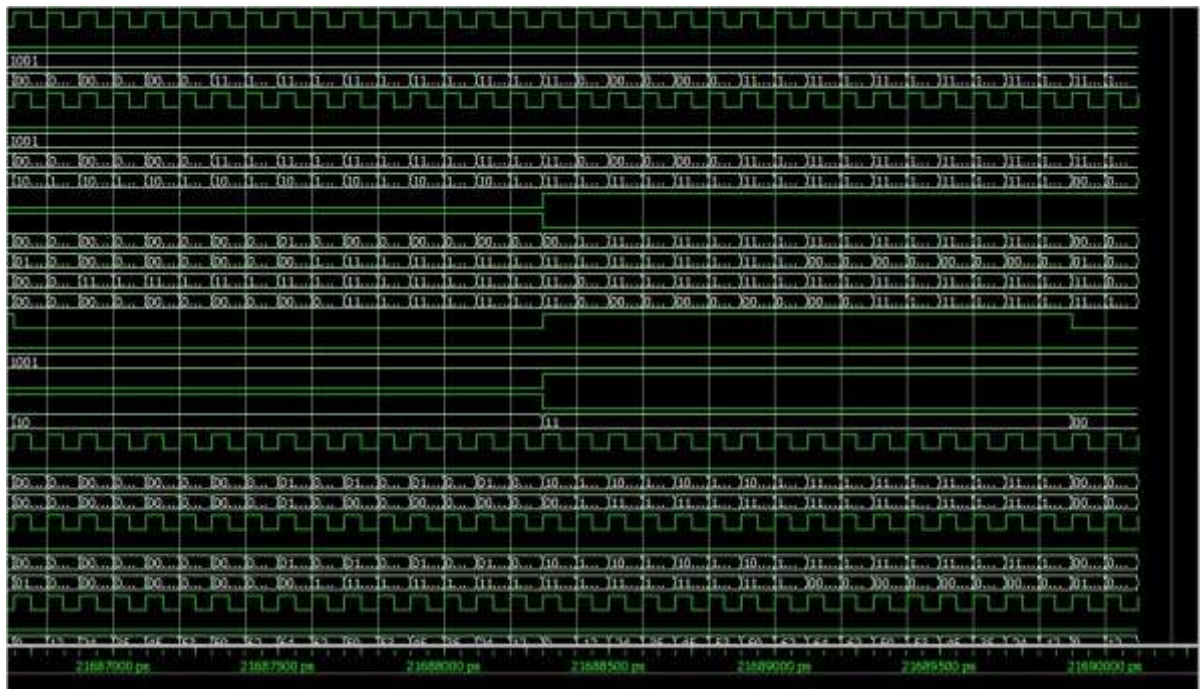
From the above flow chart, we can observe that the input data directly given to the SIPO converter. It divides the input data as even and odd. These even and odd are multiplied in separate multipliers with sinusoidal and cosine waves respectively. Here the sine wave is in phase component and the cosine wave is quadrature phase

component. The outputs of both the multipliers are added in adder block. It gives the output known as QAM. This signal is forwarded through a XNOR logic gate to get QPSK signal i.e., output. Simulation results and conclusion have shown in below discussions.

IV. SIMULATION RESULTS

In this paper we are designing the QPSK using the Verilog HDL and synthesised in MODEL SIM6.2.

This synthesis reports yielding that expected wave forms are matching with the practical results shown here.





V. CONCLUSION

The design of QPSK has designed and verified. It can able to transfer two bits per symbol using four phases leads to minimize the chip area and decreases the power consumption. Our structure minimizes the number of blocks to perform this technique. The obtained simulation results are verified successfully.

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