A NEUTRAL CURRENT COMPENSATION FOR THREE-PHASE FOUR-WIRE UPQC

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ABSTRACT

The unified power quality conditioner (UPQC) is an advanced custom power electronic device, which compensates the voltage and current- related power quality problems in the power distribution arrangements. In this project a UPQC technique for applications with neutral current compensation technique with a non-stiff source is implemented. The implemented technique functions to operate the UPQC to reduced dc-link voltage without compromising its compensation capability apparoachment. This technique is proposed to maintain the reduced neutral current and match the dc-link voltage requirement of the series and shunt active filters of the UPQC. The system uses a capacitor in series with the interconnecting of an inductor of the shunt connected active power filter, and the neutral point of the terminal is connected to the star connected transformers to the load and also connected to the UPQC. The average switching frequency of the power electronic switches is minimized then correspondingly there reduction in the switching losses of the inverter. Detailed design arrangements of the VSI parameters and series capacitor have been explained in this paper. The experiment results are taken out on 3-phase UPQC prototype to verify the proposed system technique and the simulation results are verified by using the PSCAD/MATLAB and the results are presented in this paper.

Index Terms*: *Average Switching Frequency, Neutral Current Compensation Technique, Hybrid Topology, Dc-Link Voltage, Unified Power Quality Conditioner (UPQC), Non-Stiff Source.

I. INTRODUCTION

With The progression of power electronics and digital control techniques, the non-conventional energy sources are gradually increasingly being associated to the distribution systems arrangements. On the other hand, with the explosion of the power electronics parameters, nonlinear loads, distortions and unbalanced loads have reduced the power quality (PQ) in the power distribution network arrangements. Tradition of power devices have been implemented for increasing the quality and performance of generated electrical power. Unified PQ conditioner (UPQC) is an adaptable tradition power device which having of two inverters associated back-to-back and involves in supply voltage, neutral current and load current problems. UPQC can concurrently work as shunt and series active power filters. The series connected filter of the unified control strategy UPQC is called as dynamic voltage restorer (DVR). It is used to sustain balanced, ripple free nominal voltage at the load side. The shunt connected facts device in UPQC is called as distribution static compensator (DSTATCOM), and it is used to regulate the required load reactive power, distortions and maintain the load currents thereby controlling the source current balanced and ripple free with maintained the unity power factor. Consideration of Voltage rating of dc-link capacitor highly affects the compensation quality performance of an active filter.

In universal, the produced dc-link voltage for the shunt active filter has much larger value than the maximum value of the line-to-neutral voltage. This is completed in order to get a proper protection at the peak of the sending source voltage. The authors explained about the current harmonic contents control limit and loss of monitoring limit, which explains that the dc-link voltage must be larger than or equal to √6 times than the phase voltage of the operating system for ripple free elimination. When the dc-link voltage is lower than this control limit, there is in proper resultant required voltage to drive the currents produced from the inductances so as to find out the reference currents to neglect the ripples.

The first condition for reactive power compensation technique is that the amplitude of reference dc-bus capacitor voltage must be larger than the maximum voltage at the point of common coupling (PCC). Because the before mentioned analysis, many researchers have utilized a larger value of dc capacitor voltage depended on the required applications. Correspondingly, for the series active filter, the minimum maintenance of dc-link voltage is controlled at a value equal to the maximum value of the line-to-line voltage of the system for sufficient compensation.

In the state of the UPQC, the dc-link voltage constraint for the series and shunt active filters is not the equal compensation. Thus, it is a challenging major task to have a frequent dc-link of suitable rating in order to accomplish acceptable shunt and series compensation.

The shunt active filter functioned with the higher dc-link voltage when concerned to the series active filter for effective compensation. In order to get effective compensation for both series and shunt active filter, the developers are avoid with no choice rather than to choose ordinary dc-link voltage depended on shunt active filter obligation. This will effect in over evaluation of the series active filter as it necessities less dc-link voltage checked and verified shunting active filter.

Due to this principle, a higher dc link voltage depended on the UPQC technology has been recommended. With the larger value of dc-link capacitor and the voltage source inverters maintenance is very excessive, and the power electronic switching elements are preferred to control the VSI also necessary to be required and sufficient higher values of voltage and current. In this case enhanced the total size and cost of the Voltage Source Inverter. To diminish the dc-link voltage storage ability, few steps were implemented in order to get the proper result in the demonstration. In a hybrid filter has been explained for motor drive applications features. The filter is associated in shunt with a diode rectifier and triggered at seventh harmonic frequency. Even though a graceful work, the implementation is particular specified to the motor drive requirement, and we have not considered the reactive power compensation, which is a significant feature in UPQC applications.

The three-phase four-wire arrangement, neutral-clamped technology is performed for UPQC. This technology explains that the independent control implementation of every leg of both the series and shunt connected inverters, but it uses capacitor voltage controlling is explained, four-leg VSI strategy for shunt active filter has been implemented for three-phase four-wire system arrangement.

This process eliminates the voltage balancing controlling of the dc-link capacitor, however the autonomous control of the inverter legs is not achievable. To conquer the troubles concerned with the four-leg strategy, the authors implemented a T-connected transformer and 3-phase VSC depended DSTATCOM. Nevertheless, this method leads to increases the cost and size of the UPQC because of the occurrence of additional transformer.

In this project, a UPQC strategy with minimized dc-link voltage is developed. This method consists of capacitor is connected in series with the interfacing inductor of the shunt connected active filter. The capacitor enables and maintains the minimization of dc-link voltage condition of the shunt active filter and concurrently maintains

the proper requirement of reactive power to the load side, so it is maintain nearly unity power factor improvement, without facilating the effective technique in its performance. This permits us to maintain the dc-link voltage requirement capabilities of the series and shunt active filters strategy with a common mutual dc-link capacitor.

Additional, in this arrangement, the system neutral is associated to the star connected transformers to the load and also connected to the UPQC negative terminal point of the dc bus. This will vanishes the neutral current compensation and also maintain the requirement of the fourth leg in Voltage Source Inverter of the shunt connected active filter and enables independent control of each leg of the shunt VSI with a single dc capacitor.

The simulation results are carried out using PSCAD/MATLAB simulator; results are obtainable in the paper. An example of three-phase UPQC is designed in the experiments to test and verify the developed method, and the complete results are accessible in this paper.

II. EXISTING SYSTEM

In this the traditional and developed technology of the UPQC is explained in detailed manner. For this purpose we are designed a power circuit of the neutral-clamped VSI technology-depended UPQC which is preferred as the traditional topology in this investigation. Although this topology uses two dc energy storage devices, each leg of the Voltage Source Inverter can be regulated independently, and identifying the problem and controlling in very smooth with less number of power electronic switches when verified with other VSI strategies.

In this technology we are designed like, *vsa*, *vsb*, and *vsc* are sending end voltages of particular phases such as a, b and c. The voltages of the *vta*, *vtb*, and *vtc* are terminal point voltages of the converter. The voltages of the dynamic voltage restorer are given as *v*dvr*a*, *v*dvr*b*, and *v*dvr*c* are additional voltages are generated by the series connected active filter. The three phase sending end currents are demonstrated as by *isa*; *isb*, and *isc*, and the load side currents are denoted by *ILA*, *ilb*, and *ilc*. The shunt connected active filter currents are represented by *ifa*, *ifb*, *ifc*, and *iln* gives the current in the neutral leg. *Ls* and *Rs* give the feeder

The interconnecting the parameters like inductance (L) and resistance (R) of the shunt connected active filter are denoted by *Lf* and *Rf* considered and they are connected to internally inductance and filter capacitor of the series connected active filter are noted by *L*se and *C*se, correspondingly.

The load connected with both linear and nonlinear loads for our desired requirement. The dc-link capacitors alignment and voltages between them are identified by *C*dc1 = *C*dc2 = *C*dc and *V*dc1 = *V*dc2 = *V*dc, correspondingly, and the entire total dc-link voltage is specified as *Vd*bus *V*dc1 + *V*dc2 equals to the 2*V*d. In the developed topology, the voltage between each common mutual dc-link capacitor is selected as 1.6 times more than the peak value of the sending side voltages as given.

In this strategy, the system neutral has been associated to the negative point of the dc bus along with the capacitor Cf is associated in series with the interconnecting inductance of the shunt connected active filter.

The passive capacitor *Cf* has the ability to maintain a part of the reactive power required sufficient by the load side converter, and the active filter will neutralize and controls the required sufficient reactive power and the distortions are presented in the load. The extra parameters like the placing of a capacitor in series with the interconnecting inductor of the shunt connected active filter will drastically minimize the dc-link voltage necessity and accordingly decreases the average operating frequency of the switches.

This concept will be designed with analytic explanation in the consequent part. The minimized dc-link voltage constraint of the shunt active filter functioned us to the maintain the dc-link voltage constraint with the series

connected active filter. This method vanishes the high rating of the series connected active filter of the UPQC regulation system arrangement.

The developed project of the series capacitor *Cf* and the other VSI devices have major effect on the quality of the compensator. These are specified in the next segment. This strategy uses a single dc capacitor unlike the neutral-clamped method and as a result avoids the requirement of complementary the dc-link voltages.

Each leg of the inverter can be prohibited separately in shunt connected active power filter. Special the methods are explained in the literature, this strategy does not necessitate the fourth leg in the shunt connected active filter for three-phase four-wire system arrangement. The quality of this topology will be mentioned in clear

Generally in this arrangement provides the power quality of the distribution system maintain the effective control strategy for the mitigation of harmonics under unlike dc link voltages condition and also maintain the sudden change in voltages and it also maintain the load side current does not producing the ripples in load side consideration .But in this circuit it is intended the neutral current compensation and hence the power quality of the system reduces them the reliability of the system reduces correspondingly.

III. PROPOSED SYSTEM

The proposed implemented block diagram is illustrated below mentioned figure 1. By using the three phase-four les compensation technique we can control the neutral current compensation, harmonic mitigation, unbalancing load conditions also it maintains the proper balancing voltages with sufficient reactive power compensation is provided **.**

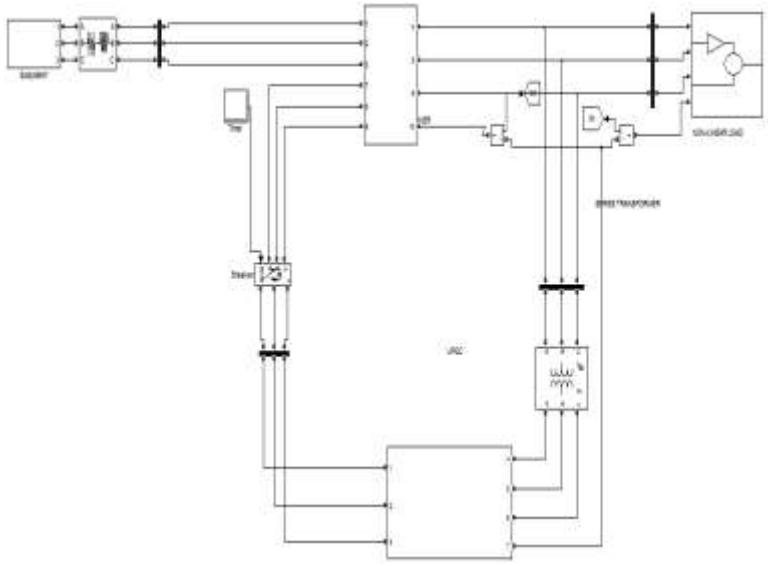

Fig:1 The Schematic Diagram For The Proposed System

There various control strategies are developed to control and maintain the required sufficient power quality achieved by the instantaneous active and reactive power control method (p-q theory), synchronous reference frame (d-q theory) , power balance technology and also maintain by using the hysteresis loop control strategy we can achieve the requirement by monitoring the D-STATCOM and voltage source converters (VSC) are produced load requirements.

In the active and reactive power control strategy we are calculated the values of active and reactive power values are measured after filtering the harmonics of the three phase four wire system arrangement. D-SATCOM and VSC are effective control strategies to maintain and control of the neutral current compensation.

IV. NEUTRAL CURRENT COMPENSATION METHOD

The main consideration of to produce the neutral currents in the three phase distribution systems are by the unbalancing phase currents are developed because of the in proper single phase rectifiers and harmonic content will be presented in the distribution systems because of the sending end voltage having the third harmonic contents. Not even in the unbalanced conditions only even balanced voltage consideration situations they may chance to produce the neutral current.

In the balanced voltage consideration there very high neutral current will be generated in the three phase systems with the computer loads i.e. non-linear loads are operated in those developed systems. There is a scope to produce the ripples in the three phase distribution by the non-linear conditions.

There is various strategies are performed to mitigate the neutral current compensation by monitoring the active and reactive power compensation control, synchronous reference frame, power conditioning strategy also maintain the use of zigzag transformers in the distribution systems also by the use of hysteresis loop control strategies are mitigate the unwanted harmonics, distortions and hence the load becomes ripple free in the distribution system considerations.

By presented the these type of ripples in the distribution systems the power quality of the system is reduced so we have to maintain and employed an advanced control strategy to control the these currents in order to get the required sufficient power quality of the system. In our project we are implemented the hysteresis loop control strategy is compensate the harmonics and hence the power quality of the reaches to very high.

V. HYSTERISES LOOP CONTROL

The traditional hysteresis current band control method is maintained very effective and fast response, unconditioned stability and produced better accuracy from the uneven switching frequency responses it produces the acoustic noise is generated due to this the designing of the input filters is very difficult to design for this reason the hysteresis loop control technique is implemented.

The conventional hysteresis band control is represented in the below mentioned figure. The figure compresses that it is having the hysteresis around the reference line current, the required reference current in the line of the active filter is denoted by *I**c And the actual line current is represented by the *I*c.

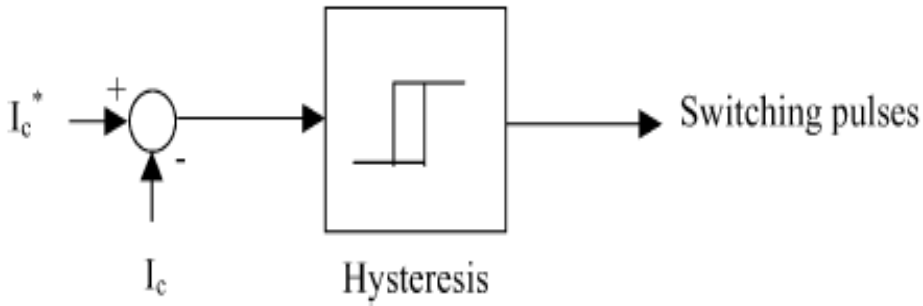

Fig: Traditional Hysteresis Band Current Controller

The switching pattern is decided by this hysteresis current band control technique it can provide the pulses to the corresponding converters. The switching logic for the hysteresis loop strategy is explained as follows:

If the function performed the in this manner *Ica* < (*i*∗ ca− HB) then the upper switch is goes to OFF and lower switch is goes to ON for converter leg “a” (SA=1).

If the function performed the in this manner *i*ca > (*i*∗ ca + HB) upper switch is goes to ON and lower switch is goes to OFF for converter leg "a" (SA = 0).

The switching pulses are determined by measuring the currents then after checking the functions by maintain the states of SB and SC for the phases of B and C we can generate the pulses for the converters to performed successful manner. The hysteresis loop control band width (HB) is affects by changing the upper and lower limits of the band control then response of the system is also varies.

The band width of hysteresis current control is affected by the instantaneous compensation current variation (d*i*c/d*t*) and *V*dc voltage to maintain and minimized the influence of the current distortion content to the modulation waveform.

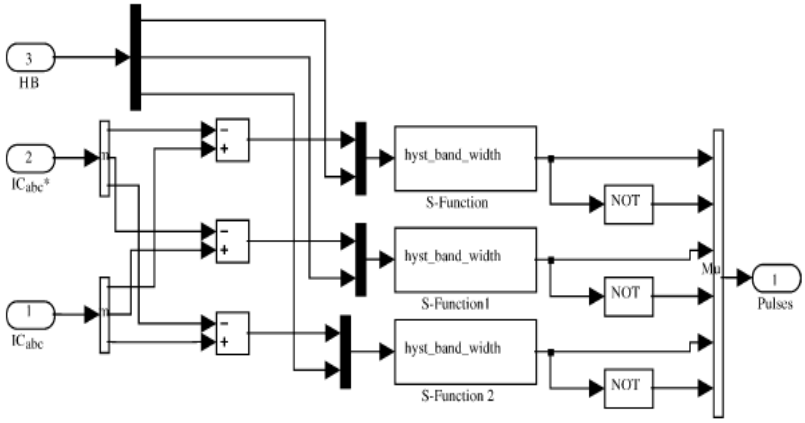

Fig: The Block Diagram for the Hysteresis Band Current Controller

The modulation frequency of the supply voltage and the voltage of capacitor and scope of the required reference current of the compensator *I**c current wave. The block diagram for the hysteresis current is illustrated above mentioned figure and it is functioned by calculating the values of voltage *V*dc and frequency of the modulation signal and also PWM technique performance is improves active power filter performance to produce the pulses to the converters.

VI. CONCLUSION

UPQC technology for three-phase four-wire system arrangement has been implemented in this suggested paper, which has the ability to mitigate the load voltage by maintaining the lower dc-link voltage based on the non-stiff source. The Design of the filter elements for the series and shunt active filters is demonstrated in detail manner. The proposed control apparoachment is explained from the simulation and experimental results in a 3-phase distribution system arrangement with neutral-connected to the star connected transformer UPQC technology.

The implemented strategy reduces the neutral current compensation by maintain the hysteresis loop band control strategy gives the advantages of both the neutral-clamped technology and the four-leg strategy. Detailed compensation strategies are designed for the conventional and required sufficient methodologies. From the discursion, it is obtained that UPQC strategy with hysteresis control and PWM strategy will improves the performance of the system is very effective manner and also has less THDs in the source currents and less average operating frequency, and required load voltages with minimized dc-link voltage as compared to the traditional UPQC topology.

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