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LOW POWER AND REDUCED AREA IN CARRY SELECT ADDER

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ABSTRACT

Power consumption and reduced area is one of the most important design objectives in integrated circuits. As adders are the most widely used components in such circuits, the adders must be design efficiently. This paper proposes the simple and efficient approach to reduce the maximum power consumption and area. Based on the idea of sharing two adders used in Carry Select Adder a new design of a low-power high performance adder is presented. In the regular Carry Select Adder one of the Ripple Carry Adder is replaced by Binary Excess Code-1 and further BEC-1 is replaced by carry selection and carry generation unit. The result analysis shows that the proposed structure is better than the conventional CSLA.

Keywords: Adder, Carry Select Adder (CSLA), Modified CSLA (MCSLA), Square Root CSLA (SQRT CSLA).

I INTRODUCTION

There are different entities that one would like to optimize when designing a VLSI circuit. These entities can often not be optimized simultaneously, only improve one entity at the expense of one or more others. The design of an efficient integrated circuit in terms of power, area and speed simultaneously, has become a very challenging problem. Power dissipation is recognized as a critical parameter in modern VLSI design field. The objective of adder is to provide a physically compact, high speed and to consume low power. To save significant power consumption of a VLSI design, it is a good direction to reduce its total power. Adders are used to calculate addresses, table indices, and similar operations. Recent trends in VLSI are moving towards the need of adders, which consumes low power. Design of area- and power-efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder.

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design.

II PAPER CONTRIBUTION

In this paper high speed Carry Select Adder is designed to perform the fastest addition operation. In the ripple carry adder 'N' bit number is added but one of the disadvantage is delay is increased. In the next stage to overcome this problem the conventional Carry Select Adder and regular Carry Select Adder is designed to perform the fastest addition.

The proposed Carry Select Adder is designed using carry selection unit and carry generation unit. It reduces area, power and delay when compared to existing Carry Select Adder.

III PRELIMINARIES

3.1 Types of Carry Select Adder

The number of bits in each carry select block can be uniform, or variable. When variable case, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of multiplexer delays. The two types of Carry Select Adder they are Uniform sized adder and Variable sized adder. In the Uniform sized adder there are two types they are conventional Carry Select Adder and modified Carry Select Adder.

3.2 Ripple Carry Adder

Ripple Carry Adder consists (RCA) of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder travel longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of ripple carry adder. The value of N increases, delay of adder will also increase in a linear way. Therefore, ripple carry adder has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area.

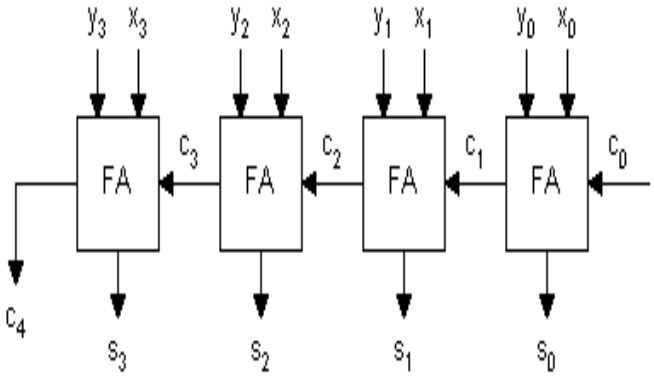

Fig.1 Ripple Carry Adder

3.3 Conventional Carry Select Adder

The conventional Carry Select Adder provides away to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance as shown in Fig.2. Once the original

value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional Carry Select Adder makes use of Dual ripple carry adder to generate the partial sum and carry by considering input carry C_{in}=0 and C_{in}=1, then the final sum and carry are selected by multiplexers.

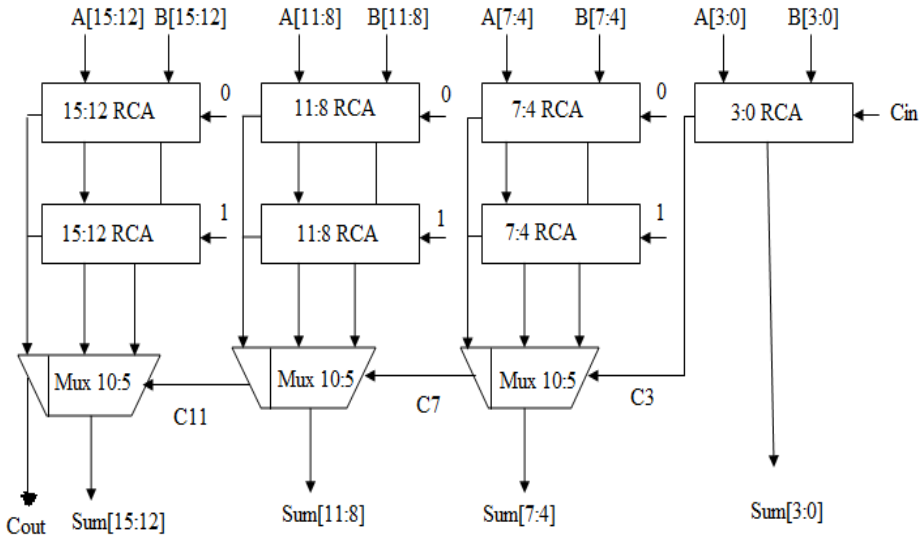

Fig.2 16-bit Conventional Carry Select Adder

3.4 Modified Conventional Carry Select Adder

In the Modified conventional Carry Select Adder basic idea of this work is to use Binary to Excess- 1converter (BEC) instead of ripple carry adder with C_{in}=1 in order to reduce the area and power as shown in Fig.3 and logic diagram using multiplexer is shown in Fig.4. Binary to Excess- 1converter (BEC) uses less number of logic gates than N-bit full adder structure. To replace N-bit ripple carry adder, an N+1 bit Binary to Excess- 1converter (BEC) is required.

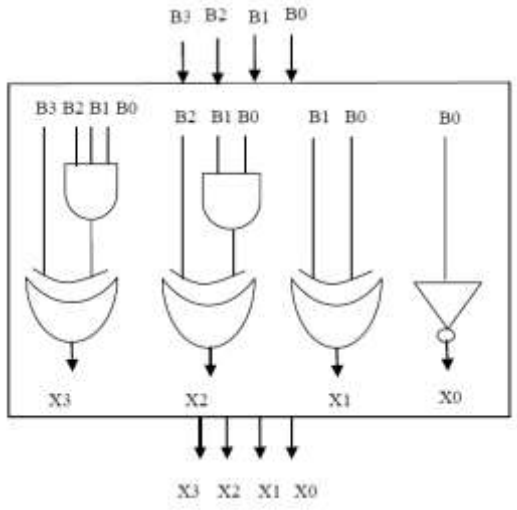

Fig.3 4-bit Binary to Excess-1 Converter

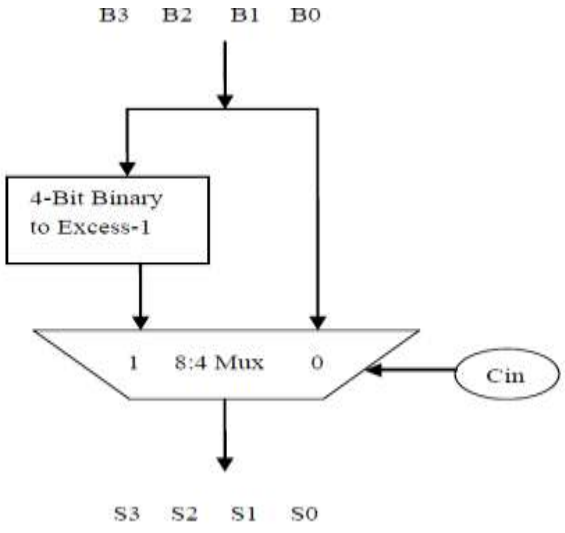

Fig.4 4-bit Binary to Excess-1 logic with 8:4 multiplexer

Table.1 Truth table of 4-bit Binary to Excess-1 logic

Binary	Excess-1
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Therefore Modified Conventional Carry Select Adder is shown in Fig.5 has low power and less area than conventional Carry Select Adder.

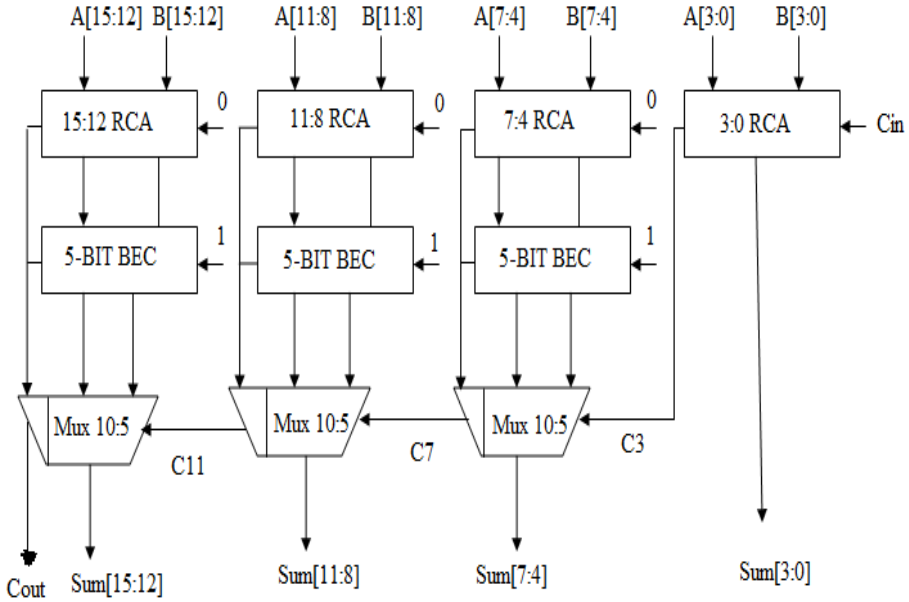

Fig.5 16-bit Modified Conventional Carry Select Adder

3.5 Regular SQRT Carry Select Adder

In regular Carry Select Adder there is only one RCA to perform addition of the least significant bits [1:0] as shown in Fig.6. The remaining bits, the addition is performed by using a two ripple carry adders in order to perform calculation twice one time with the assumption of carry being zero and other assuming carry one, then the final sum and carry are selected by the multiplexer (mux). Group 2 to group 5:- In a group, there are two RCA that receive the same data input but different cin. The upper adder for cin=0, the lower adder a cin=1. The cin=0, the sum and carry-out of the upper RCA selected and if cin=1, the sum and carry-out of the lower RCA is selected. The cin=0 used one half adder for the 1st bit of that RCA and another bits used full adder. The cin=1 used full adders.

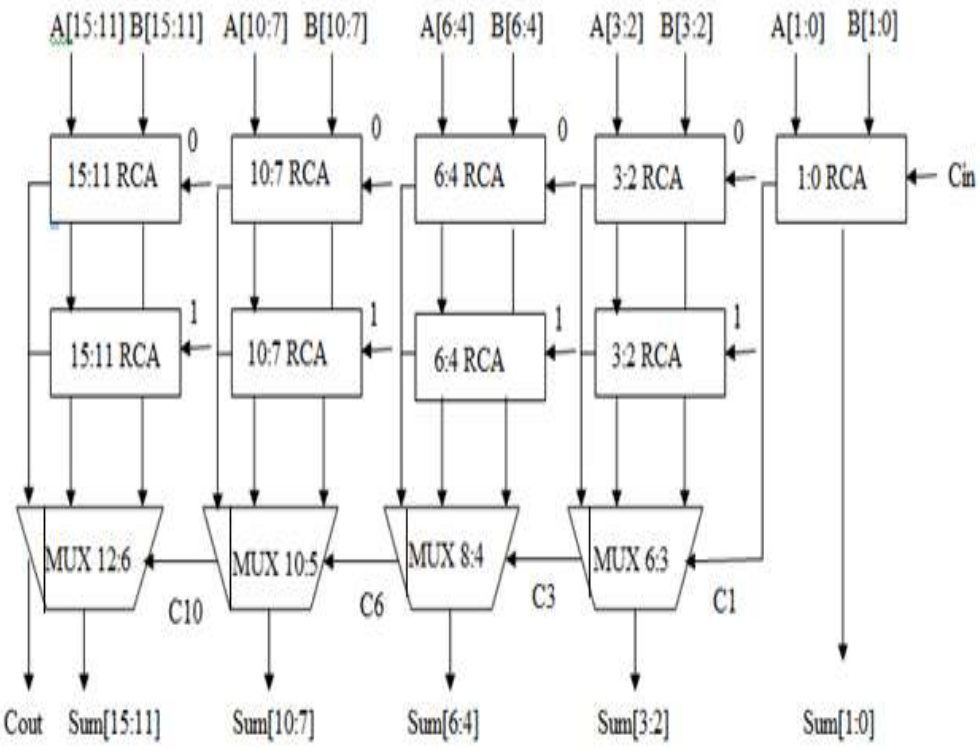

Fig.6 16-bit Regular Carry Select Adder

3.6 Modified Regular SQRT Carry Select Adder

This architecture is similar to regular 16-bit SQRT CSLA, the only change is that, it used binary to excess-1 converter (BEC) instead of RCA with c_{in}=1 in the regular CSLA to achieve lower area delay and power consumption as shown in Fig.7. The number of bits required for BEC is 1 bit more than the RCA bits. The modified SQRT CSLA is also divided into various groups. Each groups having the RCA, BEC and multiplexer. The XOR gate in BEC of modified CSLA is replaced with the optimize XOR gate in AOI. The optimize XOR gate is used in modified CSLA reduction in no of gates. The advantage of this logic comes from lesser number of logic gates. It has 5 groups of different size RCA. Group 1 contains 2-bit RCA which contains only one ripple

carry adder which adds the input bits, input carry and result, sum and carry. The 2 bit input of A and B and 1 bit input is c_{in}. In modified CSLA there is only one RCA to perform addition of the least significant bits [1:0].

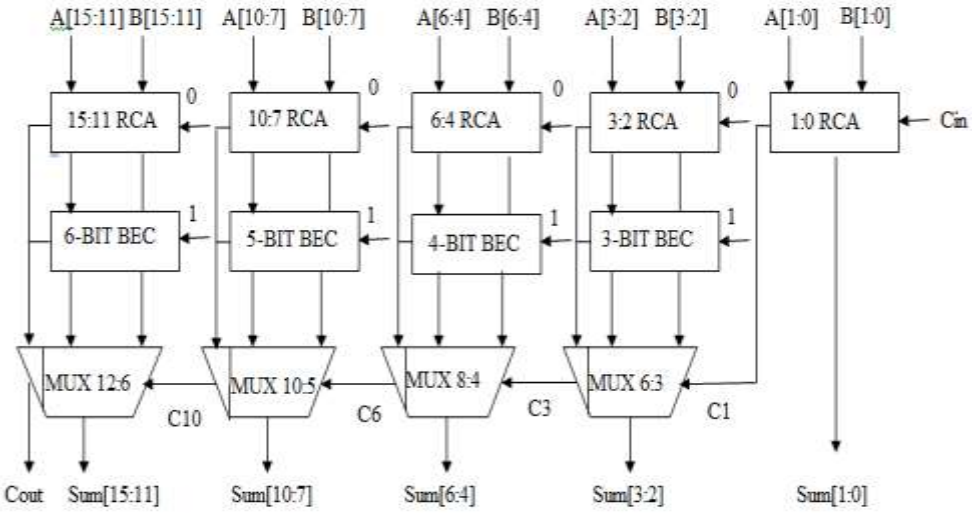

Fig.7 16-bit Modified Regular Carry Select Adder

IV PROPOSED CARRY SELECT ADDER

The Carry Select Adder has two units: 1) sum and carry generator unit (SCG) and 2) sum and carry selection unit. The SCG unit consumes most of the logic resources of CSLA and significantly contributes to the critical path as shown in Fig.8. Different logic designs have been suggested for efficient implementation of the SCG unit. The SCG unit of the conventional CSLA is composed of two n-bit RCAs, where n is the adder bit-width. The logic operation of the n-bit RCA is performed in four stages: 1) half-sum generation (HSG); 2) half-carry generation (HCG); 3) full sum generation (FSG); and 4) full carry generation (FCG). Suppose two n-bit operands are added in the conventional CSLA, then RCA-1 and RCA-2 generate n-bit sum (s0 and s1) and output-carry (c0out and c1out) corresponding to input-carry (cin = 0 and cin = 1).

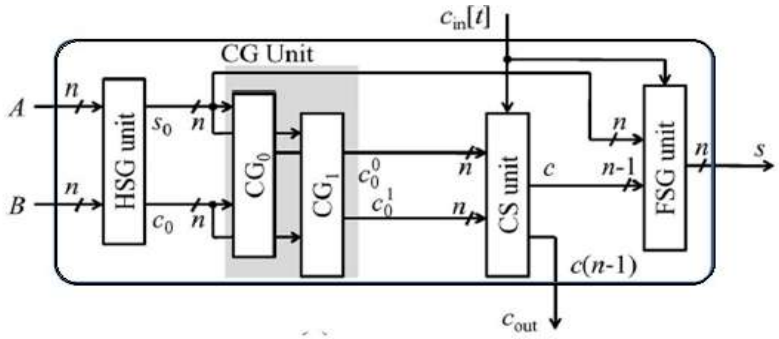

Fig.8 Proposed Carry Select Adder

The Fig.9 consists of one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n-bit operands (A and B) and generate half-sum word s0 and half-carry word c0 of width n bits each. Both CG0 and CG1 receive s0

and c0 from the HSG unit and generate two n-bit full-carry words corresponding to input-carry '0' and '1', respectively. The logic circuits of CG0 and CG1 are optimized to take advantage of the fixed input-carry bit.

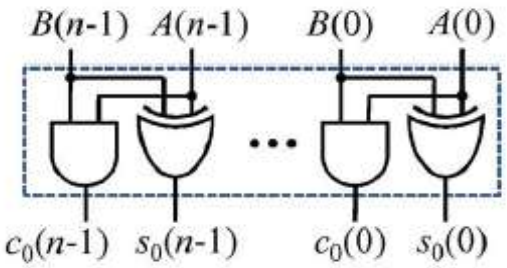

Fig. 9(a) HSG

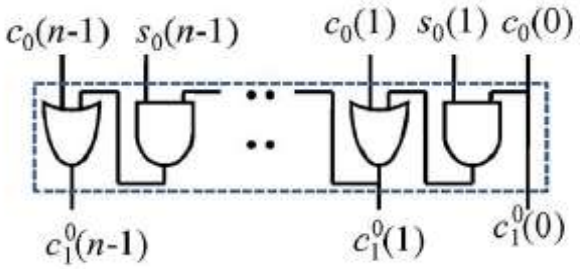

Fig. 9(b) Carry Generation CG0

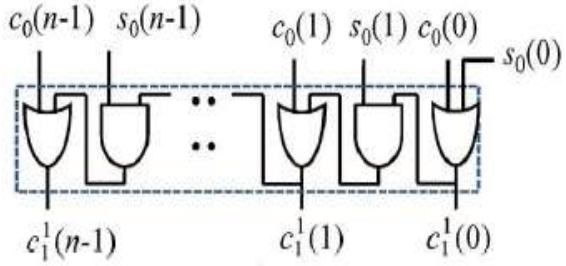

Fig.9(c) Carry Generation CG

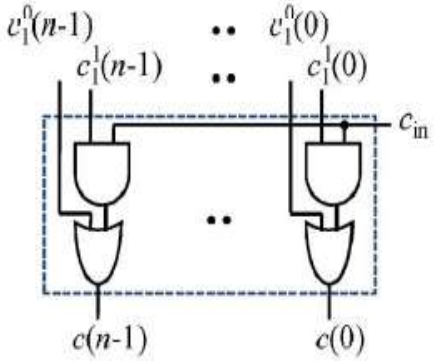

Fig.9(d) Carry Selection Unit

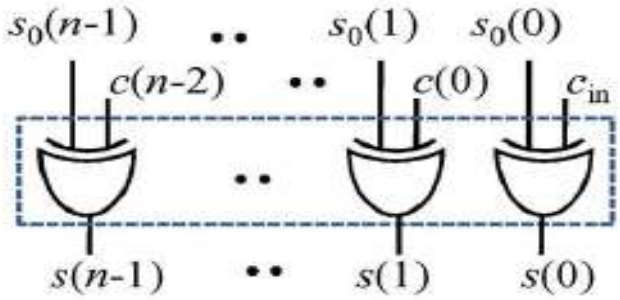

Fig. 9(e) FSG

This work has been developed using Xilinx tool. Table .2 shows the comparison between the various adders like conventional CSLA, Modified CSLA, regular SQRT CSLA, modified SQRT CSLA and proposed CSLA for 8-bit, 16-bit, 32-bit. The comparison is taken for parameters are area, delay and power. Fig.8 shows that the proposed CSLA has less number of gates and hence less area.

Table.2 Comparison of Adders for Area, Delay, and Power

WORD SIZE	ADDER	AREA(GATE COUNT)	DELAY (ns)	POWER (mW)
8-bit	Conventional (Dual RCA)	204	15.51	96.57
	Modified (with BEC)	165	16.76	89.57
	Regular SQRT (Dual RCA)	153	12.45	199
	Modified SQRT(with BEC)	140	13.50	165
	Proposed CSLA	96	6.60	25
16-bit	Conventional (Dual RCA)	520	20.11	120
	Modified (with BEC)	410	19.81	94.63
	Regular SQRT (Dual RCA)	370	17.15	350
	Modified SQRT(with BEC)	310	18.77	240
	Proposed CSLA	192	11.90	25
32-bit	Conventional (Dual RCA)	1040	34.12	110
	Modified (with BEC)	814	30.01	87.14
	Regular SQRT (Dual0 RCA)	710	27.18	530
	Modified SQRT(with BEC)	740	33.19	420
	Proposed CSLA	520	24.96	75

V CONCLUSION

The proposed approach will avoid the unwanted addition and thus minimize the power dissipation as well as the design structure of the CSLA designed by using reduced gates gives the low power consumption when compared to use of ripple carry adders in carry select adder architecture. Therefore the total power consumption, area and delay will be reduced which gives the high speed addition operation and good performance of the system.

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