NOVEL REVERSIBLE 16*16 WALLACE TREE MULTIPLIER USING TSG GATES

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ABSTRACT

*In the current era, reversible logic has emerged as a potential computing model as it afford less power consumption which makes it applicable for low power CMOS design, optical computing, quantum computing and nanotechnology. This paper describes about the implementation of reversible logic for ALU operation via TSG gate and compressor. It utilizes a 4*4 reversible gate called TSG gate which can work independently as a reversible full adder, unlike the full adder circuit designed from conventional set of gates such as AND, OR and NOT which are not reversible. A Novel reversible 4:2 compressor is also designed and used to build a novel 16*16 Wallace Tree Multiplier. With the inference of this paper, it is proved that full adder, reversible 4:2 compressor and the multiplier architectures designed using the TSG gate are beneficial than their equivalents available in literature, in terms of number of garbage outputs and reversible gates. Thus, this paper provides a foundation to build more complicated circuits without much power dissipation.*

Keywords: Quantum Computing, Reversible Logic, Reversible Gates, TSG Gate, Wallace Tree Multiplier.

I. INTRODUCTION

This section provides contextual meaning of reversible logic and purpose behind it.

1.1 Descriptions

With the increasing complexity of CMOS VLSI design, power dissipation has become the main area of concern in VLSI design. In 1961, it has been demonstrated by the researcher called Landauer that circuits and systems built using irreversible gates will result in power consumption and energy dissipation due to information loss in the form of bits [1]. It is proved that the loss of one bit of information dissipates kT*log2 joules of heat energy where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [1]. Further in 1973, Bennett showed that zero power dissipation is possible in the logic circuits only if it is composed of reversible logic

gates since the amount of energy dissipated in a system will hold a direct relationship to the number of information bits erased during computation[2]. The copy of state of the output must be present at all times which can be obtained by using the reversible logic. The voltage-coded signals have energy of $Es= 1/2CV^2$, and this energy get dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process [22]. Reversible computation in a system can be performed only when the system comprises of reversible gates. The field of quantum computing also uses reversible logic. All quantum gates are reversible [12]. Reversible circuits can generate unique output vector (Ov) from each input vector (Iv), and vice versa, that is there is a one-to-one mapping between the input and output vectors. Thus, an nXn reversible gate can be represented as:

$$Iv= (I1,I2,I3,\ldots\ldots\ldots In)$$

$$Ov= (O1,O2,O3,\ldots\ldots\ldots On)$$

Classical logic gates are irreversible since input vectors states cannot be uniquely reconstructed from output vector states. There is a number of existing reversible gates such as Fredkin gate [3,4,5], Toffoli gate (TG) [3,4] and New gate (NG) [6].

1.2 Purpose of Reversible Logic

Reversible logic are of high interest in low power CMOS design [10], optical computing [11], quantum computing [12] and nanotechnology [13]. The most remarkable application of reversible logic lies in quantum computers. A balanced reversible function has half of minterms with value 1 and another half with value 0. In a n output reversible gates, the output vectors are permutation of numbers 0 to 2n-1.

1.3 Major Concern In Reversible Logic

The input that is added to an nxk function to make it reversible is called Constant input(CI) and the outputs of the reversible circuits that are not used are called as Garbage outputs(GO). These garbage outputs are just used to preserve the circuit's reversibility. Quantum cost(QC) refers to the cost of the circuit in terms of the cost of a primitive gate. These parameters i.e. CI,GO,QC, have to be reduced while designing a reversible circuits. Some of the major problems with the reversible logic synthesis are the fanouts cannot be used and also feedback from gate output to input is not permitted. However fanout in reversible circuits is achieved using additional gates. A reversible circuit design should have minimum number of reversible logic gates.

II. PROPOSED CONCEPT IN REVERSIBLE LOGIC

This paper focus on the application of new reversible 4*4 TSG gate [23,24]. It can work singly as the reversible full adder. A novel reversible 4:2 compressor is also designed from the proposed TSG gate. In addition, the optimized

adder and 4:2 compressors are used to design the novel 16*16 reversible Wallace tree multiplier. It is observed that TSG gate achieves minimized garbage outputs and minimized reversible gates, leading to high speed and low power reversible circuits. The reversible circuits proposed and designed in this work form the basis for an ALU of a primitive quantum CPU.

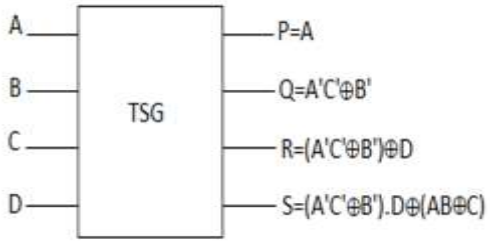

Figure 1. Proposed TSG gate

2.1 Proposed 4*4 Reversible Gate

The journalists proposed a 4*4 one through reversible gate called TS gate (TSG) which is shown in the Figure 1. It can be noted that input pattern corresponding to a particular output pattern can be uniquely determined. The proposed TSG gate is capable of implementing all Boolean functions and can also work as a reversible full adder. Figure 2 shows the implementation of the proposed gate as a reversible Full adder

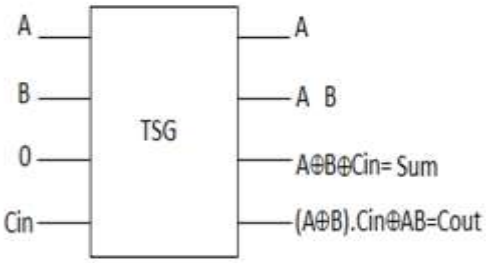

Figure 2. Proposed TSG gate as a full adder

A number of reversible full adders were proposed in [6,7,8,9]. The reversible full adder circuit in [6] requires three reversible gates(two 3*3 new gates and one 2*2 Feynman gate) and produces three garbage outputs. The reversible circuit in [7,8] requires three reversible gates (one 3*3 new gate, one 3*3 Toffoli gate and one 2*2 Feynman gate) and produces two garbage outputs. The adder circuit in [9] uses five reversible Fredkin gates and produces five garbage outputs. The proposed full adder circuit using TSG in Figure 2 uses one reversible gate that is TSG gate which produces two garbage outputs which shows that the TSG gate circuit is better than the full adder designs of [6,7,8,9] . Various full adder circuits are compared and it is given in Table 1

Table I . A Comparison of Various Reversible Full-Adder Circuits

	Number of Gates	Number of Garbage Outputs	Unit Delay
Proposed Circuit	1	2	1
Existing Circuit[6]	3	3	3
Existing Circuit[7,8]	3	2	3
Existing Circuit[9]	5	5	5

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III. REVERSIBLE 4:2 COMPRESSOR

Weinberger in 1981 introduced 4:2 compressor and he called it as "4-2 carry save module"[16]. The 4:2 compressor structure actually compresses the five partial product bits into three in which four of the inputs are coming from the same bit position of the weight j while one bit is fed from the neighboring position j-1 (known as carry-in), The output of the 4:2 compressor consists of one bit in the position j and two bits in the position j+1. The structure of 4:2 compressor is shown in the figure 3

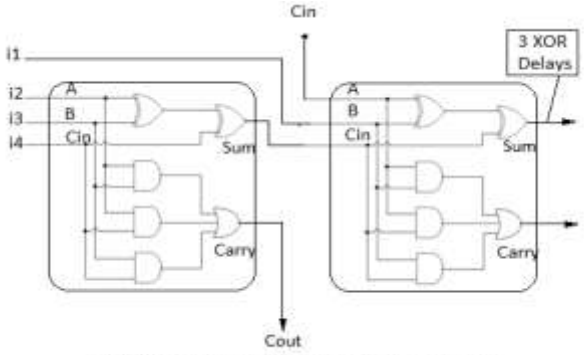

Figure 3. Logic Diagram of 4:2 Compressor

The efficiency of such a structure is higher since it reduces number of partial product bits by one half at each stage. The delay of 4:2 compressor is 3 XOR gates in series making it more efficient than using 3:2 counters i.e. full adder in a regular Wallace tree and has important feature that the interconnections between 4:2 cells follow more regular pattern than in the case of the "Wallace tree" [17,18,25]. In this paper, the 4:2 compressor is also proposed as shown in figure 4. Here, the reversible 4:2 compressor is designed from two TSG gates. The block diagram of 4:2

compressor is shown in Figure 5. Table II shows the comparison results of the 4:2 compressor using TSG with its implementation using existing reversible full adders.

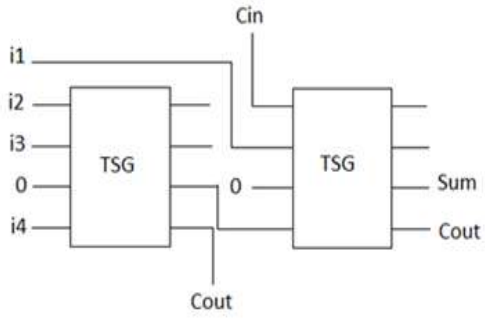

Figure 4. Proposed Reversible 4:2 Compressor designed using TSG Gate

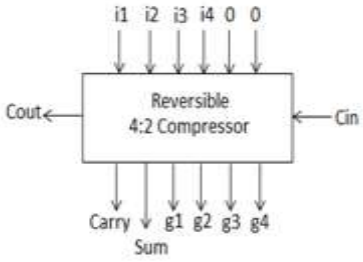

Figure 5. Block Diagram of Reversible 4:2 Compressor

Table II. A Comparison of 4:2 Compressors using Various Full adder Circuits

	Number of Reversible Gates	Number of Garbage Outputs	Unit Clock Cycle
Full Adder Using TSG	2	4	2
Existing Circuit[6]	6	6	6
Existing Circuit[7,8]	6	4	4
Existing Circuit[9]	10	10	10

IV. REVERSIBLE WALLACE TREE

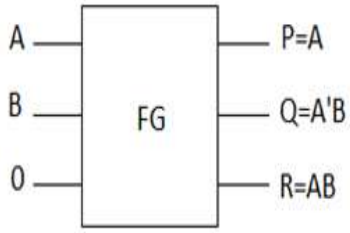

Figure 7. Use of Fredkin gates to Generate Partial Products in Parallel

A multiplication operation consists of three stages: partial products generation stage, partial product addition stage, and the final addition stage [19,20,21].The second stage is the most important and determines overall speed of the multiplier. In high speed designs, the Wallace tree construction method is usually preferred to add the partial

products in a tree-like fashion. The Wallace tree is fast since the critical path delay is proportional to the logarithm of the number of bits in the multiplier.

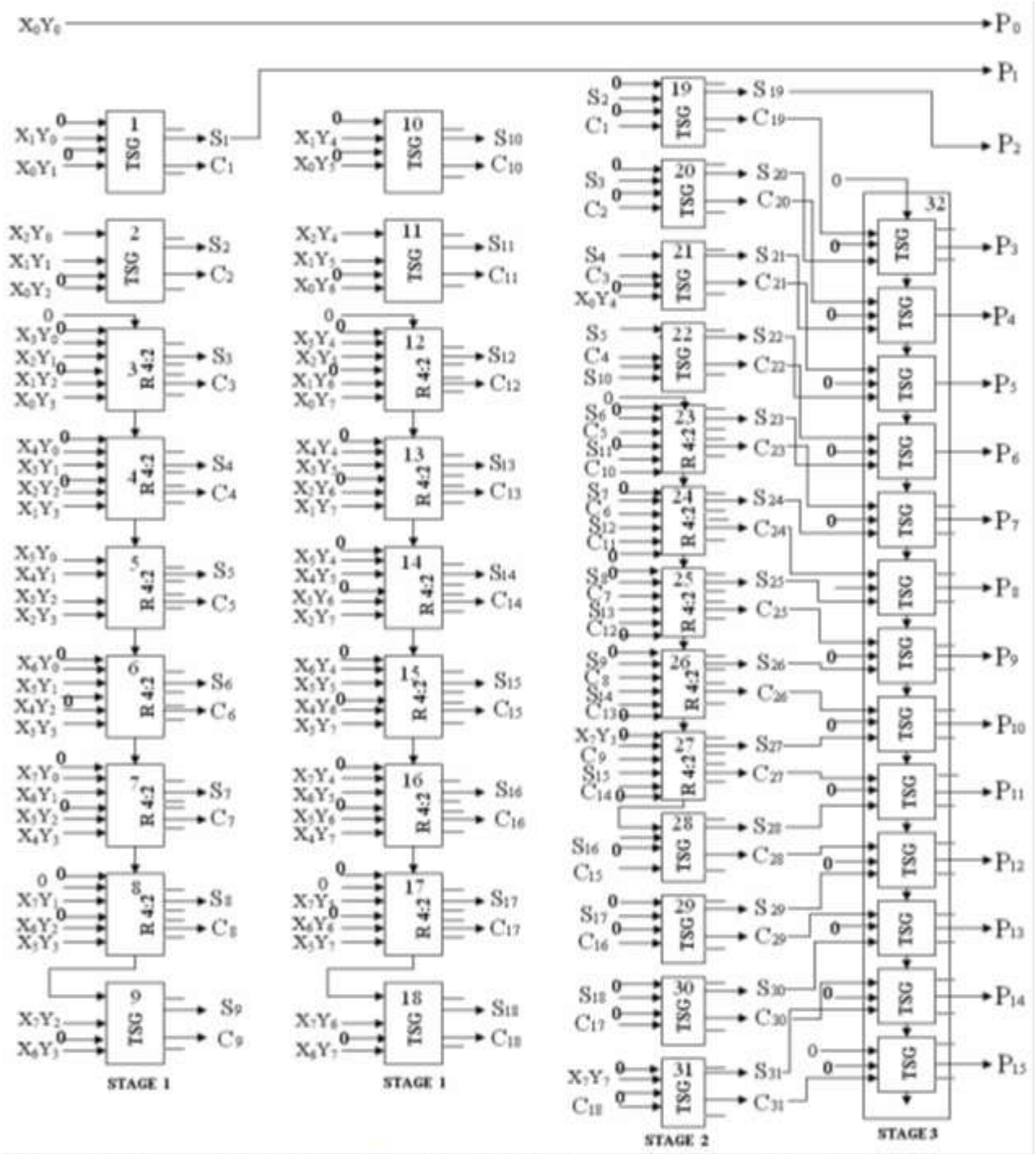

Figure 6. Reversible 8x8 Wallace Tree Multiplier using Reversible 4:2 Compressor

4.1 Reversible Wallace Tree Construction

The Figure 6 shows the circuit diagram of reversible 8x8 Wallace tree multiplier using reversible 4:2 compressor. This paper proposes reversible 16x16 Wallace tree multiplier using the reversible TSG gate, for the multiplication of two 16 bit numbers whose answer will be in 32 bit form. The method to construct the Wallace tree considers all the bits in each four rows at a time and compress them in an appropriate manner. The Wallace tree uses 4:2 compressor and full adders to compress the partial products tree. The proposed architecture can be generalized for nxn bits. The reversible full adder and 4:2 compressor designed from the reversible TSG gate are used as the basic building blocks for the design of 16x16 Wallace tree multiplier.

The generation of all partial products of the multiplication can be done in parallel by using Fredkin gates (for ANDing the bits of the multiplier and multiplicand) as shown in Figure 7.In Stage 1, as shown in Figure 6, the partial products are added using 4:2 compressors, full adders and half adders, the S and C generated of all the blocks are arranged according to their weights. In the Stage 2, the reduced partial products are again added using 4:2 compressors, full adders and half adders. The result obtained in the stage 2 is added using a parallel adder designed from TSG gates in Stage 3 to generate the product bits P0,P1,…..P31,P32.

4.2 Evaluation of the proposed Wallace Tree Multiplier

The proposed reversible 16x16 Wallace Tree Multiplier is designed from the reversible TSG gate. This is the first attempt in literature to design the reversible 16x16 Wallace Tree Multiplier. The novelties lies in the introduction of reversible TSG gate and its implementation for designing the adder and compressor, which are latter used to design reversible Wallace Tree Multiplier. There seems to be no existing counterpart in the literature and hence no comparative study is done. It has been already proved in the earlier sections that the adder and the compressor designed from the TSG gate are the most optimized one, thus making the overall architecture of the Wallace Tree Multiplier as the most optimal one.

V. CONCLUSION

The focus of this paper is the application of a new reversible 4*4 TSG gate to design the components of a primitive quantum/ reversible ALU. The TSG gate is used to design the 4:2 compressor and a optimized adder which are later used to build a novel reversible 16x16 Wallace Tree Multiplier. It is proved that the adder and 4:2 compressor and multiplier architecture designed with the TSG gate are efficient than the their counterparts, in terms of number of reversible gates and garbage outputs, resulting in the low power consuming as well as the high speed reversible circuits. All the proposed architectures are analyzed in terms of technology independent implementations. The proposed circuit can be used for building large reversible systems. Thus, this paper provides a threshold to build more complicated reversible systems.

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