CONVOLUTION ENCODING AND VITERBI DECODING BASED ON FPGA USING VHDL

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ABSTRACT

In digital electronics,the error correcting techniques plays important role in communication channel.convolutional encoding is an FEC(forward error correcting)technique used for correction of errors at the receiver.viterbi algorithm is decoding technique of convolutional codes,which is having good correcting capability on very noisy channels.In this paper ,we represent a PROASIC 3 FPGA(field programmable gate array)efficient implementation of viterbi decoder and synthesis can be done using ACTEL LIBERO v8.3 with the constraint length 3 and code rate 1/2.

Keywords: Covolutional Encoder, PROASIC 3, Viterbi Decoder, FPGA, VHDL.

1. INTRODUCTION

In real communication,errors are introduced in transmitting message.Data traffic and voice transmitted by wireless deices are introduce to fading channel and noisedue to error added in data stream. Channel coding refer signal transformation to improve the communication performance.In channel coding ,it involve the addition of bis to actual information bits for transmission,this reduces the error probability in information bit at receiver.Channel coding is divided into two forms that is block code and convolution code.In order to maintain data,data is normally encoded at the transmitter and decoded at the receiver. It helps in error correction for data transmission.

1.1 Previous Work

Convolution coding and viterbi decoding with various block length and code rate are implemented in Spartan3 FPGA using MATLAB and Xilinx.

1.2 Proposed Work

We are performing convolution encoding and viterbi decoding by onsidering constraint length 3 in Proasic3 FPGA kit using actel liberov8.3 software.It is low cost device and compatible.

II. COVOLUTION ENCODER

Convolution encoder is described with the help of state table, state diagram and trellis diagram. In convolutional encoder n is number of input bits, k=3 is constraint length.Input is shifted bit by bit in memory register as m0 and m1.output is calculated from generator polynomial by modulo-2 addition.

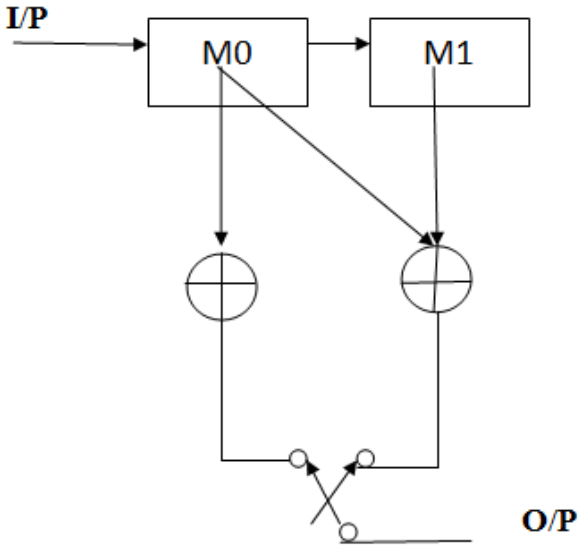

Fig 2.1 Convolution Encoder

$O1 = I/P \oplus m0$ …….. (1)

$O2 = m0 \oplus m1$ …… (2)

Table 2.1 State table

Input bit	Present state (m0m1)	Next state (m0m1)	Output bits (O1O2)
0	00	00	00
1	00	10	10
0	01	00	01
1	01	10	11
0	10	01	11
1	10	11	01
0	11	01	10
1	11	11	00

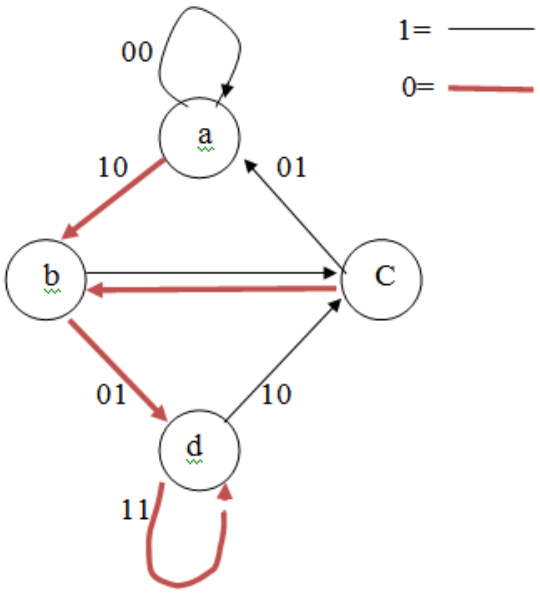

Fig 2.2 State Diagram

III. VITERBI DECODER

Viterbi decoding is developed by Andrew J. in 1963.This is first dominant technique for convolutional codes rather than threshold decoding and sequential decoding.It has highly satisfactory bit error performance.It has high speed of operation.Viterbi decoding has fixed decoding timeIt has well suited to network decoder implementation.The viterbi decoding algorithm is used in decoding Trellis coded modulation .The block diagram of viterbi decoder is shown by following fig 3.1

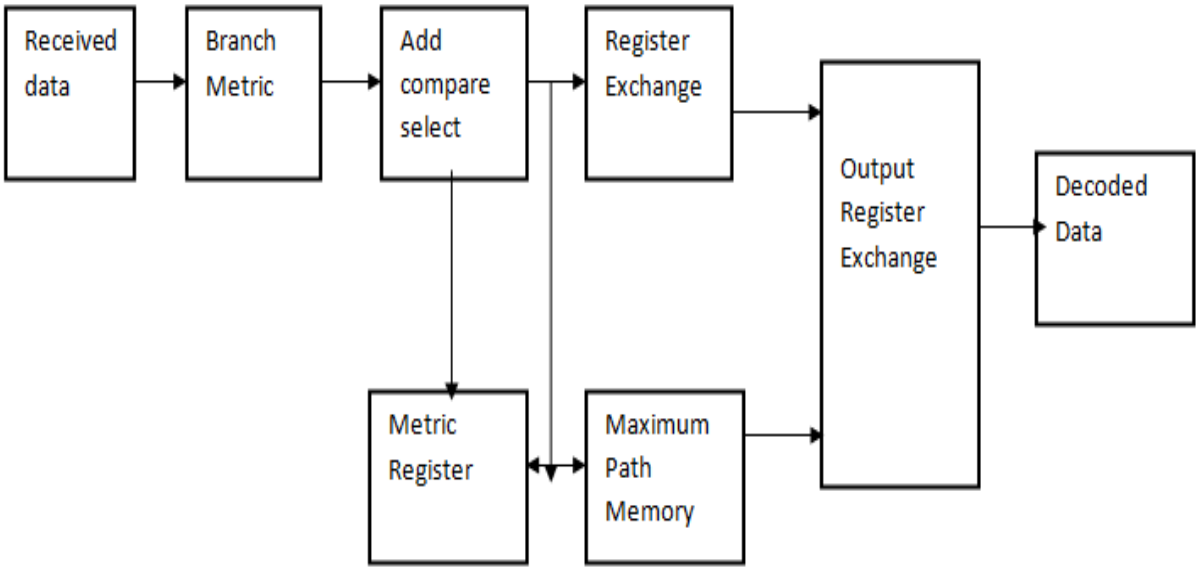

Fig 3.1 Block Diagram of Viterbi Decoder

3.1 Branch Metric Unit

Branch metric unit is the first unit of viterbi decoder.Here the received data symbols are compared to ideal outputs of encoder from the transmitter and branch metric is calculated.Hamming distance and Euclidean distance is used for branch metric computation.

3.2 Register Exchange

This unit is trace-back process or register exchange,where the survivor path and output data are identified .Trace-back and register exchange is important technique used for the path history management in chip designs of viterbi decoders.

3.3 ACS (Add Compare Unit) Unit

A new value of the state matrics has to be computed at each time instant.In other words ,state metrics have to be updated every clock cycle.Therefore ACS unit is the module that consumes the most power and area.The new branch metrics are added to previous state metrics to form the candidates for new state metrics.Comparision can be done by using subtraction of two candidates state metrics and the MSB of the difference points to larger one of two.

3.4 TRELLIS DIAGRAM

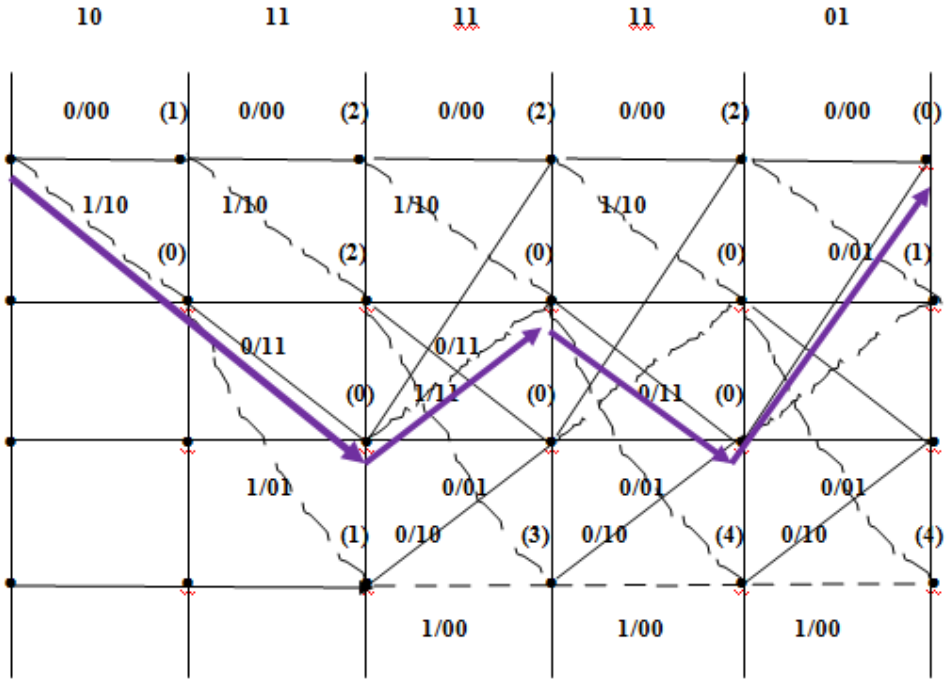

Fig3.4.1: Viterbi Algorithm for Trace Back Path

Decoded code vector is 10100

IV. PROGRAMMABLE DEVICES

1. SPLD (PAL,PLA,and ROM) and CPLD are relatively small and useful for simple logic devices upto about 20000 gates but FPGA can handle larger circuits upto 100000 gates.
2. Power consumption in CPLD is more (0.5W-2W static and 0.5W-4W dynamic) than in FPGA (0.1w-2w).
3. FPGA provide logic blocks,I/O blocks,interconnection wires and switches. FPGA is a array of small logic blocks surrounded by input output.It has very low static and dynamic power consumption

V. APPLICATION

1. In geostationary satellite communication the combination of viterbi decoding and RS (Reed-Soloman) coding is used.
2. Viterbi decoders are used in Digital communication, lso in wired/wireless communication,voice-band data communicatonand HDTV.
3. Viterbi decoders are used in mobile communicatin where the available power and bandwidth are limited.
4. Viterbi decoders are used in mass storage media such as hard disk,magnetic recording channel,CD-ROM and DVD.

VI. CONCLUSION

In this paper we presented implementation of the Viterbi Decoder with constraint length 3 and code rate ½.We have tested the functionality of the Viterbi Decoder Code implemented in FPGA by designing a Test Bench for performing Error Detection and Correction.We have implemented Viterbi Decoder to improve the accuracy of received information at the receiver.

REFERENCES

[1] Yin Sweet Wong, Wen Jian Ong, Jin Hui Chong, Chee Kyun Ng, Nor Kamariah Noordin," Implementation of Convolutional Encoder and Viterbi Decoder using VHDL"in Proceedings of 2009 Student Conference on Research and Development (SCOReD)

[2] Ms.G.S. Suganya, Ms. G.kavya," RTL Design and VLSI Implementation of an efficient Convolutional Encoder and Adaptive Viterbi Decoder"in International conference on Communication and Signal Processing, 2013.

[3] J.Tulasi, T.Venkata Lakshmi & M.Kamaraju," FPGA Implementation of Convolutional Encoder And Hard Decision Viterbi Decoder"in International Journal of Computer & Communication Technology (IJCCT), ISSN 2012.

[4] S.S. Poduttwar,H.M. Baradkar, V.R.Thakare," Convolution Encoder Implementation using FPGA'' in processding of International Journal of Applied Information Systems (2249 – 0868) National Level Technical Conference "X-PLORE 13"

[5] Devendra Made, Asst. Prof. R.B. Khule, Dipak Iwanate," Implementation of Adaptive Viterbi Decoder''in International Journal of Engineering Trends and Technology-Volume4Issue2-2013