SIMULATION OF MULTILEVEL INVERTER EMPLOYING CASCADED 3-PHASE TRANSFORMERS WITH COMMON-ARM CONFIGURATION USING DIFFERENT SWITCHING & PWM SCHEMES

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ABSTRACT

In multilevel inverter development for 3-phase applications, total number of transformer in the circuit can be reduced by using of cascaded 3-phase transformer circuit instead of single-phase transformer circuit. In the scheme, total number of switching components in the circuit is still a drawback to achieve lower cost and smaller size of the inverter compared with conventional multilevel inverter. This paper includes a challenging method to reduce total switching components in the multilevel inverter by adopting common-arm structure. In this paper, a common-arm is applied to the 3-phase cascaded H-bridge multilevel inverter circuit. By inserting of a common-arm structure in the circuit, we will demonstrate a minimization method of the switching components in the 3-phase cascaded H-bridge multilevel inverter circuit. To verify the validity of the proposed approach, here different pulse width modulations with different switching schemes have been applied.

Keywords: Multilevel Inverter, Cascaded 3-Phase Transformer, Common Arm Configuration

I. INTRODUCTION

In many industrial fields, multilevel inverters have been received great attention. The most valuable advantage of them is to synthesize high voltage outputs with low switching frequency. Hence they are considered as a substitute of conventional PWM inverters. Among multilevel inverters, cascaded H-bridge multilevel inverter is consisted of low voltage H-bridge modules connected in series, and each module has an independent dc link. Therefore, the cascaded H-bridge multilevel inverter scheme has a higher flexibility in a module configuration than conventional method. The inverter scheme has been successfully applied for high power applications. However, the scheme has a weakness in dc link cell charging which is performed independently. In order to overcome the drawback, several modifications with a single dc source using cascaded transformers have been reported. The formatter will need to create these components, incorporating the applicable criteria that follow. Among the researches, have proposed better circuit configurations of the conventional cascaded H-bridge multilevel inverter. In those papers, a single dc input source is required to operate a cascaded transformer which is mainly operated in low frequency range. Multilevel output voltage levels can be easily achieved by the cascaded H-bridge multilevel inverter scheme which has much less electrical components than the conventional method. However, if the scheme is applied to the 3 phase application, final electrical circuit is occupied by many electrical components such as switches, transformers, and other components to operate. To solve the problem, an approach implemented by 3- phase transformers instead of single-phase transformers. The paper has

presented that the 3-phase transformer scheme can decrease the number of transformers, but it still needs more efforts to reduce the number of switches. In this paper, a common-arm is applied to the 3-phase cascaded H-bridge multilevel inverter circuit. By inserting of a common-arm structure in the circuit, we will demonstrate a minimization method of the switching components in the 3-phase cascaded H-bridge multilevel inverter circuit. To verify the validity of the proposed approach, here different PWM techniques have been applied using different PWM switching schemes.

II. PROPOSED CHB-MLI WITH COMMON ARM CONFIGURATION

2.1 Conventional Cascaded H-Bridge Multilevel Inverter

If we have a conventional cascaded H-bridge multilevel inverter consisted of four H-bridge cells, the output voltage becomes the sum of the terminal voltage produced by each H-bridge cell which is powered by its independent dc input source. The peak value of the output voltage is always less than four times of an input dc source voltage. Therefore an auxiliary voltage-boosting circuit is required to get the required voltage. As an alternative, we can consider a boost type H-bridge multilevel inverter which is operated by a cascaded transformer. Every H-bridge cell is parallelly connected to a dc input source, and the secondaries of all transformers are connected in series. Output voltage of the conventional cascaded H-bridge multilevel inverter can be obtained by the sum of terminal voltages of the H-bridge cells. Usually, the output voltage can be controlled by the voltage of dc input source and the turn ratio of each transformer. The transformer's mechanical separation between primary and secondary coils produces galvanic isolation between an input source and output loads in the multilevel scheme. However, when we like to modify the circuit configuration to 3-phase scheme, the multilevel inverter scheme requires more transformers since each phase is generated by a transformer.

2.2 Cascaded H-Bridge 3-Phase Multilevel Inverters Using 3-Phase Transformers

Fig 2.1 shows a circuit configuration of a 3-phase cascaded H-bridge multilevel inverter. It consists of a single dc input and 3-phase transformers. By using 3-phase transformer scheme, the number and the volume of transformers can be reduced when we compared with single phase transformer. Consequently, total cost of the system can be reduced due to the less components and smaller volume of the system.

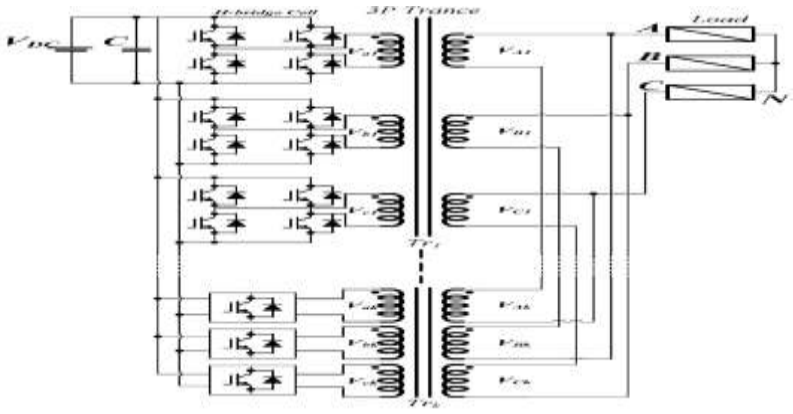

Fig 1.Cascaded H-Bridge Multilevel Inverter Employing 3-Phase Transformers

The primary of each transformer is connected to H-bridge module so as to synthesize V_{DC}, 0, and $-V_{DC}$. The secondary of the transformer is connected in series to pile output level up. Each phase output is delta-connected to get rid of the 3rd harmonic component. 3-phase approach described in Fig 1 is an effective and economical circuit configuration to synthesize multilevel output voltage. The circuit configuration has an advantage in

utilization rate of transformer and it can decrease the system volume by using 3-phase transformers compared with single-phase transformers. In addition, the system has a function of a general switching scheme whose operating frequency is equal to that of fundamental. It means that the system can minimize switching losses. Unfortunately the system still requires mass of switching components to operate it.

For example, if the system has five 3-phase transformers as shown in Fig 1, the system has 60 switches. To reduce switching components in the 3-phase cascaded H-bridge multilevel inverter in Fig 1, we apply a common-arm scheme to the circuit which has five 3-phase transformers.

2.3. Common Arm Configuration Technique

As shown in Fig.2 one extra arm of an H-bridge which decides polarity of each phases connected in common. Because the arms are connected in common, 24 switches can be removed from Fig 1. If k number of 3-phase transformers is used, removable number of switches (p) from Fig 2 is calculated as $p=6(k-1)$ (1)

When we design the 3 phase inverter with Intelligent Power Module (IPM) or Insulated-gate Bipolar Transistor (IGBT) module which has 6 switching devices, the inverter requires 10 switching modules.

If we remodel the 3 phase inverter with the proposed method described in Fig.2, the inverter is composed of 5 switching modules which have same current rating as conventional one, and 1 common arm switching module which has 5 times current rating than conventional one. That is, in the circuit configuration, current ratings of

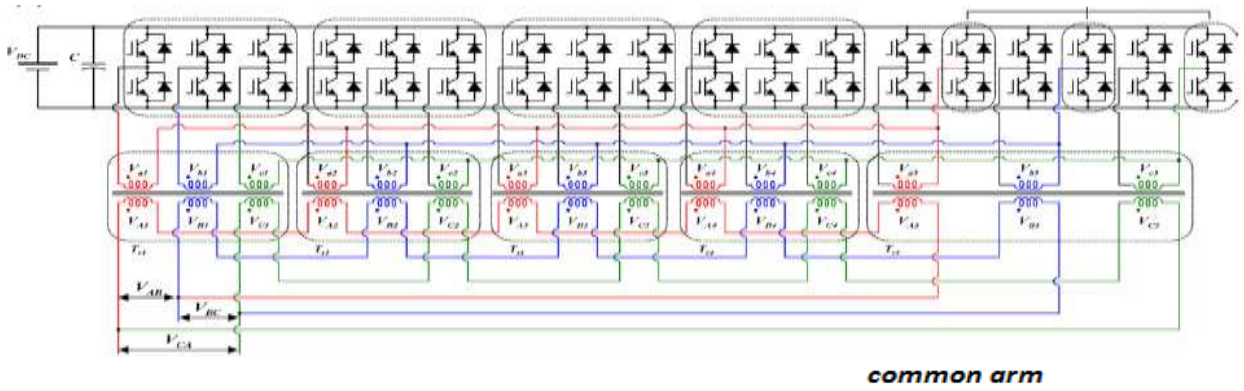

Fig 2.1 Proposed MLI Using Common Arm Configuration

common-arm switches become much higher than other switches. The smaller number of switching component reduces total cost of the system when we compare cost between 5 conventional switching modules and a 5 times current rating common arm switching module. An increase of current rating in a switching device is not directly proportional to that of the cost and size.

Moreover, this common arm method has a merit to reduce the current protection circuit. In the conventional method, we need more than one current protection circuit to prevent over-current on each switching module. However, with the proposed method, we need only one current protection circuit on the common arm switching circuit since the current is flowed through the common arm. In addition, it can decrease the number of gating drivers and the size of overall system by decreasing the number of switches.

From Fig.2.1, primary of each phase is connected to a half bridge and a common-arm. Fig2.2 is a simplified representation of Fig .2.1. Since the secondary of each phase is series-connected to generate V_{AS}, V_{BS}, and V_{CS}, it can be considered as a single-phase; therefore, it can be expressed independently.

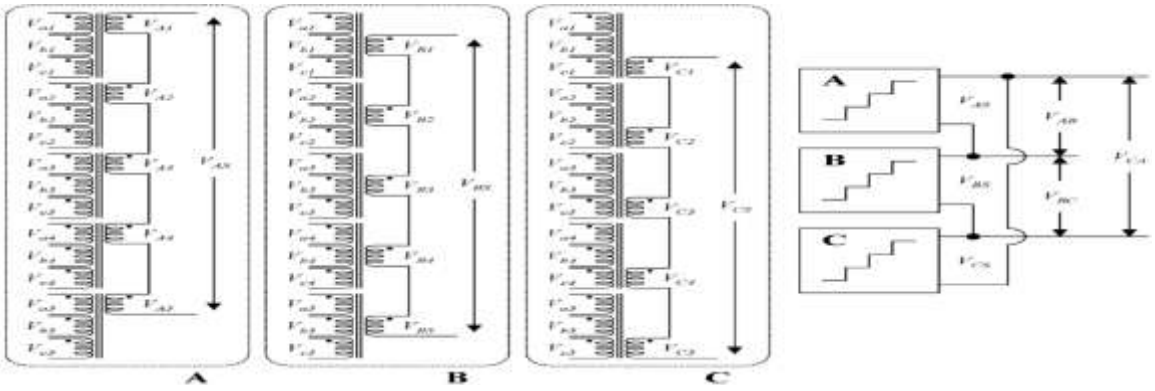

Fig.2.2 Simplified Structure of the Proposed Multilevel Inverter with Five 3-Phase Transformers

In Fig.2.2, V_{ak}, V_{bk}, andV_{ck} meanthe primary phase voltage of kth transformer. V_{Ak}, V_{Bk}, and V_{Ck} are the secondary phase voltage of each transformer. Hence, the relation between the primary and the secondary voltage of the transformer is given as

$$\begin{bmatrix} V_{Ak} \\ V_{Bk} \\ V_{Ck} \end{bmatrix} = \frac{T}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix} \quad (2)$$

where T is the transform ratio (n2/n1) between the primary and the secondary of the transformer.

If each primary voltage is balanced in three phases, the sum of each phase voltage becomes zero. However, it is often unbalanced because the primary of each transformer is connected to independent bridge cell generating VDC, 0, and −VDC. As shown in Fig .3, each phase voltage is connected in series; therefore, the line voltage V_{AB}, V_{BC}, and V_{CA} can be written by

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} V_{AS} \\ V_{BS} \\ V_{CS} \end{bmatrix} = \begin{bmatrix} V_{A1} + V_{A2} + \cdots + V_{Ak} \\ V_{B1} + V_{B2} + \cdots + V_{Bk} \\ V_{C1} + V_{C2} + \cdots + V_{Ck} \end{bmatrix} \quad (3)$$

By applying Eqs. (2) & (3), the line voltage can be expressed as

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \frac{T}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{aS} \\ V_{bS} \\ V_{cS} \end{bmatrix} \quad (4)$$

Above formula means that the primaries are connected in series, but actually the primary voltages of the transformers are originated from the same dc source; therefore it cannot be connected in series. It just means a virtual sum of the input dc sources.

III. PULSE WIDTH MODULATION SCHEMES

3.1 Pulse Width Modulation (PWM) Scheme

The reason for using PWM techniques is that they provide voltage and current wave shaping customized to the specific needs of the applications under consideration. By using PWM techniques, the frequency spectra of input waveforms can be changed such that the major non-fundamental components are at relatively high frequency and also to reduce the switching stress imposed on the power switching devices. Most PWM is generated by comparing a reference waveform with a triangular carrier waveform signal. However, the reference waveform may come in various shapes to suit the converter topology, such as sine wave and distorted sine wave. A sinusoidal waveform signal is used for PWM in DC to AC converter where it is used to shape the output AC voltage to be close to a sine wave.

3.2 PWM Switching Techniques Classification

The PWM switching can be divided into two switching scheme which are PWM with Bipolar voltage switching and PWM with Unipolar voltage switching.

3.2.1. PWM with Bipolar Voltage Switching

The basic idea to produce PWM Bipolar voltage switching signal is shown in Figure 3.1. It comprises of a comparator used to compare between the reference voltage waveform V_r with the triangular carrier signal V_c and produces the bipolar switching signal. If this scheme is applied to the full bridge single phase inverter all the switches S1, S2, S3 and S4 are turned on and off at the same time. The output of one leg is equal and opposite to the output of another leg . The output voltage is determined by comparing the reference signal, V_r and the triangular carrier signal,V_c . Comparison between these two signals and the resulting output waveform are clearly illustrated in Figure 3.2.

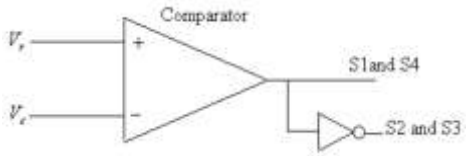

Fig 3.1: Bipolar PWM Generator

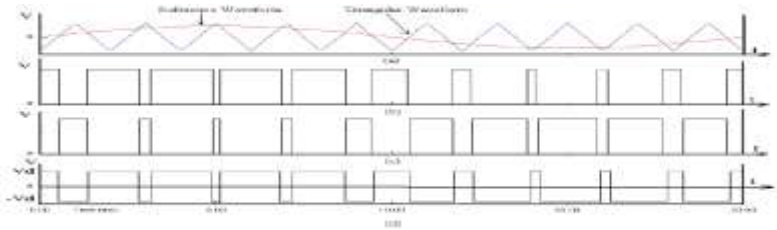

Fig 3.2: SPWM with Bipolar voltage switching (a) Comparison between reference waveform and triangular waveform b) Gating pulses for S1 and S4 (c) Gating pulses for S2 and S3 (d) Output waveform

3.2.2. PWM with Unipolar Voltage Switching

In this scheme, the triangular carrier waveform is compared with two reference signals which are positive and negative signal. The basic idea to produce SPWM with Unipolar voltage switching is shown in Figure 3.3. The different between the Bipolar SPWM generators is that the generator uses another comparator to compare between the inverse reference waveform $-V_r$. The process of comparing these two signals to produce the Unipolar voltage switching signal is graphically illustrated in Figure 3.4.

In Unipolar voltage switching the output voltage switches between 0 and V_{dc} , or between 0 and $-V_{dc}$. This is in contrast to the Bipolar switching strategy in which the output swings between V_{dc} and $-V_{dc}$. As a result, the change in output voltage at each switching event is halved in the Unipolar case from $2V_{dc}$ to V_{dc} . The effective switching frequency is seen by the load is doubled and the voltage pulse amplitude is halved. Due to this, the harmonic content of the output voltage waveform is reduced compared to Bipolar switching.

In Unipolar voltage switching scheme also, the amplitude of the significant harmonics and its sidebands is much lower for all modulation indexes thus making filtering easier, and with its size being significantly smaller.

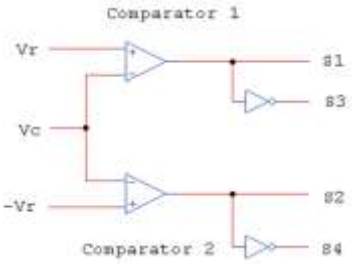

Fig 3.3: Unipolar PWM Generator

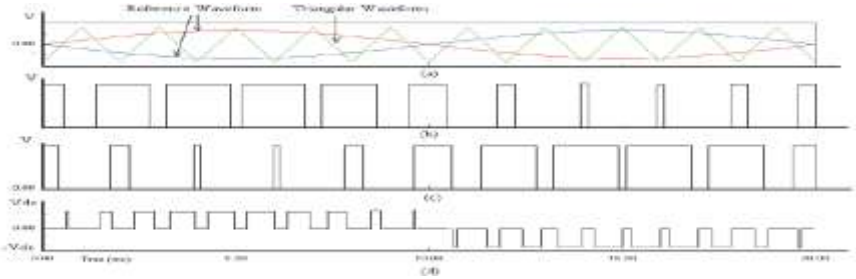

Fig 3.4: SPWM with Unipolar voltage switching (a) Comparison between reference waveform and triangular waveform (b) Gating pulses for S1 and S4 (c) Gating pulses for S2 and S3 (d) Output waveform

3.3. Pulse Width Modulation Methods

The natural sampling techniques for a multilevel inverter are categorized into two and they are:

1) Single-Carrier SPWM (SCSPWM) and 2)Sub-Harmonic PWM (SHPWM)

Sub-Harmonic PWM is an exclusive control strategy for multilevel inverters and has further classifications. They are:

(i) Carrier Disposition PWM method

- Phase Disposition (PD)
- Alternative Phase Opposition Disposition (APOD)
- Phase Opposition Disposition (POD)

(ii) Phase Shifted Carrier PWM method (PSPWM)

3.3.1 Carrier Disposition PWM Method

For an N-level inverter, N-1 carriers with the same frequency *fc* and the same amplitude *Ac* are disposed such that the bands they occupy are contiguous. The reference waveform has maximum amplitude *Am*, a frequency *fm*, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the IGBT corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the IGBT corresponding to that carrier is switched off . The phases of carrier signals are arranged to produce three main disposition techniques known as PD, POD and APOD.

Carrier Disposition method arrange N-1 carrier waveform of same amplitude and frequency in continuous bands to fully occupy the linear modulation range of the inverter. The reference or modulating wave is positioned at the center of the carrier set, and continuously compared with the carriers to obtain the necessary gating pulses.

3.3.2 Phase disposition PWM

In phase disposition method all the carriers have the same frequency and amplitude. Moreover all the N-1 carriers are in phase with each other. It is based on a comparison of a sinusoidal reference waveform with vertically shifted carrier waveform. In this method, for an N level inverter

Bipolar switching: (N-1) carrier waves are compared with one reference wave.

Unipolar switching: (N-1)/2 carrier waves are compared with two reference waves.

For this technique, significant harmonic energy is concentrated at the carrier frequency, but since it is a co-phasal component, it doesn't appear in the line-to-line voltage.

3.3.3 Phase opposition Disposition PWM

In Phase Opposition Disposition (POD), the carrier signal above the zero axis all the carrier wave have same frequency, same amplitude and in phase each other. But the below the zero axis all the carrier wave have same frequency, same amplitude and in phase but all carrier wave have phase shifted 180 degree compare to the above zero axis carrier waveform. In this method, for an N level inverter:

Bipolar switching: (N-1) carrier waves are compared with one reference wave.

Unipolar switching: (N-1)/2 carrier waves are compared with two reference waves.

The significant harmonics are located around the carrier frequency, for both the phase and line-to-line voltage waveform.

3.3.4 Alternative Phase Opposition Disposition PWM

Carriers in adjacent bands are phase displaced by 180°. In Alternate Phase Opposition Disposition PWM (APOD), every carrier waveform is out phase with its neighboring carrier wave by 180 degree. All the carrier waveform have same frequency, same amplitude and but compare one carrier waveform to neighbor carrier waveform is phase shifted 180 degree. Odd carrier waveforms are in phase but compare to even carrier waveform are out of phase shift 180 degree in odd carrier waveform. In this method, for an N level inverter,

Bipolar switching: (N-1) triangular waves and one sinusoidal wave.

Unipolar switching: (N-1)/2 triangular waves and two sinusoidal waves.

With this method, the most significant harmonics are centered as sidebands around the carrier.

3.3.5 Phase Shift PWM

Here carriers are phase shifted by 360/(n-1), where n is the level of MLI. For 3 level, carriers phase shifted by 180deg. For 5 level, carriers phase shifted by 90deg. Optimum harmonic cancellation is achieved, phase shifting each carrier by $(k-1)\pi/n$, where, k is the kth inverter, n is the number of series-connected single phase inverters $n= (L-1)/2$ where L is the number of switched DC levels that can be achieved in each phase leg. In this method, for an N level inverter

Bipolar switching: N-1 carrier waves are compared with one reference wave.

Unipolar switching:(N-1)/2 carrier waves are compared with two reference waves.

IV. SIMULATION RESULTS:

4.1 Three Level CHB-MLI Using Cascaded 3-Phase Transformers with Common Arm Configuration

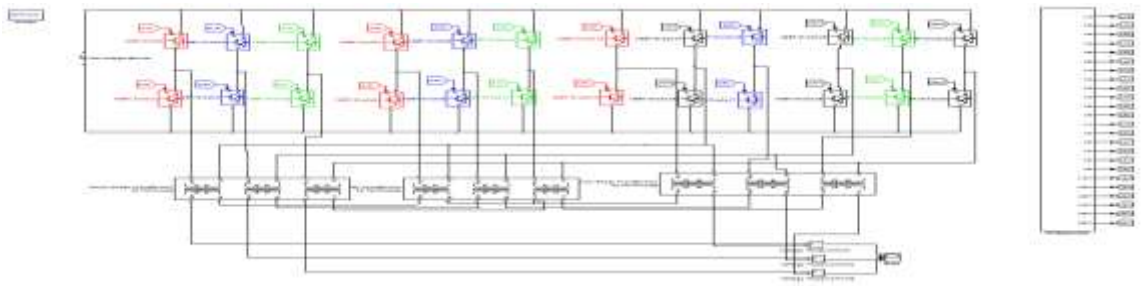

Fig 4.1 Simulation Circuit of 3 Level CHB-MLI Using Cascaded 3-Phase Transformers With Common Arm Configuration

Fig 4.1. shows the simulation circuit of Cascaded H-Bridge three level multilevel inverter using cascaded three 3-phase transformers with common arm configuration technique. Here 3 three phase 3 level MLI's are connected using Three 3-phase transformers. And common arm configuration is applied to reduce switches. Since here three transformers are used, therefore 12 switches are reduced. Here input source is taken as 100V dc. Then the ac output voltage will be 600v. And it can be observed in fig 4.1.2 and fig 4.1.4.

4.1.1 Bipolar Switching Sequence

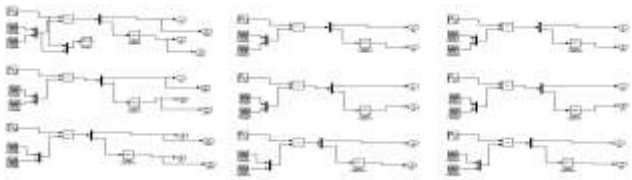

Fig 4.1.1 Switching Sequence for 3 Level CHB-MLI

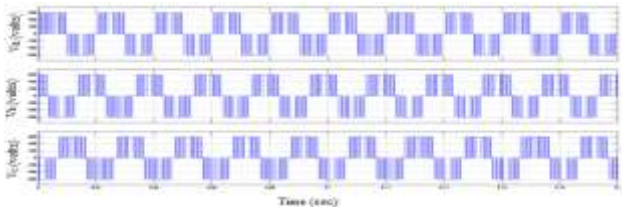

Fig 4.1.2. Output Waveform of 3 level CHB-MLI When Bipolar Switching is Applied

4.1.2 Unipolar Switching Sequence

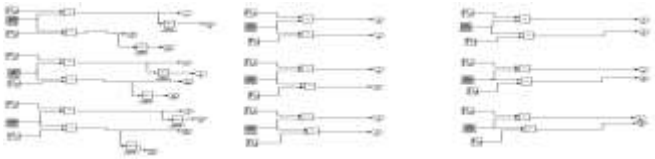

Fig 4.1.3 Switching Sequence for 3 Level CHB-MLI

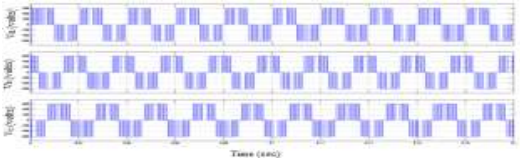

Fig 4.1.4 Output Waveform of 3 Level CHB-MLI when Unipolar Switching is Applied

4.2. Simulation Circuit of 5level CHB-MLI Using Cascaded 3-Phase Transformers with Common arm Configuration

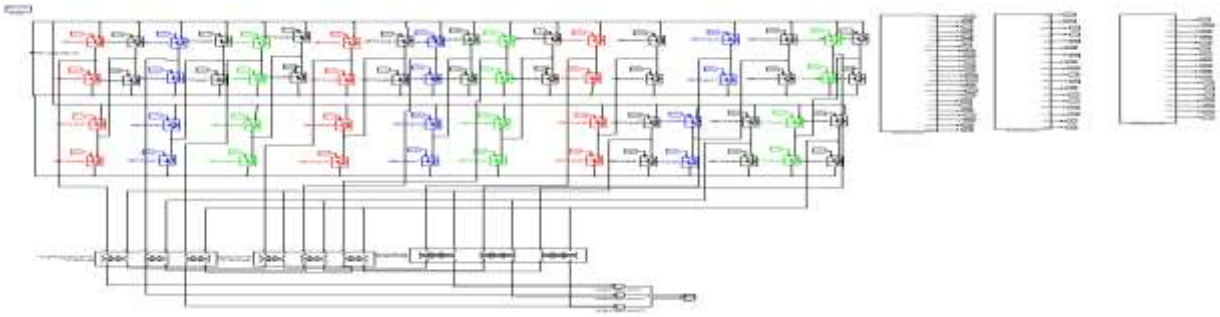

Fig.4.2. Simulation Circuit of 5level CHB-MLI Using Cascaded 3-phase Transformers with Common arm Configuration

Fig 4.2 shows the simulation circuit of 5 level CHB-MLI using cascaded 3-phase transformers with common arm configuration technique. Here it contains three 3-phase 5level MLI's connected using three cascaded 3-phase transformers. And common arm configuration technique has been applied to reduce number of switches. Here input dc source is 100V and the ac output voltage will be 600V and it can be observed in followed output waveforms.

4.2.1 Bipolar Switching Sequence

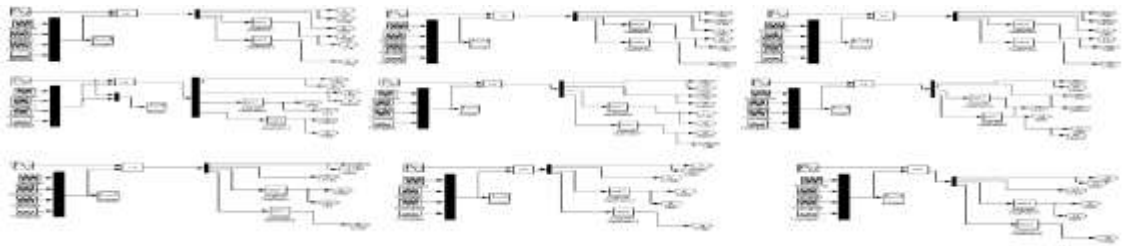

Fig 4.2.1.Bipolar switching sequence applied for 5 level CHB-MLI.

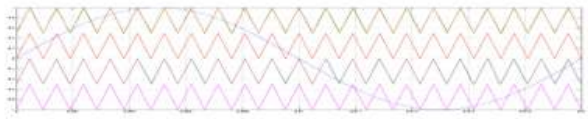

Fig 4.2.1.1 Pulse generation for 5 level CHB-MLI when PD-PWM is applied

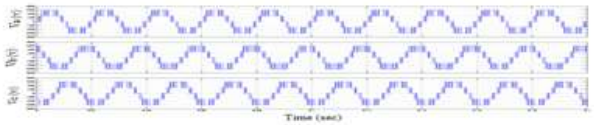

Fig 4.2.1.2 Output voltage of 5 level CHB-MLI when PD-PWM is applied.

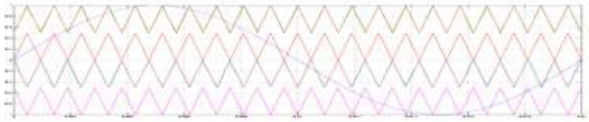

Fig 4.2.1.3 Pulse generation for 5 level CHB-MLI when POD-PWM is applied

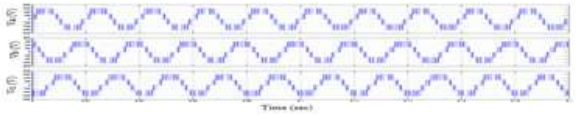

Fig 4.2.1.4 Output voltage of 5 level CHB-MLI when POD-PWM is applied

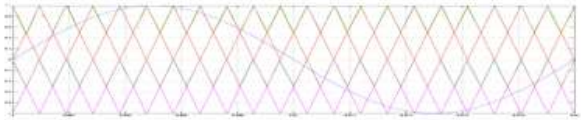

Fig 4.2.1.5 Pulse generation for 5 level CHB-MLI when APOD-PWM is applied

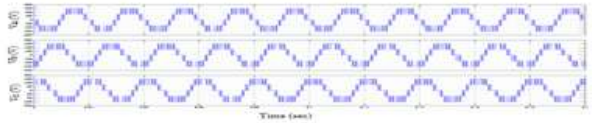

Fig 4.2.1.6 .Output voltage of 5 level CHB-MLI when APOD-PWM is applied

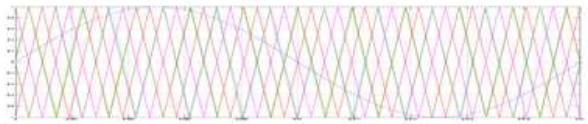

Fig 4.2.1.7 Pulse generation for 5 level CHB-MLI when PS-PWM is applied

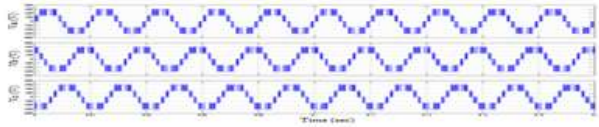

Fig 4.2.1.8 Output voltage of 5 level CHB-MLI when PS-PWM is applied

4.2.2. Unipolar switching sequence

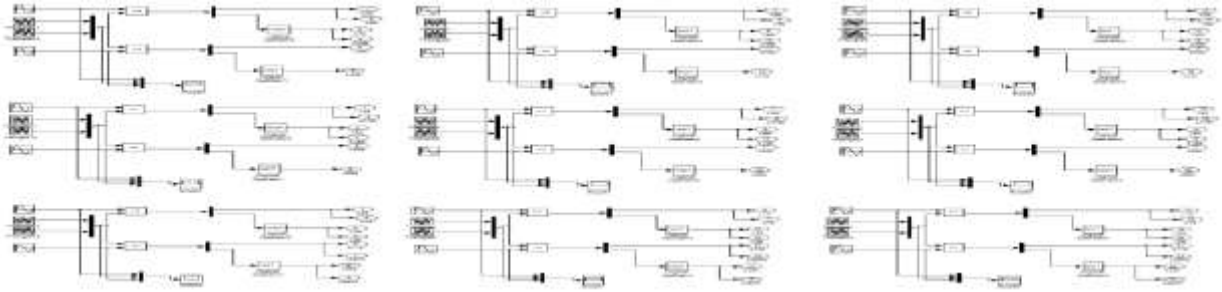

Fig 4.2.2.Unipolar Switching Sequence Applied for 5 level CHB-MLI

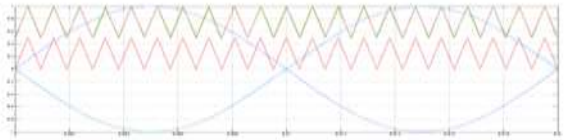

Fig.4.2.2.1 Pulse generation for 5 level CHB-MLI when PD-PWM is applied

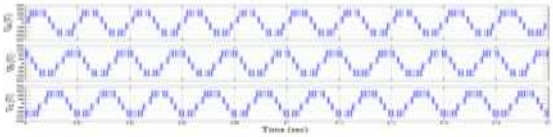

Fig.4.2.2.2 Output voltage of 5 level CHB-MLI when PD-PWM is applied

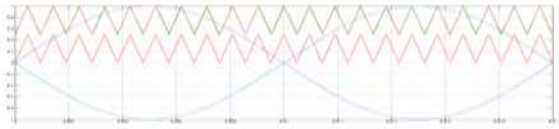

Fig.4.2.2.3 Pulse generation for 5 level CHB-MLI when POD-PWM is applied

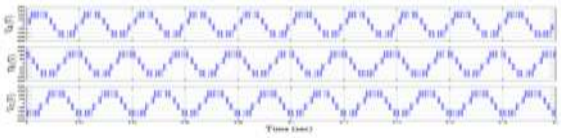

Fig.6.22.Output voltage of 5 level CHB-MLI when POD-PWM is applied

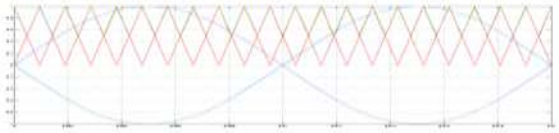

Fig.6.23. Pulse generation for 5 level CHB-MLI when APOD-PWM is applied

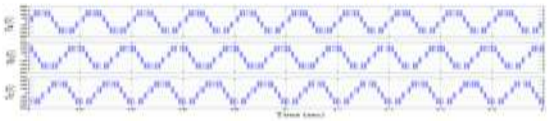

Fig.6.24.Output voltage of 5 level CHB-MLI when APOD-PWM is applied

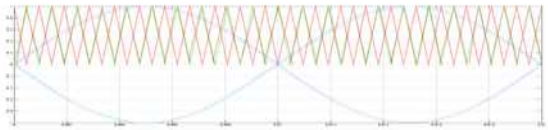

Fig.6.25. Pulse generation for 5 level CHB-MLI when PS-PWM is applied

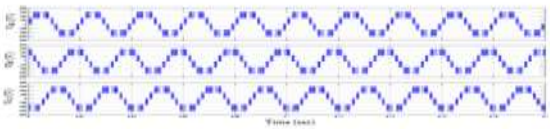

Fig.6.26.Output voltage of 5 level CHB-MLI when PS-PWM is applied

V.COMPARISON TABLES

5.1. Comparison of CHB-MLI with & without Common arm Configuration Technique

CHB-MLI employing cascaded 3-phase transformers without common arm configuration technique			**CHB-MLI employing cascaded 3-phase transformers with common arm configuration technique**		
MLI	**Transformers used**	**No.of switches required**	**MLI**	**Transformers used**	**No.of switches required**
3 level	Three	36	3level	Three	24
	Five	60		Five	36
5 level	Three	72	5level	Three	60
	Five	120		Five	96
7level	Three	108	7level	Three	96
	Five	180		Five	156

5.2. Comparison of Bipolar & Unipolar Switching Techniques

Bipolar Switching technique			Unipolar switching technique		
MLI	**Carrier waves**	**Reference waves**	**MLI**	**Carrier waves**	**Reference waves**
3 level	Two	One	3 level	One	Two
5 level	Four	One	5 level	Two	Two
7 level	Six	One	7 level	Three	Two

5.3. Observation of THD for Circuit when Different PWM Techniques are Applied

Bipolar Switching technique		Unipolar Switching technique	
PWM technique	THD%	PWM technique	THD%
APOD	22.68	APOD	19.02
POD	24.73	POD	20.84
PD	27.42	PD	20.84
PS	16.52	PS	14.56

VI. CONCLUSION

These days electrical system has been trended in smaller, low cost, and lighter. In this paper, a cascaded multilevel inverter adopting a common-arm configuration to reduce the number of switching devices is proposed. The proposed configuration has achieved smaller system by reduction of switching components and its gating drivers. When we use the proposed inverter scheme, the scheme generates higher current rating than conventional circuit. Fortunately, disadvantage of the current rating in the proposed circuit can be compensated by advantage of the size effect by reduction of switching component and gating drivers.

Valuable advantages of the proposed approach are summarized as follows:

1) Efficient and economical circuit configuration to synthesize multilevel outputs by using three-phase transformers.

2)Increase of utilization rate and decrease of volume by using three-phase transformers.

3) Possibility of using a single dc source by using isolated transformers.

4) Little transition loss of switch due to low switching frequency and reduced electromagnetic interference, which is suitable for high-voltage applications.

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BIOGRAPHY

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