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ULTRA LOW VOLTAGE SRAM WITH REPLICA DELAY TECHNIQUE

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ABSTRACT

As moving toward low supply voltages in low-power SRAM designs, threshold and supply voltage variations will give larger impacts on the power characteristics and speed of SRAM. The techniques based on replica circuits which minimize the effect of operating conditions on the power as well as speed. Replica bitlines and memory cells are used to give a reference signal whose delay tracks that of the bitlines. This signal is used to generate the sense clock with minimal slack time and control wordline pulsewidths to limit bitline swings. We implemented the circuits for variants of the technique, using cell current rationing.

Keywords: Cell Current Rationing, Low Supply Voltage, Replica Bitlines, Self Time Techniques, SRAM, Supply Voltage, Technology Scaling, Threshold Voltage, Ultra Low Voltage.

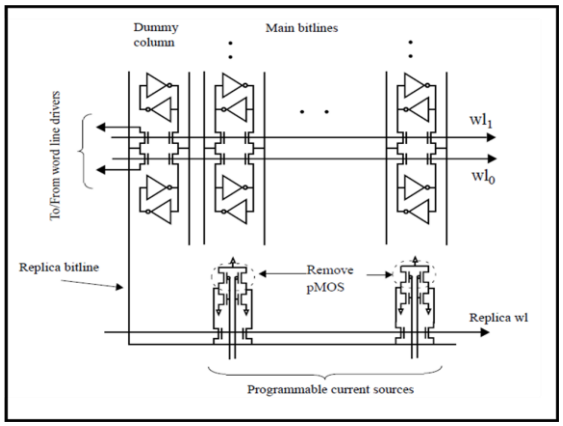
I. INTRODUCTION

Low power circuit designers have been continuously pressing down supply voltages to decrease the energy consumption of chips for portable applications. This trend has also applied to low-power SRAM's in the last decades. As the supply voltages are scaling down at a rapid rate, to control subthreshold leakage, the threshold voltages have not scaled down, which results in reduction of the gate overdrive for the transistors. The variations in the threshold voltages can lead to submicron devices in near future, the delay variations of low-power circuits will rise in the future.

II. TECHNIQUE USED

2.1 Replica Delay Element Based on Cell Current Rationing

An extra row and column containing replica memory cells can be used to provide local resetting timing information for the word line drivers. The extra row contains memory cells whose PMOS devices are eliminated to act as current sources, with currents equal to that of an accessed memory cell . All their outputs are tied together and they simultaneously discharge the replica bitline. This enables a multiple of memory cell current to discharge the replica bitline. The current sources are activated by the replica word line which is turned on during each access of the block. The replica bitline is identical in structure to the main bitlines with dummy memory cells providing the same amount of drain parasitic loading as the regular cells.

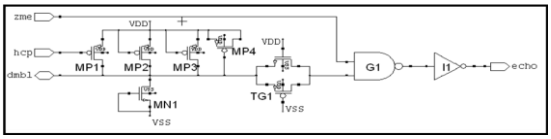


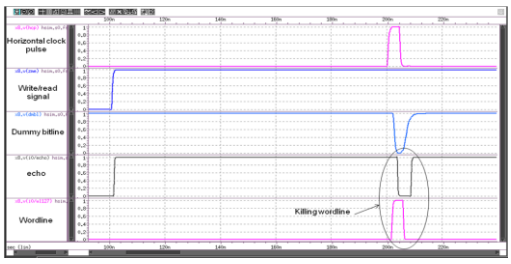
By connecting *n* current sources to the replica bitline, the replica bitline slew rate can be made to be *n* times that of the main bitline slew rate achieving the same effect as bitline capacitance rationing.

The local word line drivers are skewed to speed up the rising transition and they are reset by the replica bitline. The replica bitline signal is forwarded into the word line driver through the dummy cell access transistor. This occurs only in the activated row since the access transistor of the dummy cell is controlled by the row word line *wl*, minimizing the impact of the extra loading on the replica bitline. The forward path of the word line driver can be optimized for speed, independent of the resetting of the block select or global word line by skewing the transistors sizes.

2.2 Self Time IO Block

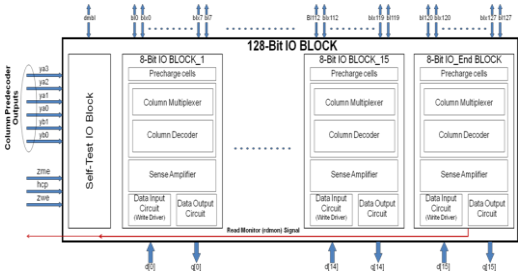
When *hcp* is low the dummy bitline *dmbl* is connected to the power supply (V_{DD}). The dummy bitline *dmbl* is connected to one input of the NAND gate G1 followed by an inverter I1. The other input of the G1 is connected to memory enable signal which is high when the chip is selected. Hence we will have a high *echo* (reset) signal. If a rising edge of the *hcp* occurs, the *dmbl* will get discharged through the capacitors form of MN1 and we will have a low echo signal. This low echo signal resets the flip-flop circuit in control block and kills the corresponding wordline.





2.3 Design of 128 bit i/o Block

The IO block is further integrated with the memory core, row decoder and control block and tested successfully. The predecoder outputs are common to all 8-bit IO blocks. The signals *zme* and *zwe* are the memory enable and read/write enable signals respectively generated from control block. The signal *hcp* (horizontal clock pulse) is also generated in the control unit from global clock pulse.



III. LAYOUT OF 128-BIT IO BLOCK

The layout is implemented in a 180nm process as part of a 1024x16CM8 SRAM. The design rule followed is UMC 0.18um 4ML RF Flash process. There are four metal layers used with the minimum metal layers width is:

Min Metal4 Width : 1.2 um

Min Metal4 Spacing : 1.0 um

Min Metal3 Width : 0.28 um

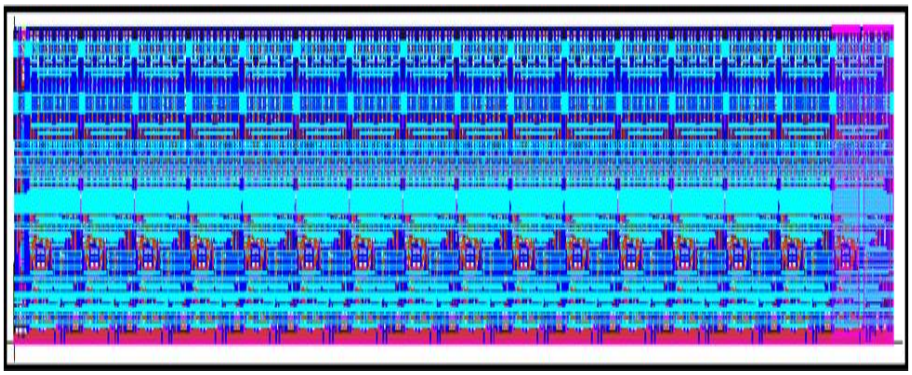
Min Metal3 Spacing : 0.28 um

Min Metal2 Width : 0.28 um

Min Metal2 Spacing : 0.28 um

Min Metal1 Width : 0.24 um

Min Metal1 Spacing : 0.24 um

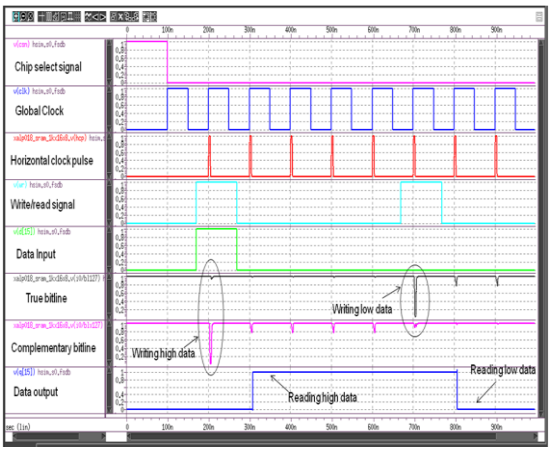


Layout of the 128-bit IO Block

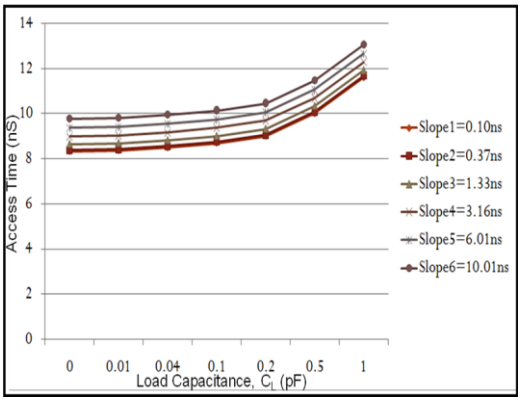
IV. MEASUREMENT RESULTS

4.1 The Memory Write/Read Operation

The simulation result which illustrates the complete write/read operation. The IO block is tested with complete memory chip.

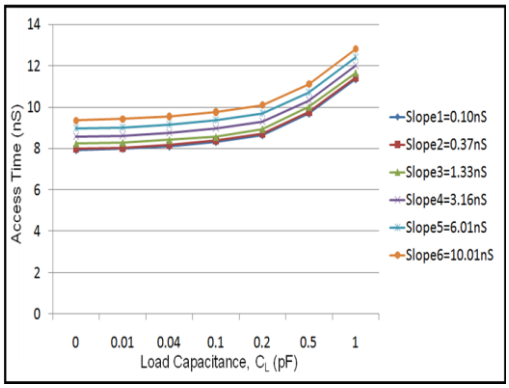


Complete Write/Read Operation



Access Time While Reading High Data

Similarly the measured read access time to read low data for different load and clock slope is tabulated in Table 5.4. A graph is again plotted in Figure between load capacitance and access time for different clock slope, which shows that the read access time is almost independent of the load capacitance.



Access Time While Reading Low Data

V. CONCLUSION

Low-power SRAM has become more important due to the high demands on the handheld devices. The active power of the SRAM is mainly consumed in bit lines and data lines because the SRAM charges and discharges the high capacitive bit lines and data lines in read and write cycles. As the bit width of SRAM becomes larger for high performance applications, the power consumption in bit lines and data lines continues to increase. The bit cell rationing is used to provide local resetting timing information for the word line drivers. Therefore, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. Considerable attention has been paid to the low-power and high-performance design. To reduce the power consumption the first technique is to reduce the active duty cycle of the memory operation using self-timed architecture. An internal clock pulse with reduced Ton (On time) is generated which controls all the memory operation. Second technique of power reduction is to use multi-stage row and column decoding which reduces the power consumption as well as it also improves the timing characteristics of memory. The behavior of an SRAM differs considerably under different operating conditions i.e. PVT conditions.

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