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DESIGN OF FIR FILTER WITH MEMORY MANAGEMENT SYSTEM FOR FREQUENCY BAND SELECTION USING VHDL

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ABSTRACT

In DSP applications, Low pass filters are used for decimation and for interpolation. While decimating, low pass filters are used to reduce the bandwidth of a signal before reducing the sampling rate. This is done to minimize aliasing effect produced due to the overlapping of replicas of original spectrum. In this paper, Area Efficient and Cost Effective Techniques for design polyphase decimation filter have been presented to flexibility in selection of various frequency bands for low frequency applications. The digital filters employed in mobile systems ,radios, tv transmitters receivers must be higher order and realized to select frequency at high speed to change channels. This Multirate design methodology is flexible,systematic and applicable to many problems in multichannel applications.

Keywords: Decimation , Interpolation, Multirate, Polyphase

I INTRODUCTION

Recently, there has been rapid progress in the field of multirate digital signal processing. The applications of multirate systems include subband coding of audio, video, speech signals, fast transforms using digital filter banks, wavelet analysis of all types of signals, and many other fields [l]. In multirate systems, decimation and interpolation filters are the most important building blocks. **A** lot of literature is available for the theory and design of decimation and interpolation filters**.** The issues regarding VLSI implementation scheme for multirate filters are under investigation**.**

In today's Digital Signal Processing applications, most common operation is a sampling rate conversion. In most of these applications, very efficient & high quality sample rate converter is required. The sampling rate of a digital signal can be changed using interpolators and decimators[1]. Multirate systems can perform a processing task with improved performance characteristics while simultaneously offering that performance at a lower cost than traditional approaches. A decimation filter is one of the most important fundamental building blocks of a multirate system when down sampling is employed. The accurate design of a decimation filter is of utmost importance because it

governs the attenuation of unwanted aliasing. Multirate system in which there is a need to reduce imaging by up sampling a digital interpolation filter is employed [3]. Interpolation and decimation (up sampling & downsampling) can be performed efficiently by using polyphase interpolator and decimator structures. These structures are obtained from the polyphase representation of the transfer function of the interpolation or decimation filter [1]. This paper,describes the implementation of decimation structures and evaluated for selection of various frequency bands. Decimation reduces the sampling rate at the output of a system so that another system with a lower sampling rate can receive this signal as input. A narrow filter followed by a down sampler is referred to as a decimator. Decimator can reduce the sampling rate up to the limit called the Nyquist rate, according to which the sampling rate must be higher than the highest frequency component present in the input signal to avoid aliasing. Reduction in sampling rate results in a cheaper implementation. Down sampling by a factor M is implemented by keeping every Mth sample and throwing away M-1 samples in between. Polyphase Decimation Filter is a digital filter (FIR/IIR) which is implemented using a polyphase decomposition technique [6][11]. Simple decimator, polyphase decimator and efficient polyphase decimators are implemented in this paper and their performances are compared in terms of speed, logic area occupied, power consumption.FIR filter is used as an antialiasing filter where parallelism can easily be achieved.

II MULTIRATE POLYPHASE FILTER DESIGN METHODOLOGY

A signal processing system that filters the data and has an output data rate is different than the input data rate called Multirate filter. The ratio of the output data rate to the input data rate is known as the Multirate factor. In decimation and Interpolation Multirate filters, the normalized transition bandwidth inversely relates to the decimation factor *M* and the interpolation factor *L*. The order of a decimation or interpolation filter increases as M or L [4].we can use multistage Multirate filters to simplify Multirate filters that have large sampling frequency conversion factors. Polyphase is a way of doing sampling rate conversion that leads to veryefficient implementations. Sampling rate reduction is required for efficient transmission, and a sampling rate increase is required for the regeneration of the speech. The processes of sampling rate reduction called decimation. It can be efficiently implemented using finite impulse response digital filters [5].

2.1 Multirate Polyphase Decimator

It is found that efficient implementations of low pass FIR filters could be obtained by a process of first reducing the sampling rate, filtering, and then increasing the sampling rate back to the original frequency. The process of sampling rate reduction in Multirate Polyphase Decimator and interpolator is shown in fig.1(a)-(b)

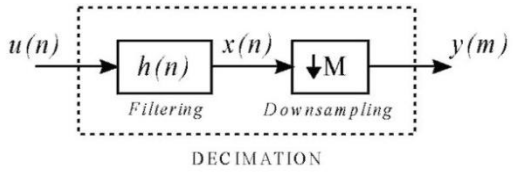

Figure 1(a): Decimation filter

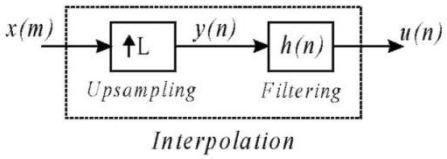

Figure 1(b): Decimation filter

In this paper we have studied,designed and simulated Multirate Polyphase Decimator in both direct and transposed form. Multirate Polyphase Decimator structure in direct and transposed form is as shown below. Fig.(2)-(3)

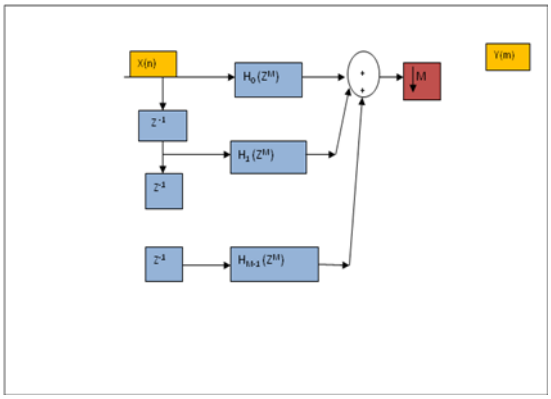

Figure 2: Polyphase Decimator direct form

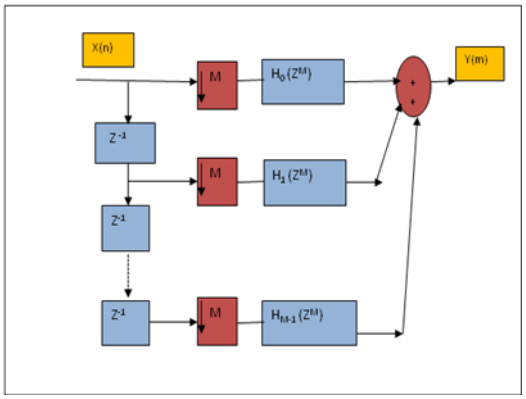

Figure 3: Polyphase Decimator tranposed form

The direct form is generally preferred because of its higher performance and power efficiency. In this, Polyphase decimator filter with a factor of 6 is designed.The impulse response is obtained by convolution of vectors with 6 ones in each, The trade-off between additions and delay elements is circuit and technology dependent, and, hence, should be evaluated on the circuit level.

III PROPOSED DESIGN OF FREQUENCY BAND SELECTION UNIT (FSU)

In this paper we propose a design of memory unit to serve the purpose of selection of frequency band. The circuit consists of single unit of 8X4 memory size as shown in fig 4.

It consists of two, data input lines of 8 bit each.One of the data line is used to set default frequency value & other input user defined frequency value.The address line is of 4-bits.When address is ‘0’ by default frequency will be selected & for other input values ‘1’,’2’,’3’user defined frequency will be selected providing flexibility in frequency selection. For 6-tap Polyphase Decimation filter such 6 units are attached to it.

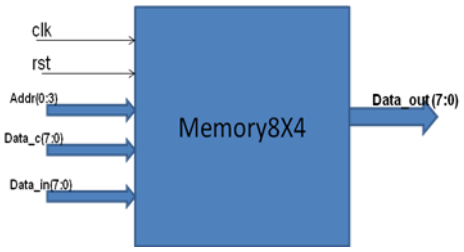

Figure 5: Memory Unit for Frequency Selection

IV RESULT

4.1 Polyphase Decimator

Following figure 5(a) – (d) shows direct form of Polyphase decimator which uses latches in direct form, this system is very efficient because it required very less power dissipation and maintaining higher speed. But this design consumed more area.

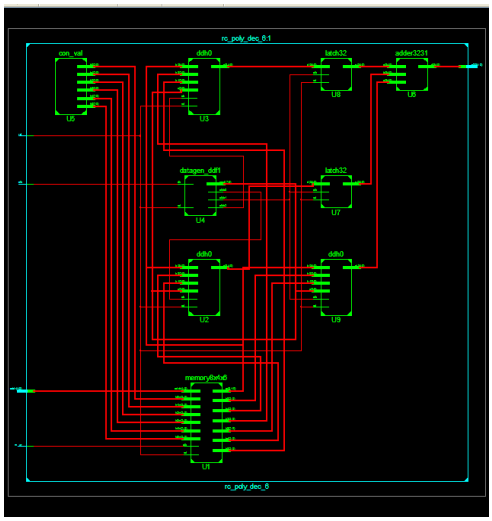

Fig. 6(a) RTL view of Polyphase decimator in direct form with FSU

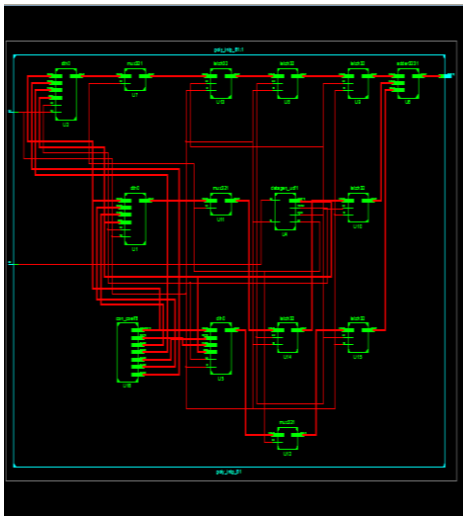

Fig. 6(b) RTL view of Polyphase decimator in transposed form with FSU

In this work, Multirate polyphase FIR filters are designed in VHDL (very High speed Integrated Circuits Hardware Description Language). Logic synthesis & simulation is done in Xilinx ISE 14.1 Project Navigator and Isim simulator integrated in the Xilinx package. The circuit performance is evaluated on the Xilinx device family

Spartan-6 XC6SLX45T-FGG484 -3C FPGA.

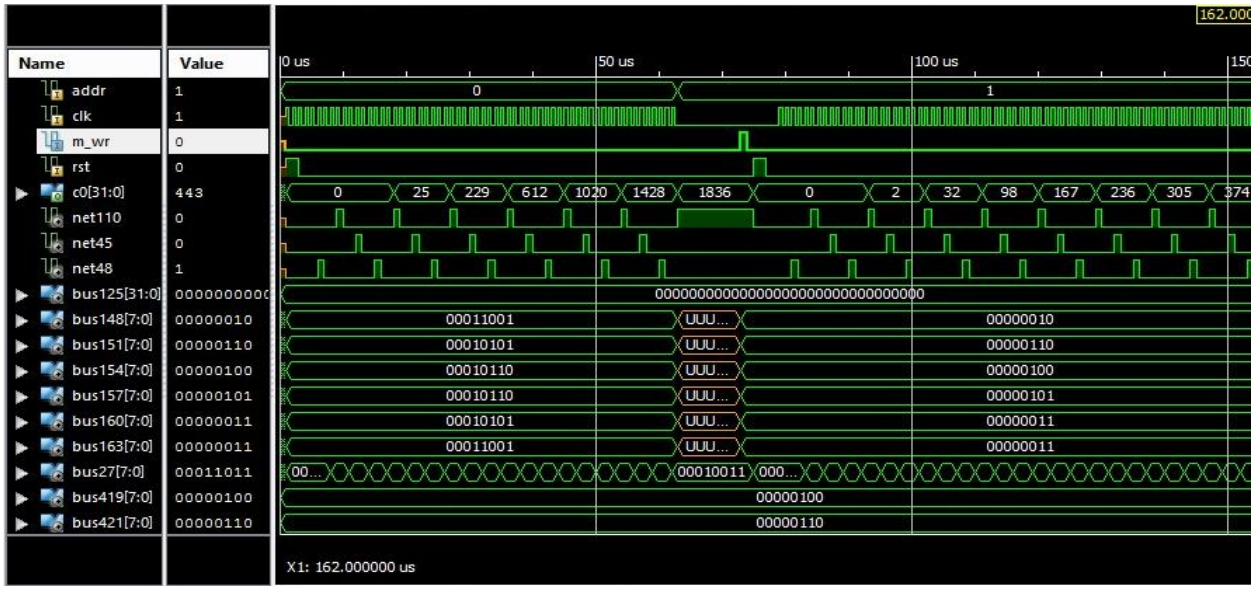

Fig. 7(a) Simulation Result of Polyphase Decimator In Direct Form With FSU

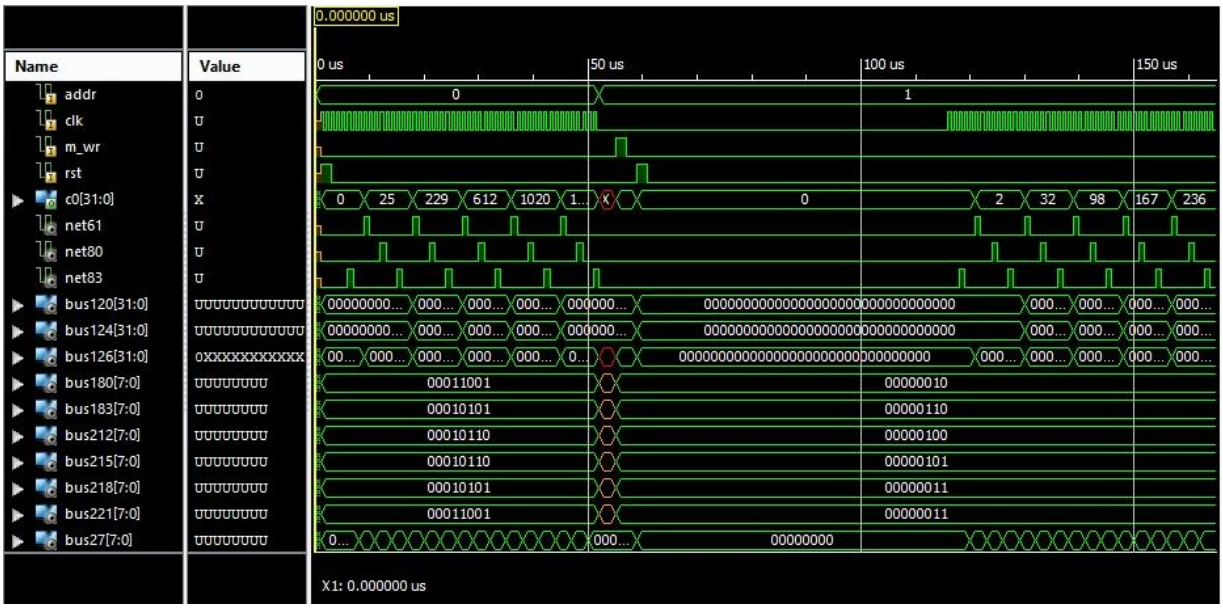

Fig. 7(b) Simulation Result of Polyphase Decimator In Transposed Form With FSU

V DESIGN SUMMARY

Sr.No	Name of Filter	No. of LUTs	Delay (ns)	Power (mW)	Memory Usage	Speed(Mhz)
1	Direct form	165/2 400	12.629	15	142636 Kb	335.45
2	Transpose form	112/2 400	6.448	15	142636 Kb	242.4
3	Polyphase decimator direct form	177/2 400	10.204	13	256296 Kb	236.79
4	Polyphase decimator transpose form	182/2 400	6.297	13	142636 Kb	274.57
7	Polyphase decimator direct form with FSU	156/2 400	8.529	11	144556 Kb	341.646

VI CONCLUSION

Design and Implementation of Multirate Polyphase decimator along with memory unit for frequency band selection is presented. Also, done the Optimization of the Module using different techniques and methodology. Authors have used Xilinx ISE 14.1 Project Navigator and Isim simulator integrated in the Xilinx package Spartan-6 XC6SLX45T-FGG484 -3C FPGA. Family. The circuit performance is evaluated on the Xilinx device family. The optimized parameters power dissipation and area and speed of the system analyzed by using Xilinx. Multirate Polyphase decimator designed using different form which provides power, area and speed for system. The results are given separately and comparison in tabulation form found satisfactory. Physical testing verified that implementation worked correctly. Direct form of Multirate Polyphase filter is best suited for implementation of digital signal processing system which requires very less power dissipation and maintaining higher speed. Polyphase decimator using FSU provides flexibility in selection of Low Frequency band which is the need of many applications like radios,tv remote where multiple channels are accessed.

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