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THE ALTERNATE ARM CONVERTER: A NEW HYBRID MULTILEVEL CONVERTER WITH DC-FAULT BLOCKING CAPABILITY

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ABSTRACT

This paper explains the working principles, supported by simulation results, of a new converter topology intended for HVDC applications, called the alternate arm converter (AAC). It is a hybrid between the modular multilevel converter, because of the presence of H-bridge cells, and the two-level converter, in the form of director switches in each arm. This converter is able to generate a multilevel ac voltage and since its stacks of cells consist of H-bridge cells instead of half-bridge cells, they are able to generate higher ac voltage than the dc terminal voltage. The director switches in the AAC are responsible for alternating the conduction period of each arm, leading to a significant reduction in the number of cells in the stacks. Furthermore, the AAC can keep control of the current in the phase reactor even in case of a dc-side fault and support the ac grid, through a STATCOM mode.

Keywords—AC–DC power converters, emerging topologies, fault tolerance, HVDC transmission, multilevel converters, power system faults, STATCOM.

I. INTRODUCTION

Increasing attention is being paid to HVDC transmission systems, especially because most of the new schemes are intended to connect remote renewable sources to the grid and the most effective way to do it is to transmit the generated power using HVDC instead of HVAC. For offshore HVDC applications, voltage-source converters (VSCs) are more suitable than current-source converters (CSCs) due to their black-start capability and ability to operate in weak ac grids, such as a network of wind turbine generators. However, compared to CSCs, their power ratings are limited and their efficiency is somewhat poorer although recent developments in semiconductor devices are closing the gap in both cases so that VSCs are becoming economically viable as technological solutions in large HVDC schemes; some of them to be commissioned in the next couple of years.
Since the 1990s, a great deal of research effort has been directed to improving converters primarily to make them more power efficient than the first generation of VSCs. The modular multilevel converter (MMC), published in 1998 for STATCOM applications, published in 2003 for HVDC Power Transmission, and followed up in brought several new features to VSC. It replaced the series-connected insulated-gate bipolar transistor (IGBT) in each arm of the two-level converter by a stack of half-bridge cells which consist of a charged

capacitor and a set of IGBTs. Since the voltage of each cell is small compared to the ac and dc voltages, a large number of cells are placed in series in each stack, resulting in the creation of a voltage waveform with numerous steps. This characteristic has two main consequences: 1) the generated ac current is very close to a sine wave and no longer requires any filtering, thus saving the implementation of bulky and costly ac filters and 2) the converter does not rely on high-frequency PWM to syntheses voltage waveforms, thus greatly reducing the switching loss and thereby improving the overall efficiency of the converter.

Notwithstanding the advantages brought by this new generation of converters, there are some aspects that can still be improved. The avoidance of the ac filter means that the cells are now one of the bulkiest components of the converter station and cell format requires a physically large capacitor in addition to the set of IGBTs. Half-bridge cells are normally used in preference to H-bridge cells in order to reduce the number of devices in conduction at any time and, therefore, reduce the conduction power loss. Even if this choice is justified by the large cost associated with the power losses, it also means that the converter is vulnerable to a dc-side fault in a similar way to a two-level converter whereas an H-bridge version would not be. The inability of half-bridge cells to produce a negative voltage results in the conduction of the anti parallel diodes connected to the IGBTs, thus creating an uncontrollable current path in case of a collapse of the dc bus voltage. Since the dc breakers for high-power applications are still under development, the lack of other fast protective mechanisms makes this loss of a means to control dc fault current problematic. In the double-clamped sub module (DCS) was suggested as a new type of cell to deal with this issue.

The DCS connects two half-bridge cells together into one cell through one additional IGBT and two diodes. This configuration offers the possibility of switching in a reverse voltage, similar to the H-bridge cell, in order to respond to the need for negative stack voltage in case of a dc-side fault.

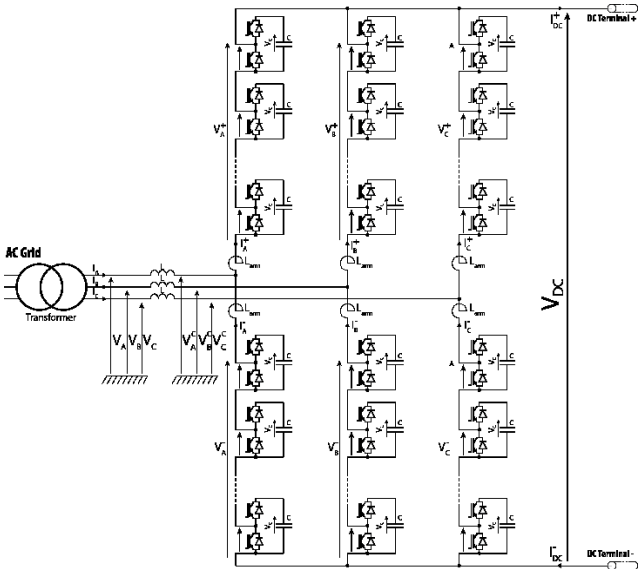

Fig.1.1 - half-bridge MMC topology

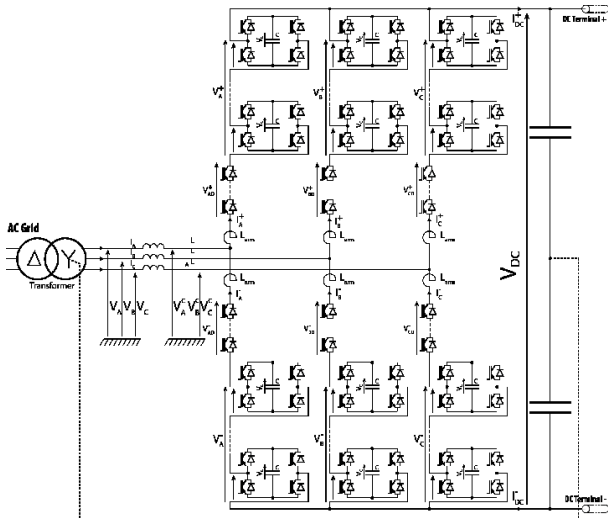

Fig.1.2 - AAC topology

The Modular Multilevel Converter (MMC), illustrated in Fig.1.1, was the first modular Voltage Source Converter (VSC) to provide both low switching losses and low AC current distortion; these features contribute to the higher power efficiency and the significant reduction in the size of the AC filters of recent VSC power stations. A number of MMC converter stations are now in operation and more are planned in the next couple of years with power ratings ever increasing. Over the last few years, a new family of hybrid topologies, such as the Alternate Arm Converter (AAC), drawn in Fig.1.2, has emerged.

These topologies essentially combine both the 2-level VSC and the MMC together in order to improve on some characteristics such as smaller overall volume, better power efficiency and, in some topologies, DC-side fault blocking capability. It has also been shown that the AAC has a better temperature distribution between the IGBT modules of a cell in comparison to the MMC. Extensive studies have also presented different modeling approaches of the electrical dynamics of these multilevel converters and it has been shown that reduced dynamic models have an acceptable level of accuracy while offering an appreciable boost in computing speed.

The AAC has a relatively similar electrical topology to the MMC with the main difference being the presence of director switches, i.e. series-IGBTs, in its arms in series with the stack of cells. The switching state of these director switches determines which arms are both generating the converter voltage waveform and carrying the AC current to the respective DC terminal. This approach has proven, to be both power and volume effective, resulting in (i) the number of cells be significantly reduced, e.g. up to half the number of cells compared to the MMC, (ii) the average cell voltage deviation is lower allowing smaller capacitors in the cells and (iii) the use of full H-bridge cells instead of half-bridge cells, thus the AAC is able to block DC-side faults without compromising its overall power efficiency.

In the case of the MMC, it was observed rapidly after the topology was proposed that unplanned circulating currents were running between the legs. This issue was later solved by implementing additional feedback loops in charge of monitoring the arm currents. Besides, it has also been observed that this circulating current can be used to reduce the cell voltage deviation of the cell capacitor or by adding a 2nd harmonic filter at the midpoint of the arm inductors. This paper presents an original arm current waveform for the in the MMC, inspired by the working mechanism of the AAC. This study focuses on the effects of changing the arm current waveforms

which only implies an update of the control system (software) but not the converter itself (hardware) which thus stays the same.

This paper presents the analysis of a new converter topology, which is part of a new generation of VSCs based on the multilevel approach but also takes some characteristics from the two-level VSC. As explained through this paper, one of the features of this topology lies in its ability to retain control of the phase current during the loss of the dc-bus voltage, thanks to the presence of H-bridge cells in the arms. The key advantage of this new topology lies in its reduced number of cells; thus, it does not compromise the efficiency of the converter, nor on the number of devices and even saves volume because of the reduced number of cells per arm. A component level simulation of a 20-MW converter is used to confirm the claimed characteristics of this new topology.

II. DESCRIPTION OF THE TOPOLOGY

2.1. Basic Operation-

The alternate arm converter (AAC) is a hybrid topology which combines features of the two-level and multilevel converter topologies. As illustrated in Fig. 2.1.1, each phase of the converter consists of two arms, each with a stack of H-bridge cells, a director switch, and a small arm inductor. The stack of cells is responsible for the multistep voltage generation, as in a multilevel converter. Since H-bridge cells are used, the voltage produced by the stack can be either positive or negative; thus, the converter is able to push its ac voltage higher than the dc terminal voltage if required. The director switch is composed of IGBTs connected in series in order to withstand the maximum voltage which could be applied across the director switch when it is in the open state. The main role of this director switch is to determine which arm is used to conduct the ac current.

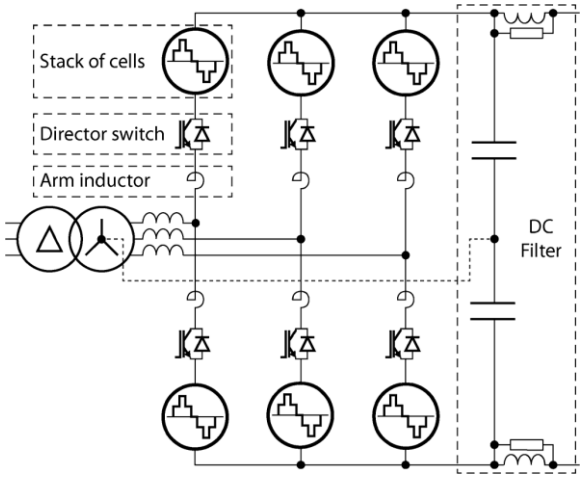

Fig.2.1.1. schematic of the alternate arm converter, with the optional middle-point connection shown in a dashed line.

Indeed, the key feature of this topology is to use essentially one arm per half cycle to produce the ac voltage. By using the upper arm to construct the positive half-cycle of the ac sine wave and the lower arm for the negative part, the maximum voltage that each stack of cells has to produce is equal to half of the dc bus voltage, which is approximately half the rating of the arm of the MMC. The resulting voltage and current waveforms of the cells and reactor switches are illustrated in Fig. 2.1.2. The aim of the AAC is to reduce the number of cells, hence the volume and losses of the converter station.

The short period of time when one arm finishes its working period and hands over conduction of the phase current to the opposite arm is called the overlap period. Since each arm has an active stack of cells, it can fully control the arm current to zero before opening the director switch, hence achieving soft-switching of the director switch, further lowering the power losses. Although normally short, the overlap period can provide additional control features, such as controlling the amount of energy stored in the stacks.

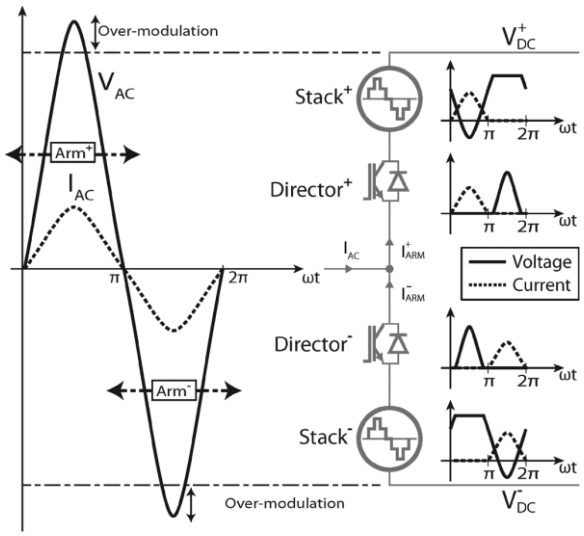

Fig.2.1.2. idealized voltage and current waveforms over one cycle in a phase converter of the AAC, showing the working period of each arm.

2.2. DC Fault Management

One of the important characteristics of this converter is the ability of its arms to produce negative voltage. In fact, the AAC already uses this ability to produce a converter voltage higher than the dc terminal voltage without requiring the opposite arm to also produce a higher than normal positive voltage from its stack of cells, provided that the director switch is suitably rated. This ability is put to use in normal operation when the converter produces a voltage which is higher than the dc bus voltage.

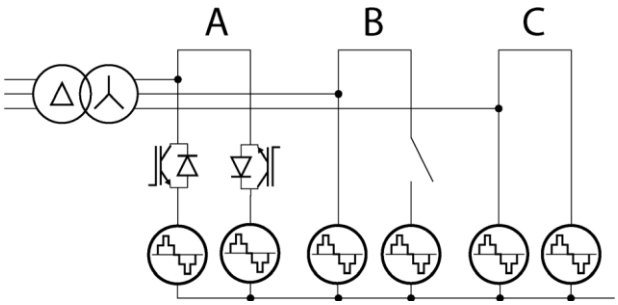

Fig.2.2.1. STATCOM modes of the AAC during a dc-side fault: alternate arms (mode A), single working arm (mode B), and dual working arms (mode C).

It can be extended to the case when the dc bus voltage collapses to a low level, for example, a fault on the dc side. Since enough cells are present in the stacks to oppose the ac grid voltage, the converter is thus able to keep all of its internal currents under control, in contrast to the two-level converter or half-bridge version of the MMC. Furthermore, even if the absence of a dc bus voltage means that it is no longer possible to export active

power to the dc side, it does not prevent reactive power exchange with the ac side. Since the arms of the AAC are still operational, the entire converter can now act as a STATCOM. There are some choices over how the director switches are used in this mode, as illustrated in Fig. 2.2.1, which lead to different modes that can be achieved by the AAC during a dc-side fault: one arm conducts per half cycle similarly to normal operation, one arm works continuously or the two arms working together, potentially increasing the reactive power capability to 2.0 p.u. This STATCOM mode of managing the converter during dc fault can help to support the ac grid during a dc outage, in contrast to the worsening effect that can be brought about by other topologies because of their inability to control dc-side fault current.

III. ARM CURRENT WAVEFORMS

In its classic operating mode, the MMC distributes equally (i) the AC current between its upper and lower arms and (ii) the DC current between the three different legs. The complete set of equations describing the arm currents is given in (1)-(6). The signs present in these equations depend on the direction of the currents, using what is illustrated in Fig 1 and 2

$$IA+ = IA/2 + IDC/3 \quad (1)$$

$$IA- = -IA/2 + IDC/3 \quad (2)$$

$$IB+ = IB/2 + IDC/3 \quad (3)$$

$$IB- = -IB/2 + IDC/3 \quad (4)$$

$$IC+ = IC/2 + IDC/3 \quad (5)$$

$$IC- = -IC/2 + IDC/3 \quad (6)$$

The AAC distributes its AC currents in a different pattern as only one arm in each leg carries the full AC current while the other has its director switch opened, blocking any current from flowing through the arm. Using the variables $\alpha_{A,B,C} \in \{0,1\}$ which represent whether the AC current of a particular leg is passing either through the top or bottom arm, the set of equations describing the arm currents in AAC mode are given in (7)-(12):

$$IA+ = \alpha A\ IA - IF/3 \quad (7)$$

$$IA- = -(1-\alpha A)\ IA - IF/3 \quad (8)$$

$$IB+ = \alpha B\ IB - IF/3 \quad (9)$$

$$IB- = -(1-\alpha B)\ IB - IF/3 \quad (10)$$

$$IC+ = \alpha C\ IC - IF/3 \quad (11)$$

$$IC- = -(1-\alpha C)\ IC - IF/3 \quad (12)$$

However the AAC inherently generates a 6-pulse ripple on top of the DC current waveform as a consequence of the alternating nature of the arm conduction periods. Since the objective of this study is to migrate an already existing MMC converter to an AAC mode of operation without having to change the hardware but only by updating the control system (i.e. software), installing a DC filter is out of question. To resolve this issue, an additional active filtering current is added to the arm currents in order to keep the DC current smooth. This

filtering current I_F (13) is obtained by calculating the ripple component of the DC current waveform resulting from AAC operation in order to suppress it by adding a circulating current of opposing sign through all three legs.

$$IF=IA++IB++IC+-IDC$$
$$=IA-+IB-+IC--IDC$$
$$=\alpha A\ IA+\alpha B\ IB+\alpha C\ IC-IDC \qquad (13)$$

The addition of this active filtering current alters the original nature of the AAC mode as the arms will now continuously run a current through them as opposed to for only one half of the cycle and no current during the other half of the cycle because the director switches would be closed. However the magnitudes of the arm currents will be small for a large proportion of the time, while the arm is not carrying the main AC current, compared to the MMC mode of operation, as shown in the simulation section below. Finally, only the arm current waveform will be different because the currents seen at both the AC and DC terminals of the converter will be the same as under the normal MMC mode of operation.

IV. SIMULATION RESULTS

4.1. Simulation Model-

In order to assess the benefits of the AAC mode of operation, shown in fig.4.1.1 a 120 MW MMC converter has been simulated using Simulink® and the Artemis® toolbox in order to simulate a reasonably large number of half-bridge cells. The characteristics of this simulation model are listed in Table 4.1. In order to better match realistic MMC converter, triplen harmonic voltage injection has been used (about 15% of the fundamental magnitude) in order to shape the converter voltage waveform into an almost trapezoidal waveform and to push the power rating to its theoretical maximum while still using only half-bridge cells. Furthermore, a power loss analysis has also been performed by post-processing the voltage and current waveforms in each cells using the power loss data from the datasheet of the 3.3 kV 1.2 kA HiPak IGBT device 5SNA 1200E330100. In the later part of the simulation section, the steady state junction temperature of the different semiconductor devices in a cell (e.g. top and bottom IGBT and diode modules) by applying the individual power loss figure of each device into a power-thermal model derived in ANSIS and assuming a coolant temperature of 60ºC shared by all the semiconductor devices.

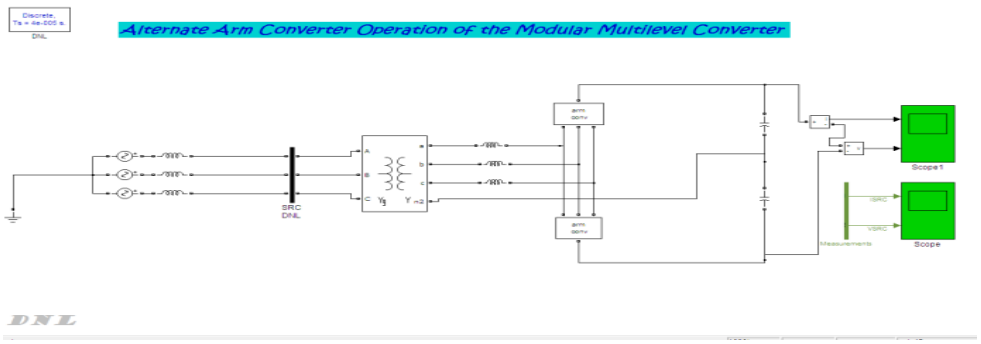

Fig.4.1.1- optimization scenarios matlab model

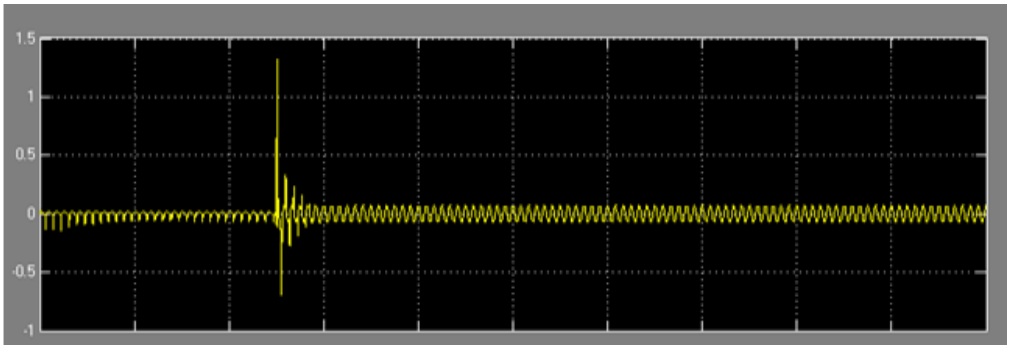

Fig.4.1.2-arm converter outputs for current

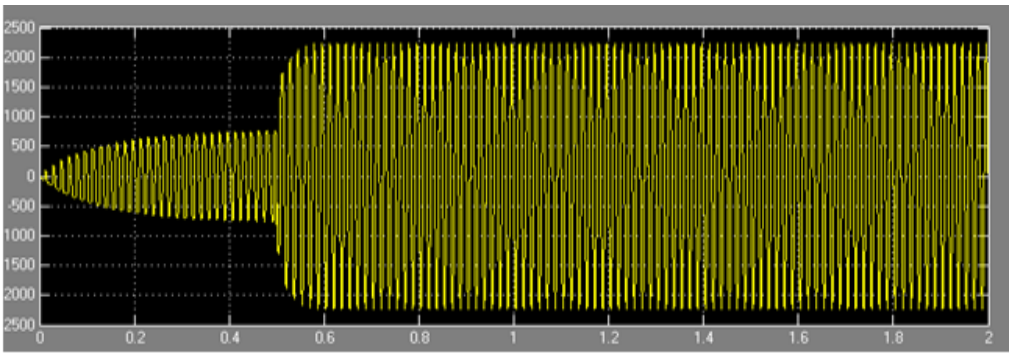

Fig.4.1.3: arm converter output for voltage

Table 4.1- Characteristics of the simulated MMC model

Rated power	120 MW
DC bus	±50 kV
AC line	55 kV
AC frequency	50 Hz
Triplen harmonic voltage	15%
Number of cells per stack	56
Cell capacitor	8 mF
Phase inductor	8 mH
Arm inductor	6 mH

4.2. Arm Current Waveforms-

The arm current waveforms resulting from this mode of operation are observed in this section. Fig. 4.2.1 shows the top arm current waveform in both MMC and AAC operating modes (respectively the red and green curves) under unity power factor rectifier mode. The third curve (blue) is the result of the difference between the two waveforms and can be interpreted as the equivalent circulating current which can be injected in the converter to move from the MMC mode to the AAC mode of operation. It can be observed that at unity power factor a large amount of the fundamental cycle is spent with a small amount of current magnitude in AAC mode as opposed to the MMC mode. As more reactive power is involved in the conversion process as shown in Fig 4.2.2 (same amount of active and reactive power) and in Fig. 4.2.3 (reactive power only), the arm current waveform becomes more and more distorted in AAC mode with still a significant portion of the cycle used by low magnitude current but at the expense of an increasing peak values to attain twice the value in the MMC mode. The power losses have computed for different operating points and the results listed in Table 4.2 with the total power loss values plotted in accordance to the angular value of their respective operating points in Fig. 4.2.4.

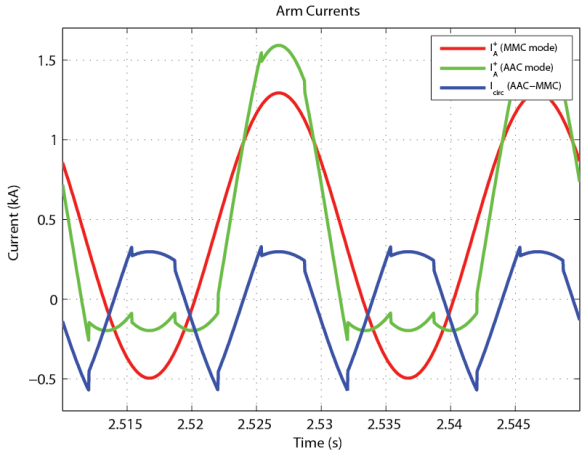

Fig.4.2.1 - Arm A+ current waveform in MMC (red), AAC (green) modes and the resulting circulating current (blue) with active power only

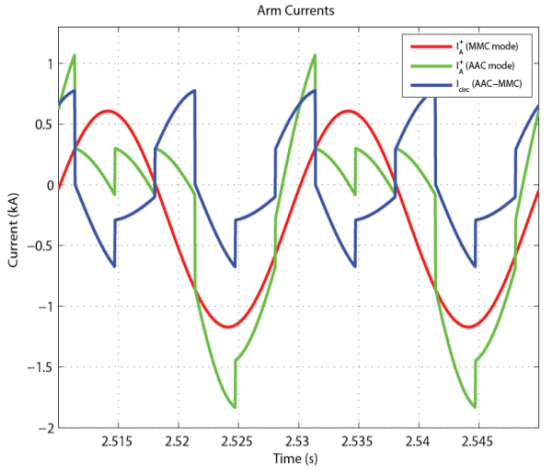

Fig.4.2.3- Arm A+ current waveform in MMC (red), AAC (green) modes and the resulting circulating current (blue) with reactive power only

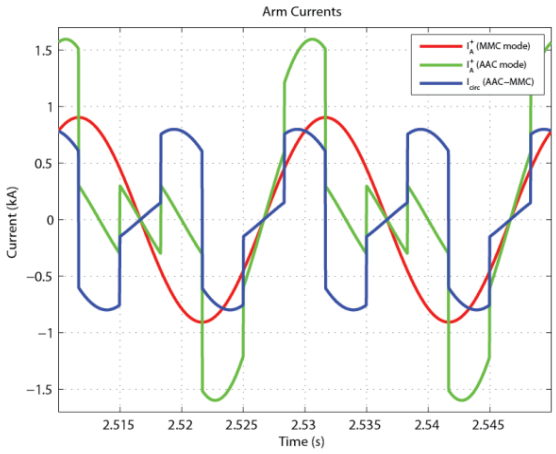

Fig.4.2.2 - Arm A+ current waveform in MMC (red), AAC (green) modes and the resulting circulating current (blue) with both active and reactive powers

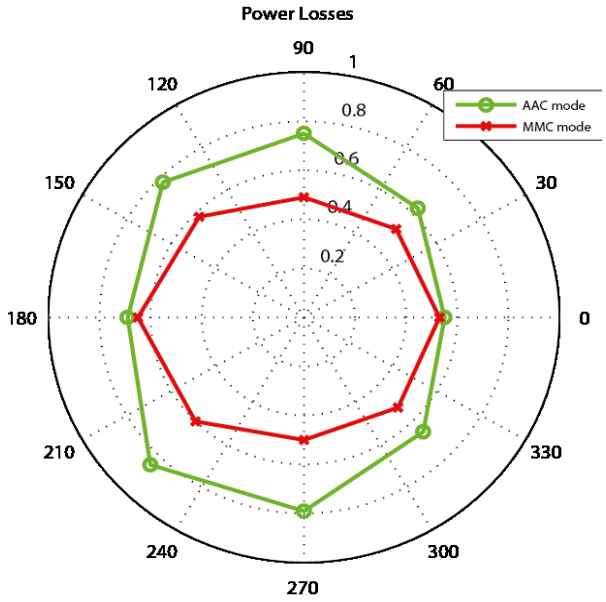

Fig.4.2.4 - Power losses as percent of the total apparent power in MMC and AAC modes for different operating point

Table 4.2. – Power losses of the MMC model depending on the mode of operation and operating point relative to the apparent power

Active Power / Reactive Power		1 pu / 0 pu	0.7pu / 0.7 pu	0 pu / 1 pu	-0.7pu / 0.7 pu	-1 pu / 0 pu	-0.7pu / -0.7pu	0 pu / -1 pu	0.7pu / -0.7pu
MMC mode	Conduction losses	0.50%	0.44%	0.36%	0.37%	0.38%	0.37%	0.35%	0.45%
	Switching losses	0.15%	0.14%	0.13%	0.13%	0.15%	0.15%	0.15%	0.16%
	Total losses	0.65%	0.58%	0.49%	0.51%	0.53%	0.52%	0.50%	0.60%
AAC mode	Conduction losses	0.53%	0.56%	0.51%	0.43%	0.38%	0.40%	0.49%	0.53%
	Switching losses	0.16%	0.22%	0.24%	0.20%	0.17%	0.26%	0.30%	0.32%
	Total losses	0.69%	0.78%	0.75%	0.63%	0.55%	0.66%	0.79%	0.85%

4.3. Observation at unity power factor:

The previous set of results indicates that this new AAC mode is only potentially attractive for unity power factor only as both the arm current peak values and the power losses are increase dramatically when reactive power is involved in the conversion process. The next part of this paper assumes that only these two operating points (inverter and rectifier active power only) are considered with the results focusing on the rectifier mode mainly since the inverter mode is merely an opposite phase angle version of the former.

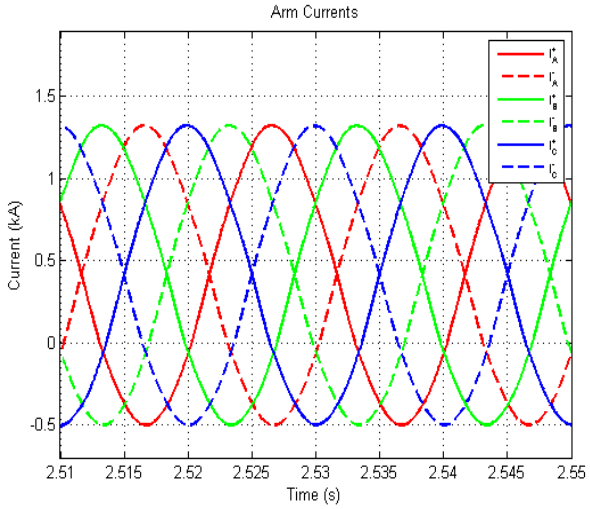

Fig.4.3.1 - arm current waveforms in MMC mode

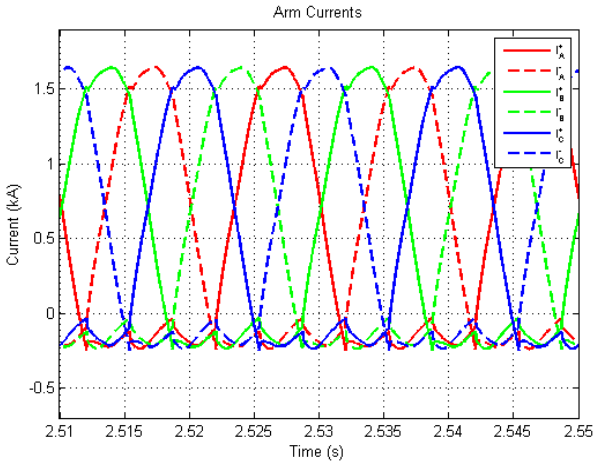

Fig.4.3.2 - arm current waveforms in AAC mode

Fig. 4.3.1 and 4.3.2 show the arm current waveforms respectively in MMC and AAC modes of operation. On one hand, the MMC mode results in the arms continuously conducting a large amount of current as opposed to the AAC mode where a significant part of the cycle is spent with only a small amount of current (around -150 A). This remaining low magnitude current mainly consists of the filtering current I_F (13). On the other hand, the peak value of the arm current currents is lower in the MMC mode compared to the AAC mode (respectively 1.3 kA and 1.6 kA thus 23% higher in the AAC case).

V. CONCLUSION

The AAC is a hybrid topology between the two-level converter and the modular multilevel converter. By combining stacks of H-bridge cells with director switches, it is able to generate almost harmonic-free ac current, as does the modular multilevel approach. And by activating only one arm per half cycle, like the two-level converter, it can be built with fewer cells than the MMC.

Since this topology includes cells with capacitors which are switched into the current path, special attention needs to be paid to keeping their stored energy (equivalently, the cell capacitor voltage) from drifting away from their nominal value. When the converter is running at this condition, the energy levels of the stacks return to their initial values at the end of each cycle without any additional action. In cases where this equilibrium is not attained, an overlap period can be used to run a small dc current in order to balance the stacks by sending the excess energy back to the dc capacitors.

Simulations of a small-scale model show that this converter is able to deliver performance under normal conditions, in terms of efficiency and current waveform quality, and provide rapid responses in the case of ac- or dc-side faults.

VI. ACKNOWLEDGMENT

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