ijates
ISSN 2348 - 7550

ULTRA LOW POWER LFSR FOR BIST

Md.Zakir Hussain[1], Md. Ali Ghazi Islam[2], Amit Sharma[3]

[1]Asst.Professor, [2,3]M.E. Student, ECED, Muffakham Jah college of Engineering and Technology Hyderabad, (India)

ABSTRACT

In most number of electronic systems that are used in safety critical applications circuit testing has to be performed periodically. For these systems power dissipation due to BIST [built in self-test] represents a significant percentage of overall power dissipation. So this paper presents an ultra-low transition test pattern generator, called ULT-LFSR, to reduce average and peak power of a circuit during test by reducing the transitions within random test pattern and between consecutive patterns. The proposed test pattern generator reduces the switching activity among the test patterns. We are reducing the transitions between consecutive patterns generated by the conventional LFSR.

Keyword:- low power, BIST,TPG,ATPG, Bipartite LFSR.

I. INTRODUCTION

The primary goal of this work has been to analyze the power dissipation of different LFSR schemes for BIST and deploy an effective LFSR using the information from the analysis. The main motive of the project is to design a different technique of Linear Feedback Shift Register (LFSR) for testing a combinational circuit. The techniques that are used in Built-in Self-Test BIST is basically an off line testing using ATE (Automatic Test Equipment) where the test pattern generator and test response analyzer are on chip circuitry (instead of equipment) based on pseudorandom patterns and involves compaction of test responses. BIST performs self-testing and reduces dependency on an External ATE. BIST is a DFT (Design for Testability) technique makes the electrical testing of a chip easier, faster and less costly.

Hence we have designed two different linear feedback shift registers which generates the pseudo random test patterns. As testing of circuit consumes 200% more power than designing it, to reduce the testing power the transitions between the two successive patterns of LFSR are being reduced using different techniques, which reduces the testing power gradually. The Test Patterns Generators proposed in this thesis are Standard LFSR and Bipartite LFSR. These LFSR are successfully executed with BIST top module in Xilinx tool. Testing is done on an CLA circuit. Hence Bipartite LFSR has the lowest power dissipation while testing the combinational circuit.

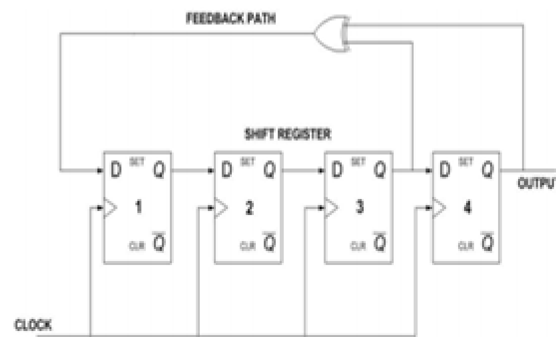


Fig. 1. Bit normal LFSR

II. PRIOR WORK

Several techniques have been reported to address the low power pattern generation problem. the technique proposed in consists of a distributed BIST control scheme that simplifies BIST architecture for complex ICs, especially during higher levels of test activity. This approach can schedule the execution of every BIST element to keep the power dissipation under a specified limit. a BIST strategy called dual-speed LFSR is proposed to reduce the circuit's overall switching activities.

This technique uses two different-speed LFSRS to control those inputs that have elevated transition densities. The low power test pattern generator presented is based on cellular automata, reduces the test power in combinational circuits.

Another low-power test pattern generator based on a modified LFSR is proposed. This scheme reduces the power in circuit under test (cut) in general and clock tree in particular.

a low-power BIST for data path architecture, built around multiplier-accumulator pairs, is proposed. The drawback is that these techniques are circuit-dependent, implying that non-detecting sub sequences must be determined for each circuit test sequence. a low power BIST based on state correlation analysis proposed.

Modifying the LFSR, by adding weights to tune the pseudorandom vectors for various probabilities, decreases energy consumption and increases fault coverage. a low-power random pattern generation technique to reduce signal activities in the scan chain is proposed. in this technique, an LFSR generates equally probable random patterns. the technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power. Authors proposed a method to select an LFSR's seed to reduce the lowest energy consumption using a simulated-annealing algorithm. Test vector inhibiting these techniques filter out some non-detecting sub sequences of a pseudorandom test set generated by an LFSR. These architectures apply the minimum number of test vectors required to attain the desired fault coverage and therefore reduce power.

International Journal of Advanced Technology in Engineering and Science
Vol. No.5, Issue No. 03, March 2017
www.ijates.com
ijates
ISSN 2348 - 7550

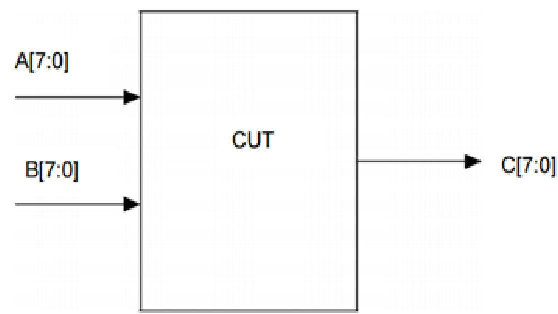


Fig. 2. Block diagram of CUT

Algorithmic methods: -

Testing very-large-scale integrated circuits with high fault coverage is a difficult task because of complexity. Therefore, many different ATPG methods have been developed to address combinatorial and sequential circuits.

- Early test generation algorithms such as *Boolean difference and literal proposition* were not practical to implement on a computer.
- The *D Algorithm* was the first practical test generation algorithm in terms of memory requirements. The D Algorithm introduced D Notation which continues to be used in most ATPG algorithms.
- *Path-Oriented Decision Making* (PODEM) is an improvement over the D Algorithm. PODEM was created in 1981 when shortcomings in D Algorithm became evident when design innovations resulted in circuits that D Algorithm could not realize.
- *Fan-Out Oriented (FAN Algorithm)* is an improvement over PODEM. It limits the ATPG search space to reduce computation time and accelerates backtracking.
- *Methods based on Boolean satisfiability* are sometimes used to generate test vectors.
- *Pseudorandom test generation* is the simplest method of creating tests. It uses a pseudorandom number generator to generate test vectors, and relies on logic simulation to compute good machine results, and fault simulation to calculate the fault coverage of the generated vector.
- *Built-in Self-Test, or BIST*, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).
- BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to.

III. TEST PATTERN GENERATION (TPG)

- *Automatic test pattern generation, ATPG* – generates pattern-data to systematically exercise as many logic-gates, and other components, as possible.

• *Built-in self-test, or BIST* – installs self-contained test-controllers to automatically test a logic (or memory) structure in the design.

A. AUTOMATIC TEST PATTERN GENERATION:

ATPG (acronym for both Automatic Test Pattern Generation and Automatic Test Pattern Generator) is an electronic design automation method/technology used to find an input (or test) sequence that, when applied to a digital circuit, enables testers to distinguish between the correct circuit behaviour and the faulty circuit behavior caused by defects. The generated patterns are used to test semiconductor devices after manufacture, and in some cases to assist with determining the cause of failure. The effectiveness of ATPG is measured by the amount of modelled defects, or fault models, that are detected and the number of generated patterns. These metrics generally indicate test quality (higher with more fault detections) and test application time (higher with more patterns). ATPG efficiency is another important consideration. It is influenced by the fault model under consideration, the type of circuit under test (full scan, synchronous sequential, or asynchronous sequential), the level of abstraction used to represent the circuit under test (gate, register-transistor, switch), and the required test quality.

B. BIST:

The main drivers for the widespread development of BIST techniques are the fast-rising costs of ATE testing and the growing complexity of integrated circuits. It is now common to see complex devices that have functionally diverse blocks built on different technologies inside them. Such complex devices require high-end mixed-signal testers that possess special digital and analog testing capabilities. BIST can be used to perform these special tests with additional on-chip test circuits, eliminating the need to acquire such high end testers.

Built-in Self-Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).

BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to. As an example, a common BIST approach for DRAM's includes the incorporation onto the chip of additional circuits for pattern generation, timing, mode selection, and go-/no-go diagnostic tests.

BIST is also the solution to the testing of critical circuits that have no direct connections to external pins, such as embedded memories used internally by the devices. In the near future, even the most advanced tester may no longer be adequate for the fastest chip, a situation where in self-testing maybe the best solution.

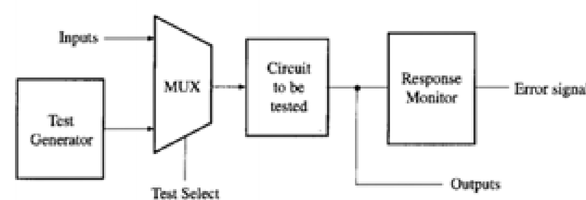


Fig. 3. BIST Architecture

International Journal of Advanced Technology in Engineering and Science
Vol. No.5, Issue No. 03, March 2017
www.ijates.com
ijates
ISSN 2348 - 7550

Advantages of implementing BIST include:

- Lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated.
- Better fault coverage, since special test structures can be incorporated onto the chips.
- Shorter test times if the BIST can be designed to test more structures in parallel.
- Easier customer support. and Capability to perform tests outside the production electrical testing environment. The last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

IV. PROPOSED WORK

A. Transition-count compression

In transition count testing, the signature is the no. of 0-to-1 and 1-to-0 transitions in the output data stream. Thus the transition count associated with sequence R=r1,r2,….,rm is

$$TC(R)=\sum_{i=1}^{m-1}\{ri \oplus ri+1\}$$

Where ∑ denotes ordinary arithmetic addition and ⊕ is modulo-2 addition. Since 0≤TC(R)≤ (m-1), the response-compression circuitry consists of a transition detector and a counter with [log m] stages .the following figures illustrates this concept. Note that the output of the transition detector and a counter with [log m] stages. figure is a function of the initial state of the flip-flop.

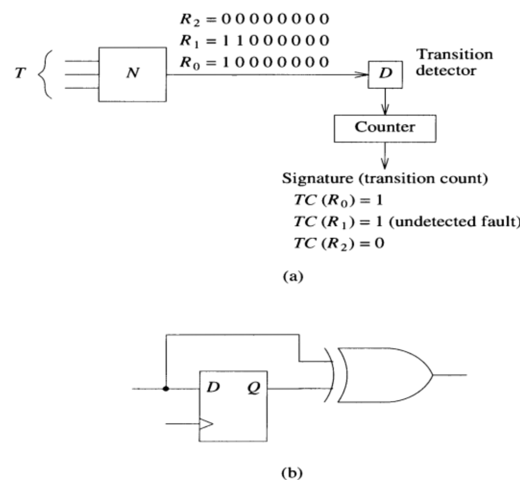


Fig. 4. (a) Transition count testing (b) Transition detector

Let T be the test sequence of length m for a circuit and R0 be the fault-free response, where TC(R0)=r. Let R be an arbitrary binary sequence of length m. R has (m-1) boundaries between bits where a transition can occur. There are

$$\binom{m-1}{r}$$

ways of assigning r transitions to m-1 boundaries so that R will also have a transition count of r. Since the sequence R obtained by complementing every bit of R has the same transition count as R. There are

$$2\binom{m-1}{r}$$

possible sequences that have a transition count of r only one of which is the response of the fault free circuit. Thus there are

$$2\binom{m-1}{r} -1$$

possible error sequences that lead to aliasing, If all faulty sequences are equally likely to occur as the response of a faulty circuit, then the probability of masking is given by

$$P_{TC}(M \mid m, r) = \frac{2\binom{m-1}{r} - 1}{2^m - 1}.$$

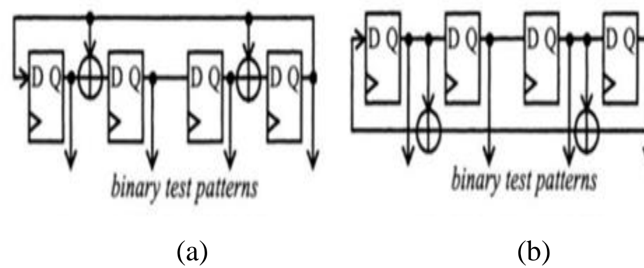
This function has similar properties to that derived for the case of one's counting. Unlike ones counting, transition counting is sensitive to the order of the bits in the response vector. Also, transition counting doesn't guarantee detecting all single bit errors.

B. Linear Feedback Shift Register:

A linear feedback shifts register (LFSR) is a shift register whose input bit is a linear function of its previous state. The only linear function of single bits is xor, thus it is a shift register whose input bit is driven by the exclusive-or (xor) of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle. The LFSR is one of the most frequently used TPG implementations in BIST applications. One reason for this is that an LFSR is more area efficient than a counter, requiring less combinational logic per flip-flop. There are two basic types of LFSR implementations, the internal feedback and external feedback LFSRs.

The external feedback LFSR best illustrates the origin of the name of the circuit: a shift register with feedback paths that are linearly combined via the exclusive-OR gates. Internal and external feedback LFSRs are duals of each other. Both implementations require the same amount of logic in terms of exclusive-OR gates and flip flops. In the external feedback LFSR, there are two exclusiveOR gates in the worst case path from the output of the last flip-flop in the shift register to the input of the first flip-flop in the shift register. On the other hand, the internal feedback LFSR has, at most, one exclusive-OR gate in any path between flip-flops. Therefore, the internal feedback LFSR provides the implementation with the highest maximum operating frequency for use in high performance applications.

The main advantage of external feedback LFSRs is the uniformity of the shift register; hence, there are some applications where external feedback is preferred. Internal feedback LFSRs are sometimes referred to as Type 1 LFSRs while external feedback LFSRs are referred to as Type 2 LFSRs. One problem with this terminology is remembering which is which, but a more serious problem is that the designations often reversed in some papers where the external l feedback LFSR is referred to as Type 1 and the internal feedback LFSR is referred to as Type 2.



(a) (b)

Fig. 5. (a) Internal feedback LFSR(b) External feedback LFSR

V. RESULT

TABLE I. COMPARISON BETWEEN REFERRED WORK AND PROPOSED WORK

Type/parameter	LP-LFSR	LP LFSR(proposed work)
Vccint(v)	1.8	1.2
Dynamic (w)	4.42	3.0
Vcco33(v)	3.3	2.5
Quiescent(w)	6.60	.041
Total power(mV)	120.22	44

From the table it is observant that, in Xilinx 7, the results obtained by implementation on xc3s200-4pq208 consumes less power when compared to [21] that in the base paper. Xilinx X-power is used for power analysis. The total power of LFSR in the referred work is 120.22mw whereas in our work is only 44. 00mw.Therefore, there is a decrease in the total power by almost 63.33% which is a significant amount of decline in the total power consumed

VI. SIMULATION RESULTS

TABLE II. XPOWER ANALYSIS:

Device	
Family	Spartan3
Part	xc3s200
Package	pq208
Temp Grade	Commercial
Process	Typical
Speed Grade	-4
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Characterization	
PRODUCTION	v1.2,06-25-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.002	3	---	---
Logic	0.000	55	3840	1
Signals	0.000	103	---	---
IOs	0.013	10	141	7
Leakage	0.041			
Total	0.056			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	36.1	83.0	27.0

ijates
ISSN 2348 - 7550

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.012	0.002	0.010
Vccaux	2.500	0.010	0.000	0.010
Vcco25	2.500	0.006	0.005	0.002
		Total	Dynamic	Quiescent
Supply Power (W)		0.056	0.015	0.041

TABLE III. DEVICE UTILIZATION SUMMARY:

Logic Utilization	Used	Available	Utilization
Number of Slices	41	1920	2%
Number of Slice Flip Flops	45	3840	1%
Number of 4 input LUTs	54	3840	1%
Number of bonded IOBs	10	141	7%
Number of GCLKs	3	8	37%

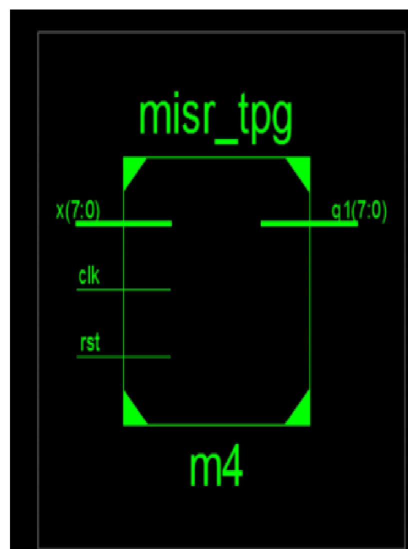


Fig. 6. MISR pin diagram:

The output of MISR is compared with the golden signature i.e. fault free output and using a comparator we can check the circuit is fault or not.

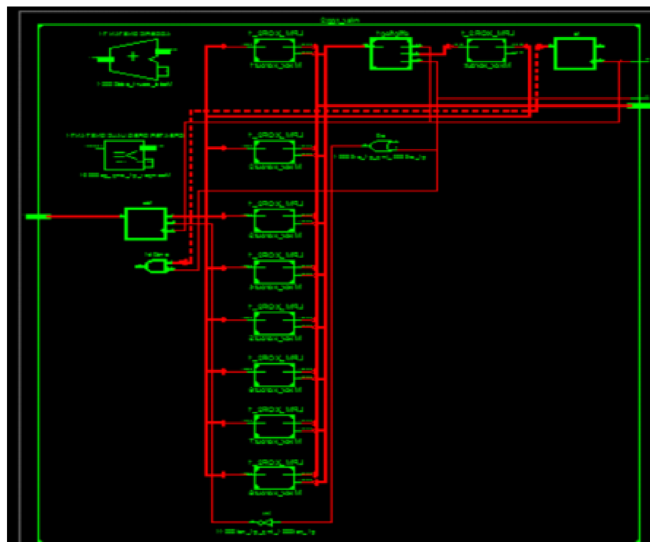


Fig. 7. 8 bit MISR schematic:

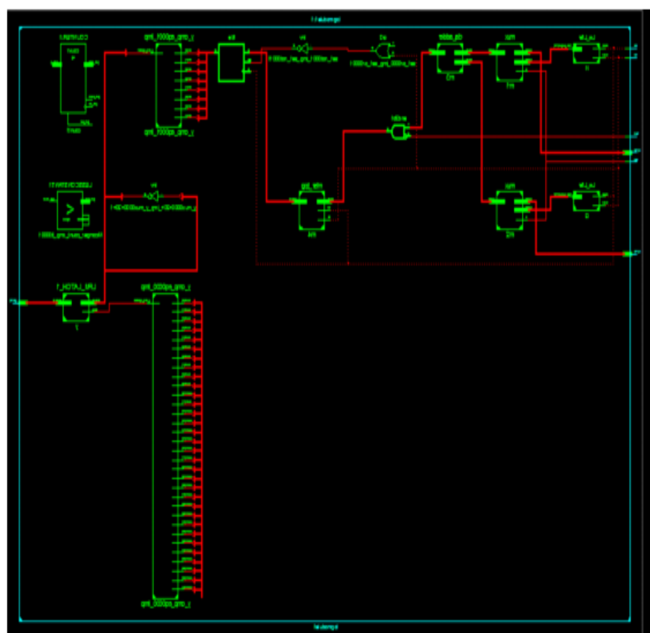


Fig. 8. RTL schematic for BIST:

This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device. The RTL schematic of total BIST architecture is shown.

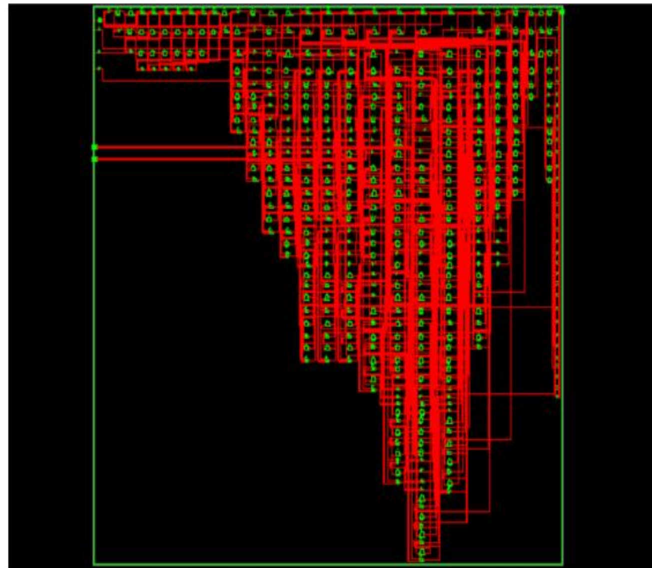


Fig. 9. Technology schematic for BIST:

This schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized to the target Xilinx device or "technology"; for example, in terms of LUTs, carry logic, I/O buffers, and other technology-specific components. Viewing this schematic allows you to see a technology-level representation of your HDL optimized for a specific Xilinx architecture, which might help you discover design issues early in the design process.

VII. CONCLUSION

This Project presented a Design and Analysis of LP LFSR i.e. Bipartite LFSR and standard LFSR architectures for Built-in
Self-Test. As testing of circuit consumes 200% more power than designing it, to reduce the testing power the transitions between the two successive patterns of LFSR are being reduced using different techniques, which reduces the testing power gradually. The Test Patterns Generators proposed in this thesis are Standard LFSR and Bipartite LFSR. These LFSR are successfully executed with BIST top module in Xilinx tool. Testing is done on an CLA circuit. The Bipartite technique is general and can be applied to almost all Test Pattern Generators. Among all the LFSR's Bipartite LFSR has the lowest power Dissipation while testing the CLA Circuit.
Our Bipartite LFSR keeps the randomness property of the n-bit LFSR intact and it also reduces the overall power consumption of Bipartite LFSR compared to LFSR because in each period of clock half of the LFSR is in the ideal mode by using two complementary enable signals (en1, en2). A considerable amount of dynamic power saving was achieved with the help of this technique. After adding it with static (or leakage) power, we got the net power saving is much less compared to other LFSR. All these calculations were with reference to Simple Linear Feedback Shift Register (LFSR).
In this project, we implemented these two LFSRs in BIST architecture and compared their power consumption. We can observe that the power is reduced in Low power LFSR since the switching activity is decreased. The

switching activity is decreased due to the intermediate patterns which were introduced in between the two patterns. Since the patterns generated are more random the overall fault coverage also increases. So the Bipartite technique has lot of advantages over other LFSR and can be used to test any circuit.

REFERENCES

[1]. M. Tehranipoor, M. Nourani, and N. Ahmed, "Low Transition LFSR for BIST-Based Application," in Proc. IEEE 14th Asian Test Symposium, 2005.

[2]. "Verilog HDL A guide to Digital Design and Synthesis" Samir Palnitkar SunSoft Press 1996.

[3]. Prathyusha Nayineni(M.Tech-VLSI),S.K. MASTHAN M.Tech,"Power Optimisation for BIST Circuitry Using Low Power LFSR",IJCTT Volume 2Issue2- 2011.

[4]. "Digital systems design and testable design" By_Miron Abramovici,Melvin a.breuer,Arthur d.friedman.

[5]. P. Girard, "Survey of Low-Power Testing of VLSI Circuits," IEEE Design & Test of Comput-ers, vol. 19, no. 3, pp. 80–90, May-June 2002.

[6]. P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A Test Vector Inhibiting Technique for Low Energy BIST Design," in Proc. IEEE 17th VLSI Test Symp., Apr. 1999, pp. 407–412.

[7]. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, "Low Energy BIST Design: Impact of the LFSR TPG Parameters on the weighted Switching Activity," in Proc. International Symp. Circuits and Systems, June, pp. 110–113.

[8]. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. J. Wunderlich, "A Modified Clock Scheme for a Low Power BIST Test Pattern Generator," in Proc. IEEE 19th VLSI Test Symp., May 2001, pp. 306–311.

[9]. P. Girard, N. Nicolici, and X. Wen, editors, Power-Aware Testin and Test Stargegies for Low Power Devices. Springer, 2009.

[10]. Ahmed N.Awad & Abdallatif S.Abu-Issa "Low Power Address Generator for Memory Built- In Self Test" The Research Bulletin of Jordan ACM, Vol II(III).

[11]. A. S. Abu-Issa and S. F. Quigley, "Bit-Swapping LFSR and ScanChain Ordering: A Novel Technique for Peak and Average-Power Reduction in Scan-Based BIST," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 5, May 2009.

[12]. S. Wang, "Generation of Low Power Dissipation and High Fault Coverage Patterns for Scan-Based BIST," in Proc. International Test Conf., Dec. 2002, pp.834–843.

[13]. J. Rajski et al., "Test Generator with Preselected Toggling for Low Power Built In Self- Test,"in Proc. IEEE 29th VLSI Test Symp., 2011.

[14]. S. Wang and S. K. Gupta, "DS-LFSR: A New BIST TPG for Low Heat Dissipation," in Proc. International Test Conf., Nov. 1997, pp. 848–857.

[15]. X. Zhang, K. Roy, and S. Bhawmik, "POWERTEST: A Tool for Energy Conscious Weighted Random Pattern Testing," in Proc. 12th International Conf. VLSI Design, Jan. 1999, pp. 416–422.

[16]. S. Wang and S. K. Gupta, "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," in Proc. International Test Conf., Sept. 1999, pp. 85–

[17]. D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian, “Low Power/Energy BIST Scheme for Datapaths,” in Proc. IEEE 18th VLSI Test Symp., May 2000, pp. 23–28.

[18]. R. M. Chou, K. K. Saluja, and V. D. Agrawal, “Power Constraint Scheduling of Tests,” in Proc. 7th International Conference VLSI Design, Jan. 1994, pp. 271–274.

[19]. A. Hertwig and H.-J. Wunderlich, “Low Power Serial Built-In Self-Test,” in Proc. European Test Workshop, May 1998, pp. 49–53.

[20]. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, “Low Energy BIST Design: Impact of the LFSR TPG Parameters on the Weighted Switching Activity,” in Proc. International Symp. Circuits and Systems, June, pp. 110–113.

[21] Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST,IACC-2009)