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A BRIEF STUDY ON CHALLENGES OF MOSFET AND EVOLUTION OF FINFETS

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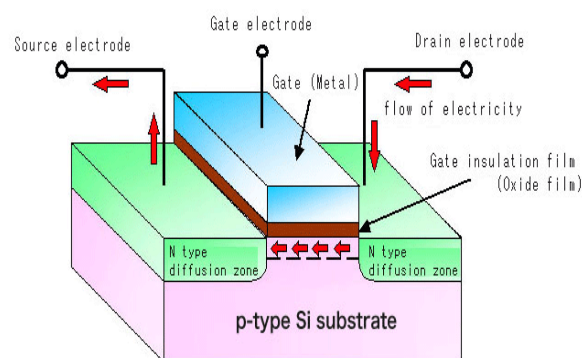
ABSTRACT

The present trend in engineering field is nano.Nano technology is found in all engineering and bio medical applications. All the analog and digital circuits of electronic fields are designed using transistors. The present scenario of chip designing is using nanolength channel transistors This paper has a study of nano scaling challenges of MOSFET, evolution of FinFET.

Keywords*: *Challenges of MOSFETs, FinFETs

I INTRODUCTION

The rapid progress of silicon technology is continuing with present generation technologies of gate lengths less than 22 nm. Moore's law states the scaling of ICs, which carried out a lot of research in Nano world. Early years of silicon era used MOSFETs for designing the circuits. Many research articles have been published that demonstrate the improved short-channel effects of conventional bulk MOSFETs [1-4,5-7]. FinFET and Trigate devices have been explored thoroughly in the past decade [8–15]. Power Challenges introduced by nanometre gate length are Short Channel effects and Variability. Section II introduces the Short channel effects(SCE) [18].Change of Materials to over come SCE is discussed in Section III .Various technologies have evolved to overcome short channel effect which is introduced in Section IV [16]. FinFETs are studied in section V[16,18].



Construction of MOSFET

Figure: 1 Structure of MOSFET

II SHORT CHANNEL EFFECTS

For MOSFET gate length less than 10nm, the mechanical tunnelling from source to drain becomes significant. Tunnelling degrades the sub threshold slope and increases the leakage current in OFF State [17].Different Physical Phenomena contribute to Short channel effects. The OFF- current of Short channel Transistors is influenced by Threshold voltage, Channel Physical dimensions, Channel doping, Drain/Source Junction depths, gate oxide thickness , The supply voltage, Drain and Gate Voltages.

Different Short channel leakage currents are Weak Inversion, Drain Induced Barrier-Lowering Effect, Gate Induced Drain Leakage and Punch through.

III CHANGE OF MATERIALS

To increase the power and speed of the circuits, the size of the transistors are shrinked. To Shrink the device, gate length is reduced (W/L ratio),if Channel length reduces, Oxide thickness must be reduced. If Oxide thickness gets small (nm),device leaks. But Oxide thickness must shrink with the device. This effects the control of gate over the channel. Two choices to overcome the effect of Dennard'scaling[20].
a) Change Materials of transistor: To reduce the size ,thickness of oxide layer must be reduced but capacitance across oxide must be constant.

$C_{ox} = \epsilon_{ox} K A/T_{ox}$ [20]

K- Dielectric constant, A- Area

C_{ox}- Oxide Capacitance, T_{ox}- Oxide Thickness

Dielectric constant must be increased to maintain constant oxide capacitance as shown in the equation. Therefore change of material from silicon dioxide layer to Hfo_2. Dielectric constant of Hfo2 increases by four times than Silicon oxide layer.

IV CHANGE GEOMETRY OF TRANSISTOR

To Overcome SCE and Variability new technologies in geometry of transistors were introduced [16].Such as

a) Strained Silicon: Thin silicon layer is deposited over the silicon germanium substrate. As silicon atoms align with silicon germanium substrate, the links between silicon atoms are stretched or compressed which leads to strained silicon. This reduces the atomic forces, which inturn increases the mobility of electron. Higher mobility increases performance of the device .Shown in Figure 1

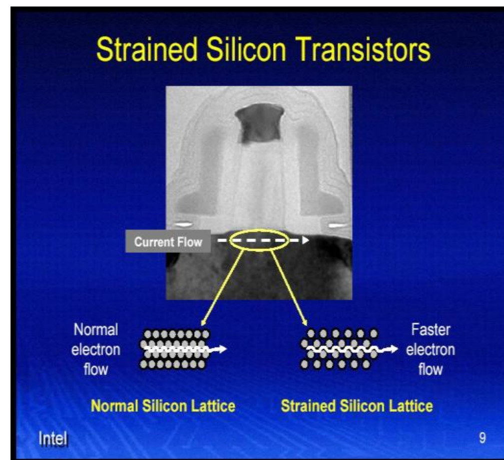


Figure: 2 Strained Silicon Transistors

b) Hetero Junction devices: Hetero structures developed by Stanford has larger carrier mobility but requires larger time.

c) Silicon on Insulator: The channel is formed in a thin layer of silicon deposited above an electrical insulator. This structure reduces junction capacitance which inturn reduces power.Other advantages are higher subthreshold slope factor, reducing leakage, reduced impact of soft errors, but more expensive and has secondary effects. Silicon on insulator are classified as FD-SOI(fully depleted silicon on insulator),PD-SOI(partially depleted silicon on insulator). Shown in Figure 2

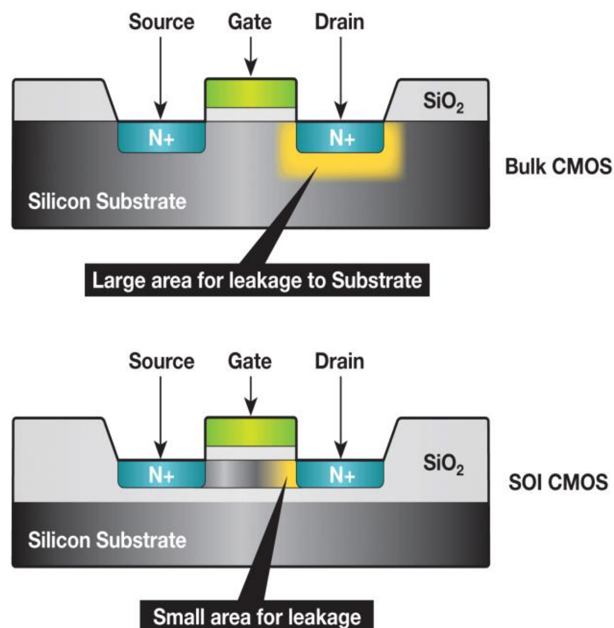


Figure: 3 Structure of CMOS and SOI-CMOS

V FinFET

FinFETs are replacing Bulk CMOS devices at NanoScale. The term FinFET was given by researchers at university of California at Berkely. Unlike MOSFET the gate is wrapped around a thin Silicon Fin which forms the body of the device. Channel length determines the dimensions of FinFET. The device structure shows the potential to scale the channel length to values that are impossible to accomplish in traditional planar devices. Operational transistors with channel lengths of 7nm had been demonstrated [16].

Structure of FinFET consists of a thin vertical Fin on a substrate which runs between source and drain. Gate is wrapped around the Fin structure in traverse form. Electrical control over the channel conduction is improved by this type of gate structure, as well overcomes the short channel effects. The term FinFET is ued generically to describe any Fin-Based, Multi-gate Transistors.

Depending on the structure of FinFET , different types of FinFETs are available such as double gateFinFET, Multi gate FinFET, Trigate FinFET, Omega –FinFET, All Around Gate FinFET(AAG).Both FullyDepleted SOI and DGFinFET have similar advantages, but DG-FinFET has relaxed constriant of channel thickness.Therefore FinFETs are more Scalable thanFD-SOI.Among all multigate FETs, Double gate and Trigate FinFETs aremost popular for their simple structure and ease of fabrication.Two or three gates wrapped arounda vertical channel enable easy alignment of gates.[18]

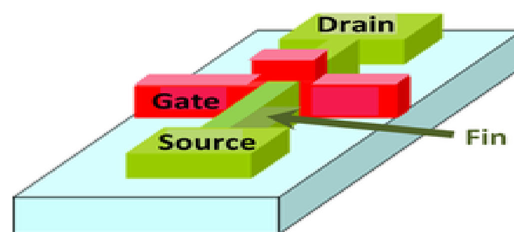


Figure: 4 Structure of FinFET

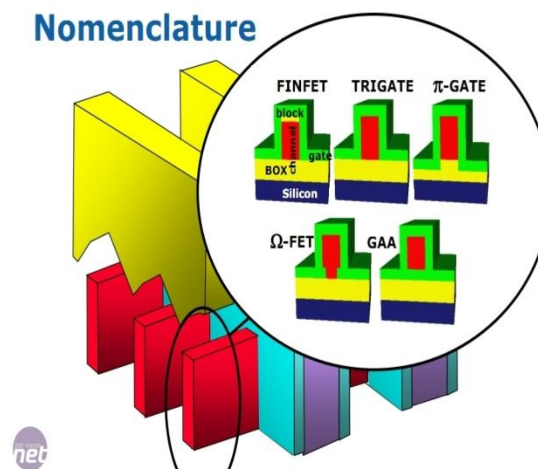


Figure:5 Different Structures of FinFET

VI CONCLUSION

This paper has a study of Nano scaling Challenges of MOSFETS, which are nothing but short channel effects and variability. To overcome this, different structures have been discussed. Finally FinFETs have been studied.

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