International Journal of Advanced Technology in Engineering and Science
Vol. No.5, Issue No. 03, March 2017
www.ijates.com
ijates
ISSN 2348 - 7550

DESIGN AND OPERATION OF A SINGLE PHASE DC-AC MULTILEVEL CONVERTERS WITH UNBALANCED DC SOURCE

Vanam Venkatesham [1], Santhosh Kumar Edukulla[2]

[1,2]*Assistant professor, Dept of EEE, Khader Memorial College of Engineering & Technology, JNTUH, TS, (India)*

ABSTRACT

The increase of transmission frequency reveals more merits than low- or medium-frequency distribution among different kinds of power applications. High-frequency inverter serves as source side in high-frequency ac (HFAC) power distribution system (PDS). However, it is complicated to obtain a high-frequency inverter with both simple circuit topology and straightforward Modulation strategy. A novel switched-capacitor-based cascaded multilevel inverter is proposed in this paper, which is constructed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched capacitor frontend increases the number of voltage levels. The output harmonics and the component counter can be significantly reduced by the increasing number of voltage levels. A symmetrical triangular waveform modulation is proposed with a simple analog Implementation and low modulation frequency comparing with Traditional multicarrier modulation. The circuit topology, symmetrical modulation, operation cycles, Fourier analysis, parameter Determination, and topology enhancement are examined. An experimental prototype with a rated output frequency of 25 kHz is implemented to compare with simulation results. The experimental results agreed very well with the simulation that confirms the feasibility of proposed multilevel inverter.

Keywords: Cascaded H-Bridge, high-frequency ac (HFAC), multilevel inverter, switched capacitor (SC), symmetrical phase shift modulation (PSM).

I. INTRODUCTION

High-frequency ac (HFAC) power distribution system (PDS) potentially becomes an alternative to traditional dc distribution due to the fewer components and lower cost. The existing applications can be found in computer, telecom, electric vehicle, and renewable energy micro grid. However, HFACPDS has to confront the challenges from large power capacity, high electromagnetic interference (EMI), and severe power losses [6]. A traditional HFAC PDS is made up of a high-frequency (HF) inverter, an HF transmission track, and numerous voltage-regulation modules (VRM). HF inverter accomplishes the power conversion to accommodate the requirement of point of load (POL). In order to increase the power capacity, the most popular method is to connect the inverter

output in series or in parallel. However, it is impractical for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity is easy to be achieved by multilevel inverter with lower switch stress. Non polluted sinusoidal waveform with the lower total harmonic distortion (THD) is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of stair case out put, thus significantly simplifying the filter design. HF power distribution is applicable for small-scale and internal closed electrical network in electric vehicle (EV) due to moderate size of distribution network and effective weight reduction. The consideration of operation frequency has to make compromise between the ac inductance and resistance, so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application.

The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor-clamped type. The former uses diodes to clamp the voltage level, and the latter uses additional capacitors to clamp the voltage. The higher number of voltage levels can then be obtained; however, the circuit becomes extremely complex in these two topologies. Another kind of multilevel inverter is cascaded H-Bridge constructed by the series connection of H-Bridges. The basic circuit is similar to the classical H-bridge DC–DC converter. The cascaded structure increases the system reliability because of the same circuit cell, control structure and modulation. However, the disadvantages confronted by cascaded structure are more switches and a number of inputs. In order to increase two voltage levels in staircase output, an H-Bridge constructed by four power switches and an individual input are needed. Theoretically, cascaded H-Bridge can obtain staircase output with any number of voltage levels, but it is inappropriate to the applications of cost saving and input limitation.

II. SC-BASED CASCADED INVERTER WITH NINE-LEVEL OUTPUT

The proposed circuit is made up of the SC frontend and cascaded H-Bridge backend. If the numbers of voltage levels obtained by SC frontend and cascaded H-Bridge backend are $N1$ and $N2$, respectively, the number of voltage levels is $2 \times N1 \times N2+1$ in the entire operation cycle.

A. Circuit Topology

Fig. 1 shows the circuit topology of nine-level inverter ($N1$ =2, $N2$ = 2), where $S1$, $S2$, S_1 , S_2 as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of $C1$ and $C2$. $S1a$, $S1b$, $S1c$, $S1d$, $S2a$, $S2b$, $S2c$, $S2d$ are the switching devices of cascaded H-Bridge. $Vdc1$ and $Vdc2$ are input voltage. $D1$ and $D2$ are diodes to restrict the current direction. $iout$ and vo are the output current and the output voltage, respectively. It is worth noting that the backend circuit of the proposed inverter is cascaded H-Bridges in series connection. It is significant for H-Bridge to ensure the circuit conducting regardless of

the directions of output voltage and current. In other words, H Bridge has four conducting modes in the conditions of inductive and resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling.

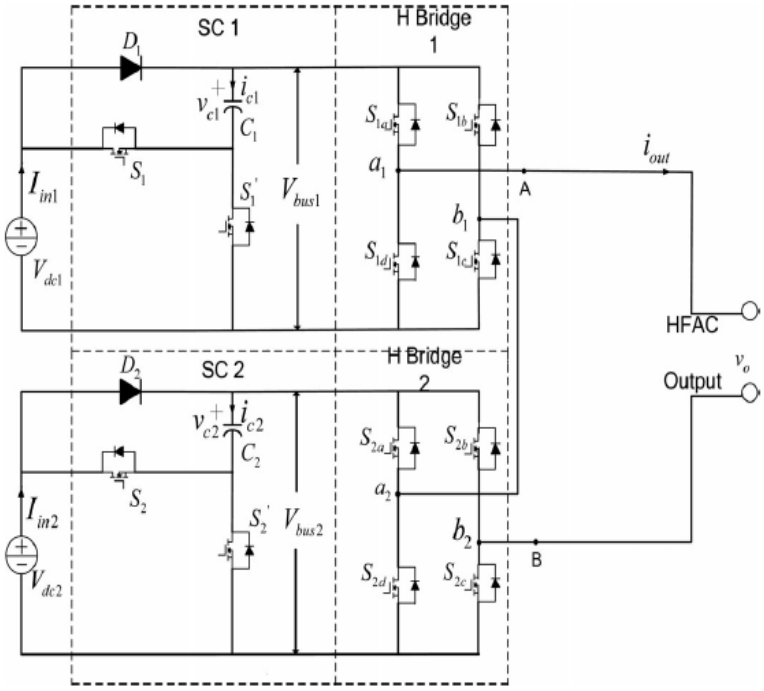

Fig.1. Circuit topology of cascaded nine-level inverter ($N1 = 2$, $N2 = 2$).

B. Symmetrical Modulation

There are many modulation methods to regulate the multilevel inverter, the popular modulations are the space vector modulation, the multicarrier PWM, and the selective harmonic elimination sub harmonic pulse width modulation, etc. However, most of them greatly increase the carrier frequency that is multiple times the frequency of reference or output. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The symmetrical PSM ensures the output voltage of full bridge is symmetrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the output frequency. The structure of symmetrical PSM and the operational waveform of symmetrical .

The logic operations of gate signals are

$$\begin{aligned} \text{gate1} &= XOR\{Q(RS), Q(D)\} \\ \text{gate2} &= XOR\{Q(RS), Q(D)\} \qquad (1) \\ \text{gate3} &= XOR\{AND\{Q(RS), NOT(PWM)\}, Q(D)\} \\ \text{gate4} &= XOR\{AND\{Q(RS), NOT(PWM)\}, \bar{Q}(D)\}. \end{aligned}$$

(2)

C. Operation Cycles

Fig. 2 demonstrates the ideal waveforms of proposed inverter. *Vc* is the triangular carrier, and *Vpp* is the peak value of *Vc*. The modulation signals of triangular carrier are *Vm* 1*c*, *Vm* 1*b*, *Vm* 2*c* and *Vm* 2*b* . *Vm* 1*b* and *Vm* 2*b* are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and δi is the duration of voltage levels controlled by them. *Vm* 1*c* and *Vm* 2*c* are used to control the alternative operations of SC1 and SC2, respectively, and αi is the duration of voltage levels controlled by them. Thus, the drive signals ofH-Bridge switches (*S*1*a*, *S*1*b*, *S*1*c*, *S*1*d*, *S*2*a*, *S*2*b*, *S*2*c*, *S*2*d*) are phase-shifted pulse signals, while the drive signals of SC switches (*S*1, *S*2, *S*_1 , *S*_2) are complementary pulse signals.

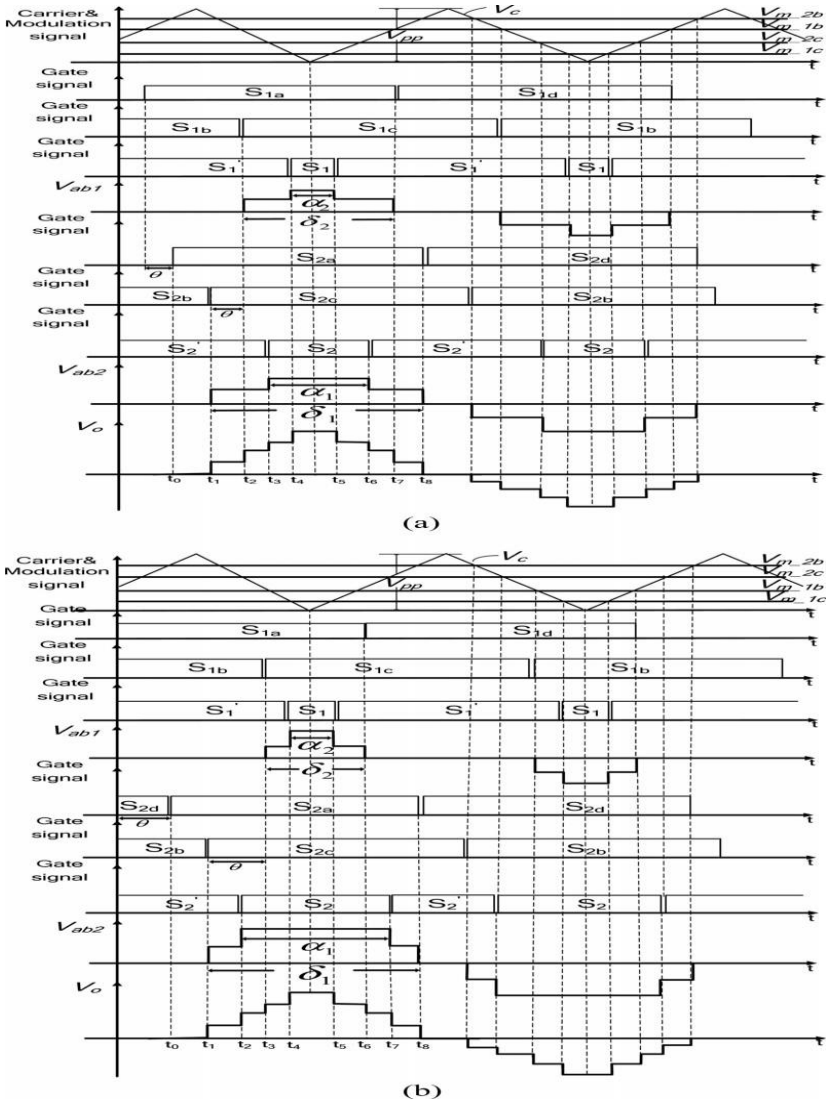

Fig.2. Operational waveforms of the proposed multilevel inverter. (a) Operational mode 1. (b) Operational mode 2.

Two operational modes are presented as shown in Fig. 2(a) and (b). Mode 1 is similar to mode 2 apart from the different positions of modulation signals ($Vm\ 1c$, $Vm\ 1b$, $Vm\ 2c$, $Vm\ 2b$). Consequently, the durations of each voltage level are controlled by modulation signals in both mode 1 and mode 2.

III.PERFORMANCE EVALUATION

A. Simulation Evaluation

The simulation based on PSIM is performed for the proposed inverter. The waveforms of output voltage vo , capacitor currents ($iC1$, $iC2$) and capacitor voltages ($vC1$, $vC2$). The following parameters are used for low power simulation. The input voltage is Vin = 12 V, the module 1 capacitor is $C1$ = 100 μF with 80 mΩ ESR, the module 2 capacitor is $C2$ = 220 μF with 50 mΩ ESR, the diodes $D1$ and $D2$ have 0.6 V forward voltage drop and 50 mΩ internal on-state resistance, and the load resistance is Ro = 12 Ω. The following parameters are used for high-power simulation. The input voltage is Vin =100 V, the module 1 capacitor is $C1$ = 300 μF with 30 Mω ESR, the module 2 capacitor is $C2$ = 560 μF with 20 mΩ ESR, and the load resistance is Ro = 12 Ω. The output frequency fs is 25 kHz.

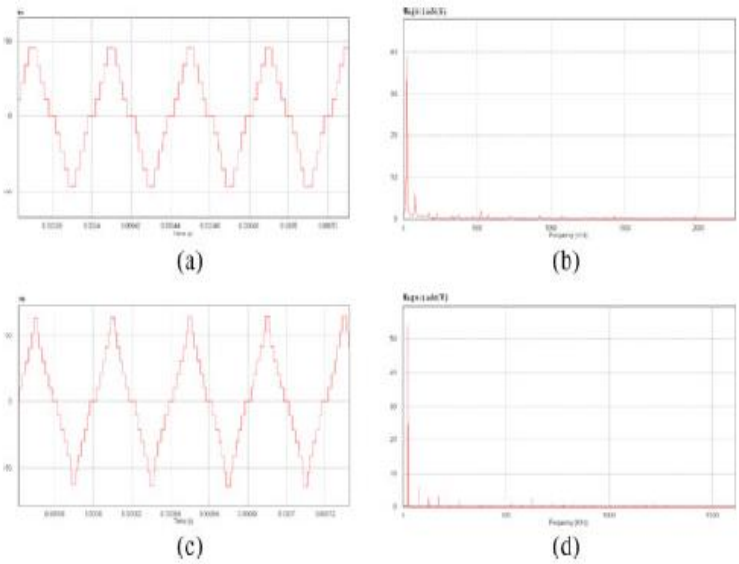

Fig. 3. Simulation waveforms of 9-level and 13-level inverter, output frequency fs = 25 kHz. (a) Output voltage of nine-level inverter ($k1 = k2 = 0.5$, $x1 = \pi/8$, $x2 = \pi/4$). (b) Spectrum of nine-level output. (c) Output voltage of 13-level inverter

B. Experiment Evaluation

An experimental prototype was implemented with output frequency of 25 kHz and output power of 50 W. The schematic of modulation circuit, that is made up of DFF, RSFF, NOT, and XOR. LM393 is a dual comparator operated at single voltage mode. The LOCMOS logic components consisting of HEF4013 (dual D flip-flop), HEF4070 (Quad 2- input XOR), HEF4081 (Quad 2-inputANDgate), and HEF4069 (Hex Inverters) accomplish the

symmetrical PSM. 5 V output in CMOS logic is magnified by boot-strap IC IR2113 to drive power switches. The schematic of power circuit is same as shown in Fig. 1. The switching devices are IRF540 MOSFETs with about 50 mΩ on-state resistances. Capacitor *C*1 is 100 μF electrolytic capacitor with ESR 80 mΩ, while *C*2 is 220 μF electrolytic capacitor with ESR 50 mΩ. *V*in is 12 V supplied by dc power supply KIKUSUI PAS40-9. The switching frequency of H-bridge backend is 25 kHz, while the switching frequency of SC frontend is 50 kHz. *Ro* is 12 Ω resistive load.

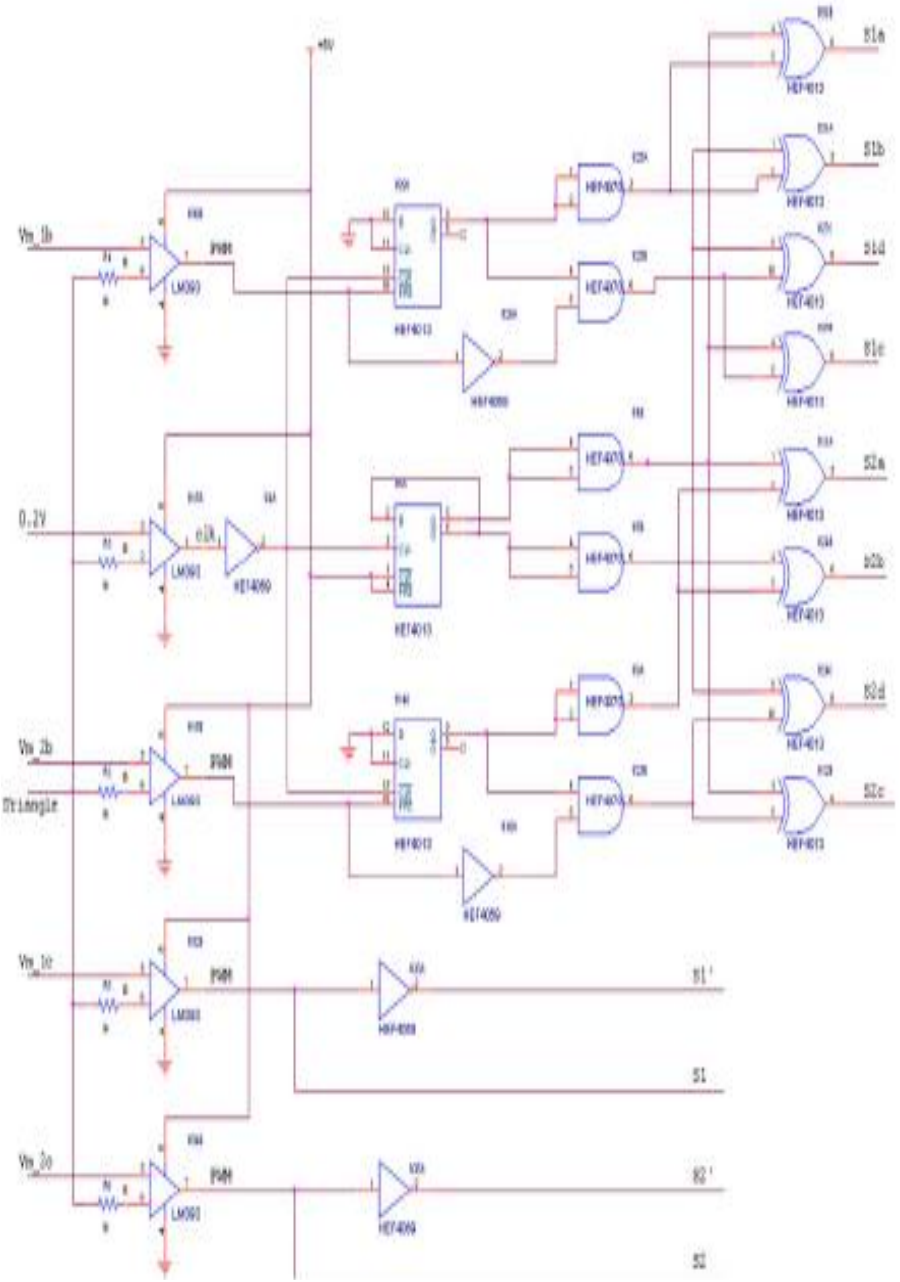

Fig.4. Schematic of modulation circuit

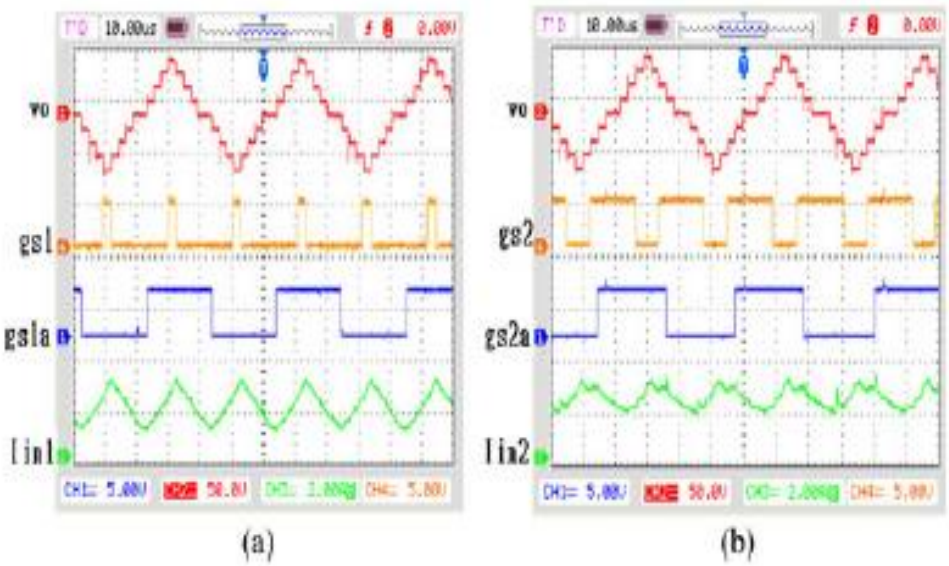

Fig.5. Observed waveforms of output voltage, gate drivers, input currents with 25 kHz frequency and 12 Ω load (*k*1 = *k*2 = 0.5, *x*1 = *π*/8, *x*2 = *π*/4). (a) Upper trace: output voltage *vo* ; second trace: *S*1 gate driver *gs*1 ; third trace: *S*1*a* gate driver of *gs*1*a* ; lower trace: input current *I*in1 . (b) Upper trace: output voltage *vo* ; second trace: *S*2 gate driver *gs*2 ; third trace: *S*2*a* gate driver *gs*2*a* ; lower trace: input current *I*in2 .

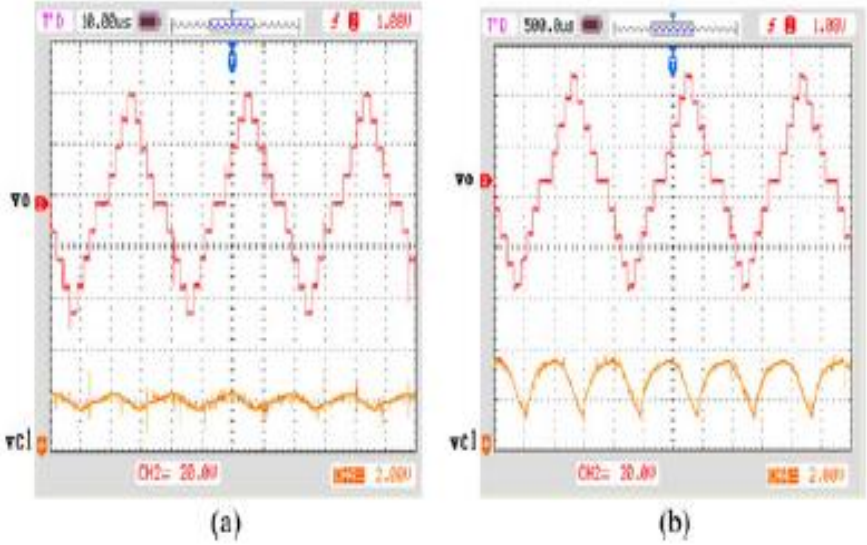

Fig.6: Observed output and capacitor voltage at condition of *k*1 = *k*2 = 0.5, *x*1 = *π*/8, *x*2 = *π*/4, and 12 Ω load. (a) Output waveforms of 25 kHz frequency. Upper trace: output voltage *vo* ; lower trace: capacitor voltage *vc* 1 . (b) Output waveforms of 500 Hz frequency. Upper trace: output voltage *vo* ; lower trace: capacitor voltage *vc* 1 .

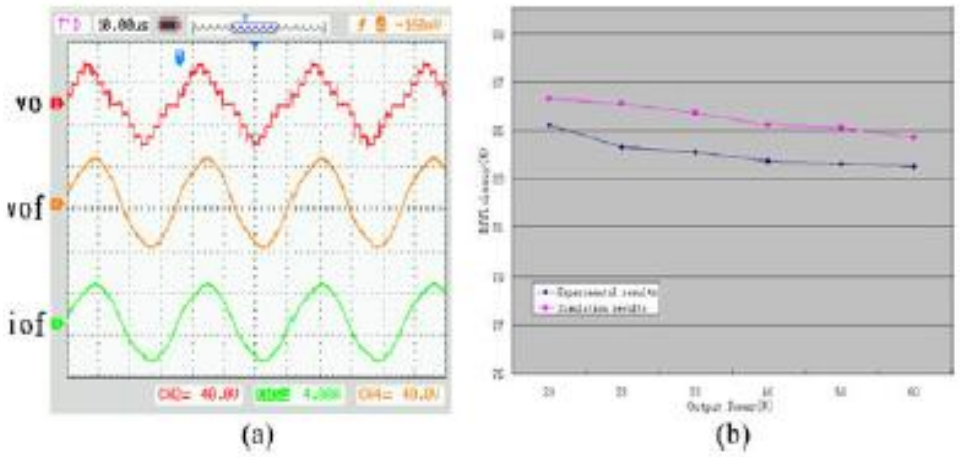

Fig.7. Output waveforms after *LC* filter and conversion efficiency. (a) Upper trace: staircase output *vo* ; middle trace: output voltage after *LC* filter *v*of ; lower trace: output current after *LC* filter *i*of . (b) Conversion efficiency comparisons of nine-level inverter with 25 kHz output under the condition of $k1 = k2 = 0.5, x1 = \pi/8, x2 = \pi/4$.

IV CONCLUSION

In this paper, a novel SC-based cascaded multilevel inverter was proposed. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation and experiment further confirm the feasibility of proposed circuit and modulation method.

REFERENCES

[1] P. Jain and H. Pinheiro, "Hybrid high frequency AC power distribution architecture for telecommunication systems," *IEEE Trans. Aerospace Electron. Syst.*, vol. 35, no. 1, pp. 138–147, Jan. 1999.

[2] J. Drobnik, "High frequency alternating current power distribution," in *Proc. 16th Int.Telecommun. Energy Conf., (INTELEC '94)*, Oct. 30–Nov. 3, pp. 292–296.

[3] B. K. Bose, M.-H. Kin, and M. D. Kankam, "High frequency AC vs. DC distribution system for next generation hybrid electric vehicle," in *Proc. IEEE Int. Conf. Ind. Electron., Control, Instrum. (IECON)*, Aug. 5–10, 1996, vol. 2, pp. 706–712.

[4] S. Chakraborty and M. G. Simoes, "Experimental evaluation of active filtering in a single-phase high-frequency AC microgrid," *IEEE Trans. Energy Convers.*, vol. 24, no. 3, pp. 673–682, Sep. 2009.

[5] R. Strzelecki and G. Benysek, *Power Electronics in Smart Electrical Energy Networks*. London, U.K.: Springer-Verlag, 2008.

[6] Z.Ye, P. K. Jain, and P. C. Sen, "A two-stage resonant inverter with control of the phase angle and magnitude of the output voltage," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2797–2812, Oct. 2007.

AUTHOR'S PROFILE

Vanam Venkatesham is working as an Assitant professor in KHADER Memorial College of Engineering & Technology, He has completed M.Tech from JNTUH ,he has 5 years of teaching experience,his intrest of areas in research is power electronics,control systems and its applications.

Santhosh Kumar Edukulla is working as an Assitant professor in KHADER Memorial College of Engineering & Technology, He has completed M.Tech,MBA from JNTUH ,he has 8 years of teaching experience,his intrest of areas in research is power electronics, Power systems and its applications.