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MODIFIED SEVEN LEVEL MULTIPLE-POLE PWM AC–AC CONVERTERS WITH REDUCED COMPONENTS COUNT

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ABSTRACT

The proposed three-phase front-end bidirectional seven-level (7L) rectifier and rear-end 7L inverter are constructed based on multiple-pole multilevel diode-clamped (M2DCC)approach, which consist a total number of 48 diode components clamped. To achieve light weight, efficiency, and better input current quality a novel multilevel ac/dc/ac converters with reduced number of semiconductor devices is proposed in this paper. Higher n-level ac/dc/ac converter topologies offer an alternative solution to address the implications of high-switching-frequency operation. These higher n-level converters have the natural ability to achieve better efficiency with lower switching and conduction losses while operating at lower switching frequency, the number of switching devices can be further reduced based on the M2DCC concept to construct a new unidirectional front-end rectifier (M2SCR).Results obtained show that low current harmonic distortions of 5% and high power factor of 0.99 are achieved with small input inductors despite low-switching-frequency operation at 1 kHz. This seven level multiple pole ac/dc/ac converter is fed to permanent magnet synchronous motor (PMSM)

I INTRODUCTION

In this paper a novel multilevel ac/dc/ac converters with reduced number of semiconductor devices is proposed to achieve light weight, efficiency, and better input current quality Higher n-level (such as 7L) ac/dc/ac converter topologies offer an alternative solution to address the implications of high-switching-frequency operation.

To achieve better efficiency with lower switching these higher n-level converters have the natural ability and conduction losses while operating at lower switching frequency, as well as power factor correction techniques to achieve low input current distortion. It can be preserved for higher level pulsewidth modulation (PWM) converters as well .In many industries Multilevel ac/dc/ac converters (which consist of front-end rectifier and rear-end inverter) for medium- to high power motor drives are widely employed. For many applications this configuration is favorable such as heat, ventilation, and air conditioning systems; pump/blower/ traction drives; and even permanent-magnet

synchronous generator wind turbine with grid connected. To achieve optimum performance simple control techniques can be implemented, due to the advantage of decoupling both front-end source and rear-end load through a dc link.

For higher n-level the realizing dc-link capacitor voltages are the greatest problem output diode-clamped converters. Thus, it results to poorer input and output performance. In between front-end rectifier and rear-end inverter, this unbalanced condition can be solved with the introduction of a multi winding transformer connected to multi pulse diode bridge rectifiers or an additional dc/dc balancing circuit

The future development of multilevel converters involves reducing the overall cost and size needed .An additional dc/dc voltage balancing circuit would be more preferable than implementing a bulky and costly multi winding transformer among the two solutions. For the motor drive applications many classical configurations of high-power transformerless seven -level (7L)ac/dc/ac drive have been experimented . with the proposed power factor correction technique to yield a fair analysis, the performances of both the proposed front-end rectifiers with the 7L-M2DCI are evaluated. The simulation results obtained along with the verified theoretical analysis have proven the feasibility of the proposed topologies for any ac/dc/ac drive applications.

Good overall performance is also achieved while operating at low switching frequency. The 7L ac/dc/ac drives based on the proposed multiple pole multilevel diode-clamped converter (M2DCC) approach presented in this paper drastically reduce the number of power diodes required.

II. OPERATING PRINCIPLES OF 7L AC/DC/AC TOPOLOGIES

Based on the classical MDCC and the proposed M2DCC approaches this section presents the operating principles of three different 7L ac/dc/ac PWM converters. The derivation of the proposed M2DCR and M2SCR topologies are explained here, whereas the proposed M2DCI topology is detailed .

Seven Level Multiple Pole PWM AC-AC Converter

In this paper the work is extended to seven level multiple pole PWM AC-AC converter. For obtaining seven levels output at the inverter side two more switches and two more diodes are added in each pole for every phase at both rectifier side and inverter side of five level multiple pole PWM AC-AC converter. The controlling circuit for five level multiple pole PWM AC-AC converter is extended to control triggering pulses for seven level multiple pole PWM AC-AC convert

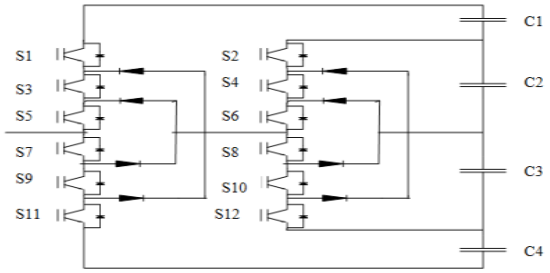

Fig. 1Seven level multiple polediode clamped network.

The 7L voltage stepped waveform is obtained with the switching positions based on a single-pole circuit configuration. It can be observed directly that the phase voltage levels are achieved across the point Va to the neutral point m.The classical 7L-MDCC ac/dc/ac converter is a back-to-back (BTB) configuration clamped inverter. In seven level multiple pole diode clamped converter 12 IGBT switches and 8 clamping diodes are used. In overall 72 IGBT switches and 48 clamping diodes utilised. But in classical method 60 clamping diodes are required. So 12 diodes are saved

III PROPOSED SEVEN LEVEL MULTIPLE POLE PWM AC-AC CONVERTER FED TO PMSM.

3.1 Permanent Magnet Synchronous Machine

The permanent-magnet synchronous machine (PMSM) drive has emerged as a top competitor for a full range of motion control applications. For example, in high-power applications the PMSM is widely used in machine tools, robotics, actuators, and is being considered such as vehicular propulsion and industrial drives.

The PMSM is known for having high efficiency, low torque ripple, superior dynamic performance, and high power density. For commercial/residential applications it is also becoming viable. For high-performance applications these drives often are the best choice and are expected to see expanded use as manufacturing costs decrease. In some instances it is referred to as a brushless DC (BDC) machine because by appropriate control it can be made to have input/output characteristics much like a separately excited brush-type DC machine The PMSM is sometimes referred to as a permanent-magnet AC (PMAC) machine or simply as a PM machine.

In the rotorthe use of permanent magnets facilitates efficiency, eliminates the need for slip rings, and eliminates the electrical rotor dynamics that complicate control (particularly vector control). The PMSM also has the drawback of requiring rotor position feedback by either direct means or by a suitable estimation system. The permanent magnets have the drawback of adding significant capital cost to the drive, although the long term cost can be less through improved efficiency

To produce the air gap magnetic field rather than using electromagnets a permanent magnet synchronous motor (PMSM) is a motor that uses permanent magnets. For use in many applications these motors have significant advantages, attracting the interest of researchers and industry. Basically, at as a transformer a PMSM machine can be looked with a moving secondary, where the coupling coefficients between the stator and rotor phases change continuously with the change of the rotor position. The machine model can be described by differential equations with time-varying inductances which are functions of the rotor position. However, such a model tends to be very complex because of the time varying inductance coefficients and associated inductance matrix. which is usually called the d-q Park's transformation, or thetwo-reaction theory. Through this method, in the three-phase stationary reference frame the variables will be transformed to constants in the synchronously rotating reference frame, which is also called d-q reference frame.The voltage transformation can be written as follows:

$$\begin{bmatrix} V_d \\ V_d \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\frac{2\pi}{3} - \theta\right) & \cos\left(\frac{2\pi}{3} + \theta\right) \\ \sin\theta & \sin\left(\frac{2\pi}{3} - \theta\right) & \sin\left(\frac{2\pi}{3} + \theta\right) \\ 0.5 & 0.5 & 0.5 \end{bmatrix}$$

$$V_d = R_s i_d + \frac{d\lambda_d}{dt} - \omega_e \lambda_q$$

$$V_q = R_s i_d + \frac{d\lambda_d}{dt} + \omega_e \lambda_q (1)$$

$$\lambda_d = L_d i_d + \lambda_{pm}$$

$$\lambda_a = L_a i_a$$

Where, Ld is the d-axis inductance, Lq is the q-axis inductance, and pm is the amplitude of flux linkage due to the permanent magnet. According to a dynamic equivalent circuit of a PMSM in the d-q frame can be drawn as shown in figure 7.

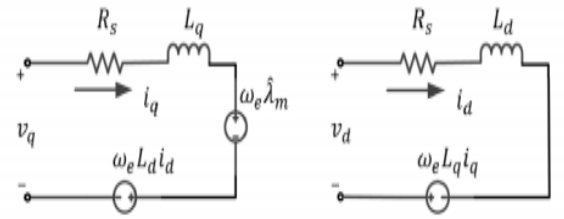

Fig 2 Equivalent circuit of aPMSM

In the d-q frame, the input power of a PMSM can be written as

$$P_{in} = \frac{3}{2}(V_d i_d + V_q i_q) \quad (2)$$

Assuming the motor losses are negligible, then the input power equals the output power, out of the motor, which can be represented as follows

$$P_{out} = \frac{3}{2}\omega_e(\lambda_{pm} i_q + (L_d - L_q) i_d i_q) \quad (3)$$

Since the output power is a product of the motor mechanical speed time the developed/output torque, the output torque can be obtained as:

$$T_e = \frac{P_{out}}{\omega_m} = \frac{p3}{22}(\lambda_{pm} i_q + (L_d - L_q) i_d i_q) \quad (4)$$

The 7L voltage stepped waveform is obtained with the switching positions based on a single-pole circuit configuration. It can be observed directly that the phase voltage levels are achieved across the point Va to the neutral point m.The proposed 7L-M2DCC topology is configured with two classical 3L-MDCC cells (Outer cell—Cell 2 and Inner cell—Cell 1) . Hence, the 7L input and output voltage stepped waveforms are achieved with the proposed multiple-pole configuration according to the corresponding switching state listed in Table I.

TABLE I

SWITCHING LOGIC FOR RESPECTIVE IGBT IN 7L-M 2 DCC TOPOLOGY

IGBT state						State Name
S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	
1	1	0	0	0	0	Saa
0	0	1	1	0	0	Sbb
0	0	0	0	1	1	Scc
1	0	0	0	0	0	S1
1	0	1	0	0	0	S2
0	1	0	1	0	0	S3
0	0	0	1	0	0	S4
0	0	1	0	0	0	S5
0	0	1	0	1	0	S6
0	0	0	1	0	1	S7
0	0	0	0	0	1	S8
1	0	0	0	1	0	S9
0	0	0	0	1	0	S10
0	1	0	0	0	0	S11
0	1	0	0	0	1	S12

However, in this proposed topology when the number of cells increases, a total number of 6(*n*-3) diode components are reduced.

Based on the multiple pole hierarchy the 7L voltage stepped waveform of the M2DCC topology is achieved with the switching positions.

3.2 Proposed Unidirectional Front-End 7L M2SCR WithRear-End 7L-M2DCI Topology

To achieve 7L input voltage stepped waveform each phase leg of the proposed unidirectional 7L-M2SCR also requires two cells, as shown. For certain ac/dc/ac drive applicationsa bidirectional power flow in the front-end rectifier is not required such as propulsion, compressor, or any non regenerative braking system. Thus, a proposed transformerless front-end unidirectional rectifier is reconstructed in Fig. 3 with the arrangement of the semiconductor devices in the bidirectional M2DCR configuration

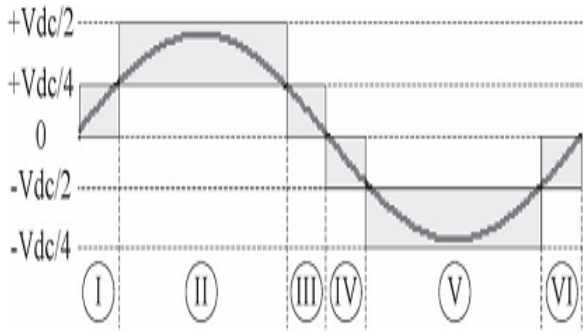

Fig. 3. Incremental input and output voltage steppedwaveform of a BTB ac/dc/ac drive.

f o l low s

For the outer cell and similarly for the inner cell the states selection of the top and bottom diodes of a M2SCR is dependent on 1-Sa1 and 1-Sa2. Hence, only two switching devices are required in each cell, with four series diodes connected to the terminals of the capacitors in the dc link. Due to lesser number of switches needed, higher power efficiency is achieved with lesser switching and conduction losses. To the neutral-point clamped of the four dc-link capacitors the two switching devices (Sa3 and Sa4) of the inner cell are connected directly, whereas the other two switching devices (Sa1 and Sa2) of the outer cell are clamped to the output terminals of the inner cell..

3.3 General Characteristic of the Classical and Proposed7L AC/DC/AC Converters

The proposed 7L ac/DC/AC converters of general characteristics of the classical is explained. The front-end rectifier and the rear-end inverter of 7L ac/dc/ ac drives are operated independently with same level-shifted PWM (LS-PWM). To achieve the desired switching signals the LS-PWM requires a reference signal and a set of four 1-kHz triangular carriers for the respective semiconductor switches. The switching function of the LS-PWM technique for the7L rectifiers and inverters is expressed as

$$\begin{cases} S_{a1}(t) = T_{a1}(t) = 2m_a \sin \omega t - 1 \\ S_{a2}(t) = T_{a2}(t) = 2m_a \sin \omega t \end{cases}$$

$$\begin{cases} S_{a3}(t) = T_{a3}(t) = 2m_a \sin \omega t + 1 \\ S_{a4}(t) = T_{a4}(t) = 2m_a \sin \omega t + 2 \end{cases} \qquad (5)$$

where*ma* is the ratio of two times the fundamental component of pole voltage to the dc-link voltage.

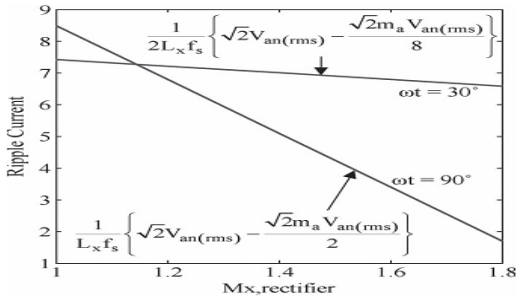

Fig.4. Ripple current versus modulation ratio of rectifier

Under the condition of steady state and balanced dc-link voltage, the general incremental output pole voltage equation is expressed as

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1}\left(\sum_{i=1}^{n-1} T_{xi} - \frac{n-1}{2}\right) \qquad (6)$$

where*Txi*is the switching states of each switching device depicted in the inverter side.*x*represents phase "a," "b," and "c;" and *n* is the number of voltage level. The voltage transfer ratios of the converters system between the dc bus voltage to the input and output voltage are defined as

$$\begin{cases} M_{x,rectifier}(t) = \frac{V_{dc}(t)}{V_{L-L}(t)}, M_{x,rectifier}(t) > 1 \\ M_{x,rectifier}(t) = \frac{2V_{xm}(t)}{V_{dc}(t)}, M_{x,rectifier}(t) \leq 1 \end{cases} \quad (7)$$

whereVxm(t) is the output pole voltage referred to the inverter side . Vx, L−L(t) is the line-to-line grid voltage.

IV. HIGH-POWER-FACTOR OPERATION OF THREE-PHASE 7L M 2DCR AND M2SCR RECTIFIERS

A. Semiconductors Voltage and Current Stresses

For the respective front-end rectifiers are derived with the switching function in (1) and based on the the voltage and current stress expressions following

The voltage and current stress expressions for the respective front-end rectifiers are derived with the switching function in (1) and based on the following In the converter design voltage and current stresses are the dominant factors considered, so that the converter can achieve optimum performance with higher reliability. For the proposed front-end rectifiers Proper selection of device rating is determined based on the global stress analysis. The maximum voltages across the power devices of unidirectional 7L-M2SCR and bidirectional 7L-M2DCR are respectively expressed in the following:

$$\begin{cases} V_{Da1} = \frac{3V_{dc}}{4} \\ V_{Da4} = V_{sa1} = \frac{3V_{dc}}{8} \\ V_{Da2} = V_{Da3} = V_{sa2} = \frac{V_{dc}}{4} \end{cases} \quad \textbf{(8)}$$

$$\begin{cases} V_{Sa1} = \frac{3V_{dc}}{4} \\ V_{Sa4} = \frac{3V_{dc}}{8} \\ V_{Sa2} = V_{Sa3} = V_{Da1} = V_{Da2} = \frac{V_{dc}}{4} \end{cases} \quad (9)$$

For the power devices in the upper phase leg, Since the maximum voltage stress expressionsare (9) and (10).Using the same expressions the respective complimentary power devices in the lower phase leg are also determined. Based on the assumed five factors (1)–(5) the average current stress is analyzed over one period of the fundamental frequency For simplification, the average current stress is approximated as follows based on respective switching functions

$$I_{sa(outercell)}(t) = I_{Da(outercell)}(t) = \frac{1}{2\pi}\int_0^{2\pi} I_a \sin(\omega t) S_{a(outercell)} d\omega t$$

$$I_{Sa(innercell)}(t) = I_{Da(innercell)}(t) = \frac{1}{2\pi}\int_0^{2\pi} I_a \sin\omega t * \left[2 - \frac{4V_{am}(1)}{V_{dc}} \sin\omega t\right] S_{a(innercell)} d\omega t \quad (10)$$

According to (10). from the current stress during the positive cycle period, it is proved that, during the negative cycle of the conduction period, Unlike the case for the unidirectional 7L-M2SCR, the current only flows through the

diodes during the positive cycle conduction period. Hence, the final net average current stress of the 7L-M2DCR in Fig. 8 is found much lower compared with that of the 7L-M2SCR.

B. Input Current Shaping of the 7L-M2DCR andthe 7L-M2SCR

The reverse current through the semiconductor switches in the bidirectional 7L-M2DCR will be cancelled out. In the upper phase leg of the proposed front-end rectifiers final average current stress for the respective power devices are shown in Fig. 8.

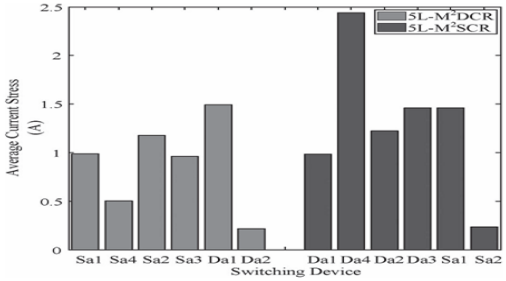

Fig.5. Average current stress level for each devices of the respective front-end rectifier topologies.

as 1.

In this case the current harmonic distortion can be minimized by increasing the switching frequency to 5 kHz and higher.when the voltage transfer ratio Mx, rectifier is greater than 1.3. This can be proved by substituting (6) into (4), where fsis observed to be cancelled away. However, the grid current distortion does not deviate much with any range of switching frequency utilized.

C. Control Theory

For the respective semiconductor switches the LS-PWM requires a reference signal and a set of six 1- kHz triangular carriers to achieve desired switching signals. The front-end rectifier and the rear-end inverter of seven level of 7L ac/dc/ac converter are operated independently with same Level- shifted PWM (LS-PWM). Under the condition of steady state and balanced dc-link voltage, the general incremental output pole voltage equation is expressed as

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1}\left(\sum_{i=1}^{n-1} T_{xi} - \frac{n-1}{2}\right) \qquad (11)$$

Where, ‘x’ represents phase “a,” “b,” and “c;” and n is the number of voltage level. High modulation index of the front-end rectifier is required to mitigate the input current distortion and achieve good voltage tracking due to its boosting effect in nature. Meanwhile, the rear-end inverter must be operated at the linear region.

In the load to prevent any high-order harmonic components incurred,there are two control loops in this to regulate the dc-link voltage and mitigate the current distortions. They are synchronous reference frame (SRF) current control and constant switching frequency modulation. To estimate peak value of reference current and to regulate the dc-link capacitor voltage the PI controller which is used as DC voltage control. To achieve high quality input sinusoidal

current with constant unity power factor SRF controller provides a good dynamic response performance and overall efficiency, and lightest weight among the other rectifier topologies.

D. Unbalanced DC-Link Capacitor Voltages

If the power converter is not adequately designed, the unbalanced dc-link capacitor voltages may disrupt the smooth operating system and affect the global reliability. By overstressing the limited blocking voltage capability of the semiconductor devices this disastrous condition will damage the converter. When any fault condition occurs by disabling the rectifier/inverter operation although this undesirable condition can be typically resolved, the overall efficiency of the system may be greatly affected.

To ensure that the power device ratings are properly selected the alternative solution to overcome this issue is during the design ,according to the worst case scenarios. Thus, the maximum voltage stress across the respective power devices of the 7L rectifiers. The obtained results are co simulated between PSIM and MATLAB Simcouple. As a result, for the classical 7L rectifiers it is essential to have series-connected switches, but these additional switching devices can be avoided for the proposed 7L topologies.It should be noted in the proposed 7L rectifiers under unbalanced condition is Vdc, that the maximum voltage stress across the semiconductor switches, unlike in the classical 7L rectifiers, which will be experiencing 2Vdc (twice the dc-link voltage).

E. SRF Current Control Scheme

The proposed control algorithm with power factor correction technique is shown,to regulate the dc-link voltage and mitigate the current distortions. two control loops, i.e., synchronous-reference-frame (SRF) current control and constant switching frequency modulation, are implemented

The detailed analyses of the outer-loop dc-link voltage control and the inner-loop current control are both presented. For the dc–dc balancing circuit the balancing control is presented in [12] and [13].Due to the simplicity of the control strategy, low-cost integrated control circuit can be designed.

The unity power factor controller for the front-end 5L rectifiers (M2DCR or M2SCR) designed is based on the SRF current control with the LS-PWM technique.

To achieve high quality input sinusoidal current with constant unity power factor performance SRF controller provides a good dynamic response. Under steady-state condition the open-loop transfer function of the dc-link voltage control is written as follows to achieve a stable control system:

$$L(s) = \frac{K_p s + K_I}{s} \cdot \frac{L_x I_d}{C_{eq} V_{dc}} \cdot \frac{\left(\frac{\sqrt{3} V_p}{L_x I_d} - s\right)}{s + \left(\frac{I_{dc}}{C_{eq} V_{dc}}\right)} \qquad (12)$$

where Id is the peak value of the reference current, which is obtained from the summation of Idc (output of dc voltage control) and feed forward current (output of Kf). Ceq and Lx are the equivalent capacitance of the dc bus

and the input (phases a, b, and c) filter inductance with the values of 600 μF and 5 mH, respectively. Kp and KI are the proportional and integral parameters of the dc voltage control loop selected at 0.4 and 15, respectively. Vp is the RMS value of the grid phase voltage, and Vdc is the mean value of the dc link voltage. The feed forward current control loop under steady-state condition is derived based on the power balanced principle, which is expressed in the following:

$$K_f = \frac{V_{dc}}{\sqrt{3}V_p} \qquad (13)$$

where Vp is the RMS value of the grid phase voltage.

V. SIMULATION RESULTS

The operation of the proposed bidirectional 7L-M 2DCR has been evaluated with the power factor control under various load conditions. Figs. 9 and 10 show the unity power factor operation under two different types of loading effect. However, the proposed unidirectional 7L-M 2 SCR topology can only achieve unity power factor without any reversal power capability with same performance obtained in Fig. 9

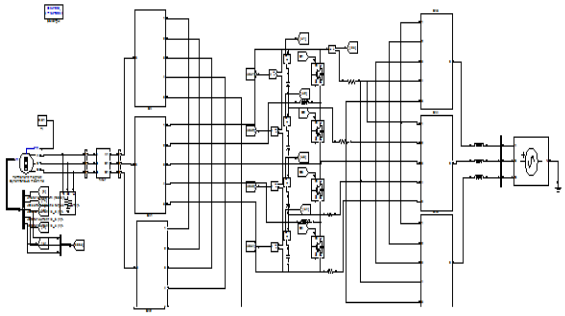

Fig 6 Block diagram of simulation

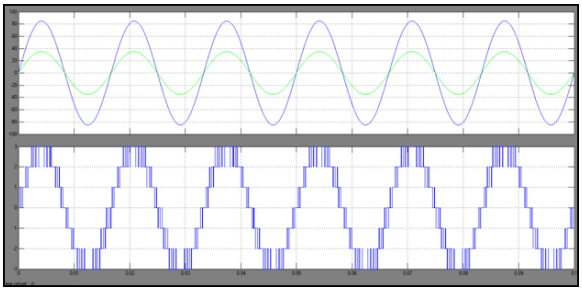

Fig. 7. Unity power factor operation with rectifying mode. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.

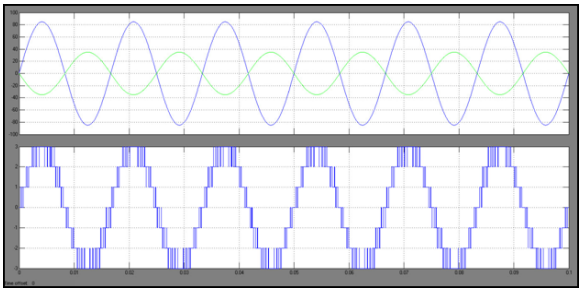

Fig. 8. Unity power factor operation with inverting mode. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.

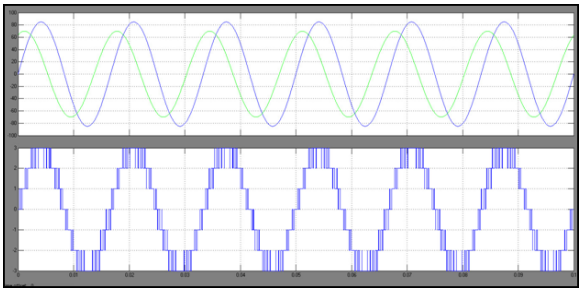

Fig. 9. Leading power factor, PF = 0 .43. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side..

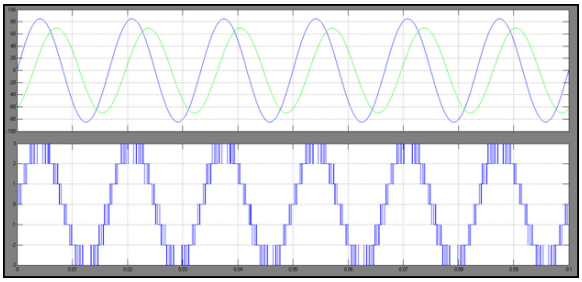

Fig. 10. Lagging power factor, PF=0.43. (a) Voltage and current at the grid side. (b) Pole voltage at the rectifier side.

TABLE II

PARAMETER SETTINGS FOR AC/DC/AC CONVERTER

System Parameters	Values
Input Grid Voltage	60 Vrms (50 Hz)
DC-Link Voltage	200 Vdc
Input Inductors (Lx)	5 mH
Mx,inverter	0.8
Switching Frequency	1 kHz

VI. CONCLUSION

In seven level multiple pole PWM AC-AC diode clamped converter Permanent Magnet Synchronous Motor is connected at output side of inverter. PMSM rotates with synchronous speed in both inverting and rectifying modes the speed and torque variations are observed. But the PMSM acts as motor in inverting mode and acts as generator in rectifying mode. To reduce the number of semiconductor devices compared with the conventional converters a new generation of front-end bidirectional 7L-M 2DCR topologies has been introduced in this paper. With low operational switching frequency of 1 kHz without the aid of any bulky LC passive filter excellent performance and low input current distortion with high power factor is achieved. In addition to that, the reduction of component counts allows the proposed converters to achieve low voltage/current stress and low switching losses.However, the dc-link voltage balancing circuit is restricted to certain power applications. These will provide a more cost-effective and energy-efficient solution for a higher level ac/dc/ac drive and can particularly be suitable for renewable energy conversion where high efficiency is paramount**.** By using simulation results we can analyze the overall converter efficiency is also improved. The size of input reactors is greatly reduced as well because of the incremental voltage stepped waveforms synthesized at low switching frequency. In the dc link this is at the small cost of having an additional voltage balancing circuitry to balance the capacitor voltages.

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