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MULTIRATE IIR LINEAR DIGITAL FILTER DESIGN FOR POWER SYSTEM SUBSTATION

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ABSTRACT

This paper presents a novel filter design of infinite impulse response (IIR) and finite impulse response (FIR) filter with different architectures has been proposed for performing high speed operation of the filter in real time systems. High speed multiplication has been an important aspect of any digital filter. Hence, in this paper, these multiplications in filter have been implemented with a canonical signed digit (CSD), factored CSD, multiplier with pipeline and without the pipeline. Though each architecture provides benefits in different aspects, the proposed filter gives a better performance in term of higher throughput with less resource utilization which has been implemented on FPGA Spartan 3E kit. This filter finds application in digital power systems.

Keywords: Intelligent Electronic Devices, Data Format Converter, Digital Filter, low pass filter, Canonical Signed Digit, low order, high speed, Group Delay.

I. INTRODUCTION

IIR filters are used in digital filter design as they need less memory and optimum number of calculations. It also provides a better performance in comparison with analog systems. For designers who, always aim to implement the filter design with less hardware requirement, IIR filter is the best approach than FIR. IIR designs can achieve the sharp magnitude response characteristic with a relatively low order, but, the phase response is non-linear. IIR filter can achieve linear phase response by a process of compensation technique. The other approach is the design for a particular cutoff frequency and decay value, followed by a FIR filter [1], which leads to adaptively compensating for the non-linear phase introduced in the IIR filter. The FIR filter, however, leaves the magnitude response unchanged.

In this paper IIR filter is designed with magnitude and group delay compensation. The filter coefficients are generated in Matlab with FDA tool and have been simulated in Xilinx ISE 14.7.

Fig. 1: Proposed Digital Data Transmit Solution.

Reliable power systems control and monitor solutions with low cost and high performance and are in high demand in deregulated power industry. The restructuring of the power industry is breaking the vertically integrated utility into competitive entities and has introduced competition into electric power markets in order to improve economic efficiency. As a result of the deregulation, cost reduction has become the utmost important strategy for every energy producer. How ever, the power industry is an intensively invested industry. At present, in a substation, a large amount of expensive control and monitoring equipment are installed to enhance security and reliable operation of the power system. However, with the progress made in the digital signal processing and telecommunication technologies, substation automation solutions with high performance can be designed with lower cost [3] In power system substations, Intelligent Electronic Devices (IED) have been installed and are replacing the conventional electromechanical or solid-state equipments, such as the digital relay, the digital fault recorder and the Remote Terminal Unit (RTU) or Phasor Measurement Unit (PMU) etc. At present, the Current Transformers (CT) and the Potential Transformers (PT) are installed in the switch yard and convert high voltage and high current signals into low voltage and low current signals[3].

II. DATA FORMAT CONVERTER DESIGNING

Filtering is the processing of a time-domain signal resulting in the reduction of some unwanted input spectral components. The filters allow certain frequencies to pass while attenuating other frequencies in the frequency domain. FIR filter is a non-recursive. The IIR filter, known as a recursive filter, uses feedback to compute output (1). The magnitude and the phase responses of the network function are the two main factors of designing the filter. The magnitude response is studied frequently in db through the gain function as in (3). The phase response is expressed by phase function or group delay function as in (4). The group delay function and the phase function have profound time-domain ramifications as they have a direct effect on the wave-shape of the output signals.

Discrete time systems with unequal sampling rate at various parts of the system are called multi rate systems. In many applications signal at a given sampling rate needs to be converted into another signal with different sampling rate.

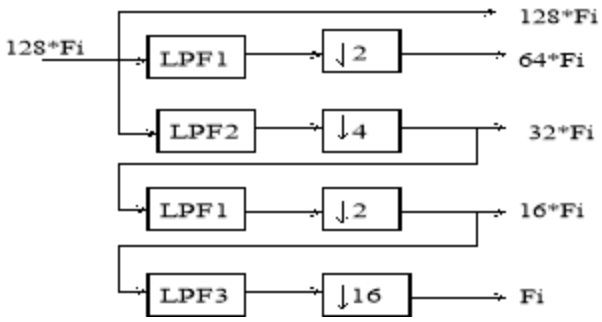

Fig. 2: Multirate Digital Data Format Converter

To achieve different sampling rates at different stages, multirate digital signal processing systems employs the down-sampler and the up-sampler, the two basic sampling rate alteration devices in addition to the conventional elements such as the adder, the multipler, and the delay.

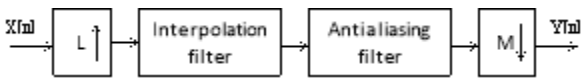

Fig. 3: Block Diagram for changing the sampling rate.

These filters are used over a wide range of sample rates and are well supported in terms of tools, software, and IP core.

Table I The Objective of The Design

Minimize:	Overall order of the filter
Minimize:	Number of samples in group delay
Pass band ripple	≤ 0.3db
Stop band attenuation	≥104db
Transition-band ratio	≤ 1/0.9
Maximal deviation in group delay	≤ 1 sample

An equiripple FIR is a special class of FIR filter which is particularly effective in meeting such specifications. The maximal deviations (ripple error) from the ideal transfer function are minimized by an equiripple design protocol [6]. The equiripple algorithm applies to a number of FIR design instances. Below Fig. 4 shows the flow graph of the proposed technique for filter design.

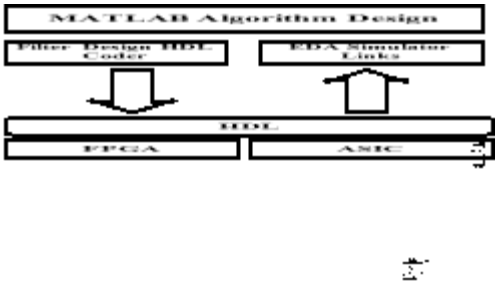

Fig. 4: Proposed methodology to design a filter.

III. ARCHITECTURE OF FIR FILTER

The transfer function of the FIR filter is

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \qquad (1)$$

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{k=0}^{N-1} h(k)z^{-k} \qquad (2)$$

Where N is the order of the filter.

h(k) is the coefficients of the filter.

FDA tool is used to design an equiripple FIR filter with the same objective, as stated above to an IIR filter which need an order of 162 for 50Hz signal. That is not acceptable in real time environment. FDA tool provides a pole zero plot, coefficient, group delay, phase response.

The Specifications in design of filter are [2] :

1) Pass band frequency (normalized) : 0.45
2) Stop band frequency (normalized) : 0.5
3) Pass band ripple (dB) : 0.1
4) Stop band attenuation (dB) : 104

The Xilinx logicore IP FIR Compiler core provides a common interface for users to import an coefficient from matlab. Fig. 5 shown is a quantized response of equiripple Filter. Matlab response is same as that of the magnitude plot in FIR IP core compiler.

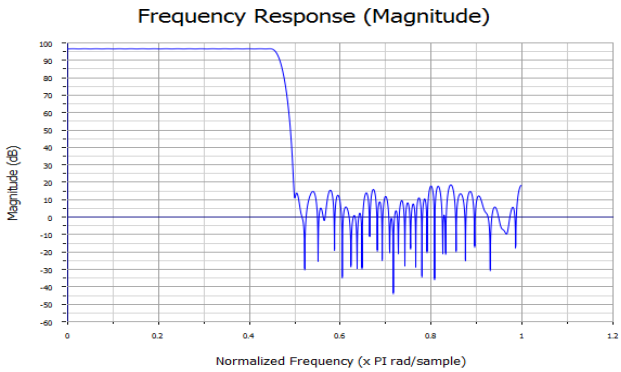

Fig. 5: Magnitude plot of design equiripple FIR filter.

The Transpose Multiply-Accumulate architecture is supported by the xtreme DSP Slice. This structure offers a low latency implementation, and also offer extra resource savings over the Systolic structure. It does not require an accumulator and can use fewer data memory resources, although it does not exploit coefficient symmetry [7].

The distributed arithmetic approach has the advantage of efficiency of mechanization. The basic operations required are a sequence of table lookups, additions, subtractions, and shifts of the input data sequence. All of these functions efficiently map to FPGAs. As the filter length is increased in a DA FIR filter, more logic resources are consumed, but throughput is maintained.

The Systolic Multiply Accumulate architecture provides an area-efficient and high speed performance filter implementations. The structure also extends to exploit coefficient symmetry offering further resource saving [7].

An FIR design module with systolic architecture is implemented in Verilog HDL with input data width as 16 bits and output data width as 40 depend on the hardware requirement data bus handle capacity this can be altered to meet an application.

The design Systolic multiply accumulate can able to use in application where the frequency requirement is up to 167.287MHz and have a moderate slice requirement in comparison with other two architectures. Hence it is the best selection for designing a filter.

Table II Synthesis Result of Design Equiripple Fir Filter

Architecture		Transpose Multiply Accumulate	Distributed Arithmetic	Systolic Multiply Accumulate
Number of slices		110	672	129
Number of slices flip flop		159	1289	203
Number of 4 input LUTs	Number used as logic	178	985	202
	Number used as shift registers	19	186	22
MULTS (MULT18X18SIO)		1	-	1
Delay(ns)		7.190	6.240	5.978
Maximum frequency (MHz)		138.089	160.253	167.287

IV. ELLIPTIC IIR FITER DESIGN

Bode plot of elliptic IIR digital filter design gives very sharp i.e. the transition width is small and phase response is non linear. But, through a process of compensation, some additional poles are added at an appropriate location and phase can be made linear. The transfer function of IIR filter is

$$y(n) = -\sum_{k=1}^{N} a_k y(n-k) + \sum_{k=0}^{M} b_k x(n-k) \qquad (3)$$

The filter design need Matlab to generate the coefficient and implement the various algorithms to analyze its performance. Further, this design is to be transferred to hardware description language (HDL) in order to obtain the hardware requirements (Power, area and speed) needed to analyzed and to implement the design on FPGA's.

The transfer function of IIR Filter with numerator coefficients b_i and denominator coefficients a_i is given in (4) and direct form II structure is shown in Fig 6.

$$H(Z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \qquad (4)$$

Magnitude response in dB

$$\alpha(\omega) = 20 \log |H(j\omega)| \qquad (5)$$ Group delay

$$T_d = -\frac{d}{d\omega}\phi(\omega) \qquad (6)$$

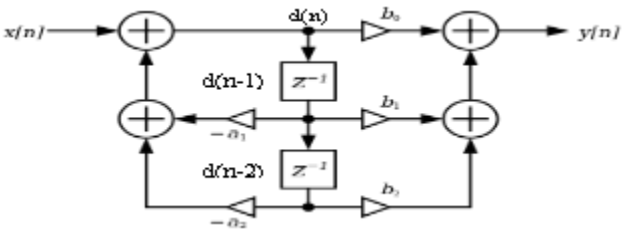

Fig. 6: Digital biquad filter direct form II structure.

The time domain expression for the IIR can be given as shown in (7) and (8). The denominator coefficients are expressed as -ve values in the fig. 6, but these can be expressed as positive values.

$$d(n) = x(n) + d(n-1).a_1 + d(n-2).a_2 \qquad (7)$$

$$y(n) = d(n).b_0 + d(n-1).b_1 + d(n-2).b_2 \qquad (8)$$

Same specifications is used here to design an IIR Filter the filter is designed for 50Hz cut off Frequency. An order with group delay compensated is 24. The 12 second order section is used to implement IIR filter. The use of direct form II realization structure reduces the necessary number of delay lines and adders as well. This is because the coefficient quantization is performed after dividing filter into sections and hence the change in location of poles is smaller. The proposed filter has an order of 24 with group delay compensation.

In order to get the best possible trade off between the signal to noise ratio at the output of the digital filter and the amount of hardware, accuracy needed has to be estimated. The structure used here is to minimize quantization errors is the 2nd order filter, also known as a biquad filter.

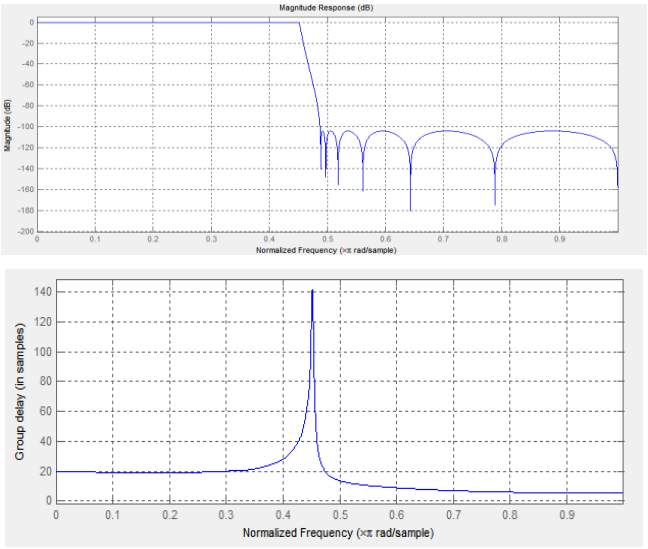

Fig. 7: Magnitude response and group delay response of LPF.

The canonical signed digit (CSD) representation is one of the existing signed digit (SD) representations with unique features which makes it useful in certain DSP applications focusing on low power, efficient-area and high-speed arithmetic [4]. As multiplier operations with additions of partial products produced by a canonical signed digit (CSD). These techniques minimize the number of addition operations required for constant multiplication by representing binary numbers with a minimum count of nonzero digits. The optimization you can achieve depends on the binary representation of the coefficients used.

V. RESULTS OBTAINED FROM AN ELLIPTIC IIR FILTER

Multiplier with pipeline registers give maximum frequency of operation and resource utilization is better in comparison to other architectures as shown in table III.

This filter design was implemented in Simulink and the output is analyzed on the spectrum scope as presented in Fig 8. The FFT length is 128, spectral average 2, and the buffer size is 128. Simulation of design filter performs well in Simulink environment and it is meeting the requirement and gives better performance.

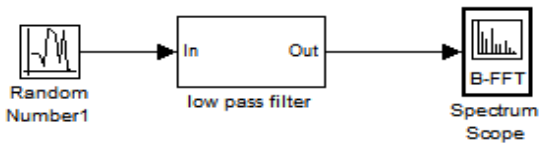

Fig. 8: Simulink model of the design elliptic IIR filter.

Table III Synthesis Result Of Iir Filter With Various Architecture

Architecture		Number slices	Number of slice flip flop	Latency	Maximum Frequency (MHz)
Multiplier	Without pipeline registers	1826	383	2	13.704
	With pipeline registers	1917	610	13	44.493
CSD	Without pipeline registers	2907	402	2	13.714
	With pipeline registers	2917	622	13	38.487
Factored -CSD	Without pipeline registers	2783	399	2	13.603
	With pipeline registers	2849	621	13	39.077

Considering the detailed operations of all two separate modules. i.e. clock divider and elliptic 50 Hz filter an top module has been written and the filter is constructed such that it is practically implementable on Spartan 3E kit to analyze its operation. Fig. 9 is a simulated response of the design filter to applied stimuli through testbench and observing its coefficient response. The below figure gives digital magnitude values in two's complemented form 15 bit equivalents.

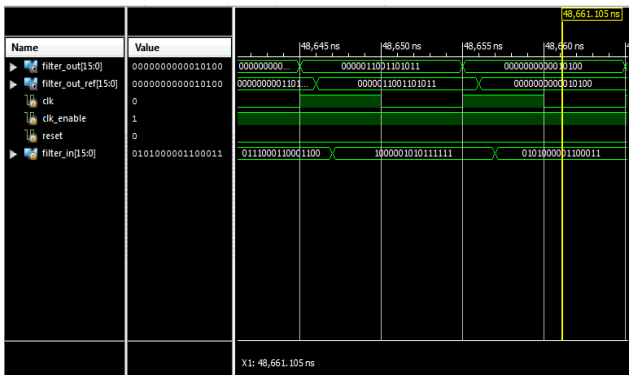

Fig. 9: Simulation result of elliptic IIR filter.

The IIR filter can be realized as two FIR filters connected back to back. The IIR filter consists of a forward FIR filter, also known as all-zero filter comprising of the numerator, and a feedback FIR filter for the denominator, or a coefficient for the poles.

Hence there is a need to design an efficient FIR filter to meet the desired specifications.

Fig. 10: Block diagram of equiripple FIR low pass filter

The Equiripple FIR filter was implemented on the Spartan 3E kit and lower 8 LSB bit's were observed by LED glow.

VI. CONCLUSION

The designed filters, FIR and IIR gives less delay and moderate resource utilization. Low hardware requirement with linear group delay are the conditions needed in power systems substations for real time application. The designed filters are used in application where the frequency requirement is up to 44.493 MHz for an elliptic IIR filter and 167.287MHz for an equiripple FIR filter applied in the area of power systems. Hence the proposed design of elliptic IIR is best suitable with lower hardware and also for real time application of the system in comparison with other techniques in the same flow. The target hardware was FPGA (Spartan-3E) for simulation.

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