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A STUDY ON COMPARISON ANALYSIS OF HIGH STEP-UP DC-DC CONVERTER WITH AN ACTIVE COUPLED INDUCTOR BY USING WITH AND WITHOUT PI CONTROLLER

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ABSTRACT

For Renewable energy applications a novel high step-up dc/dc converter is presented. It consists of a coupled inductor and two voltage multiplier cells, in order to obtain high step-up voltage gain. Two capacitors are charged during the switch-off period, using the energy stored in the coupled inductor which increases the voltage transfer gain. The energy stored in the leakage inductance is recycled with the use of a passive clamp circuit. Main power switch voltage stress is also reduced. The voltage conversion ratio, the effect of the leakage inductance and the parasitic parameters on the voltage gain is discussed. The voltage stress and current stress on the power devices are illustrated and the comparisons between the proposed converter and other converters are given. Finally, a prototype circuit rated 200-W output power is implemented in the laboratory, simulation results shows satisfactory agreement with the theoretical analysis.

Keywords: Active Coupled-Inductor, Network (ACLN), High Step-Up Voltage Gain DC–DC Converter, Low Voltage Stress.

I. INTRODUCTION

Generally recognized, the distributed PV generation systems based on the renewable energy sources have been a most promising candidate for the exhaustion of fossil fuel [1]–[3]. However, the PV source is the low-voltage source which cannot provide enough dc voltage for generating ac line voltage. Although the PV cells can connect in series to obtain the sufficient dc voltage, it is difficult to avoid the shadow effect and to obtain a constant dc voltage [4], [5]. Thus, the high step-updc–dc converters with a large conversion ratio, high efficiency, and small volume are dispensable as the dc link between the PV source and inverter [6].In general, the boost converter is widely used in such applications. Theoretically, the boost converter can provide a high step-up voltage gain with an extremely high duty cycle. In practice, the voltage conversion ratio is limited below four or five by parasitic parameters effect dramatically

[7]. Consequently, if the voltage conversion ratio is desired to be over five, the high step-up converter topologies are needed [8]–[19].The isolated converter topologies like the flyback converter can achieve a high

step-up voltage gain by adjusting the turns ratio of the transformer. However, the leakage inductor can cause the high voltage spike, and

Therefore, a high-voltage rated switch is needed [8]. Although the passive-clamped circuits and active clamped circuits can be employed, the efficiency is degraded and the cost is increased [9].

The problems in the conventional boost converter which works under the high step-up condition can be solved by introducing a coupled inductor [14], [15]. The voltage gain is extended and the voltage stress on the switch is reduced. Moreover, the cores can be integrated and the volume is reduced. However, the leakage inductance may cause the same problems as in isolated converters. Compared to the boost converter, an active network converter (ANC) has been proposed in [16], where the voltage stresses and current stresses of the switches are much lower, and the voltage conversion ratio is higher. However, there exists the switch voltage resonance due to the switches parameters inconsistency. Switched inductor ANC is proposed to extend the voltage gain, but the voltage conversion gain can only be controlled by duty cycle and the overall system volume is larger [17]. The ANC with the switched inductor and switched capacitor is proposed in [18], but the system volume is large and part count is increased greatly under the high voltage conversion gain. The ANC with coupled inductors is further proposed in [19], and the voltage gain is increased by adjusting turns ratio of the coupled inductor and the duty cycle, but the part count is still high. This letter proposes a novel high efficiency high step-up voltage gain converter which combines an active coupled-inductor network (ACLN) and a traditional boost converter with a passive Clamping circuit, called the ACLN converter (ACLNC).

II. PROPOSED HIGH STEP-UP CONVERTER

The proposed converter has the following advantages: high voltage conversion gain, small volume, low voltage stresses on switches, low diodes count, and low conduction losses on switches. The basic operating principle is first illustrated in detail, then the stresses expressions are deduced, and finally, some experimental results are provided to verify the effectiveness of the proposed converter. The proposed converter contains an ACLN which is shown in Fig. 1. The ACLN consists of two coupled inductors (L11 and L12, L21 and L22) which have the same inductance value and two Same switches (S1 and S2) which share the same operation signal.

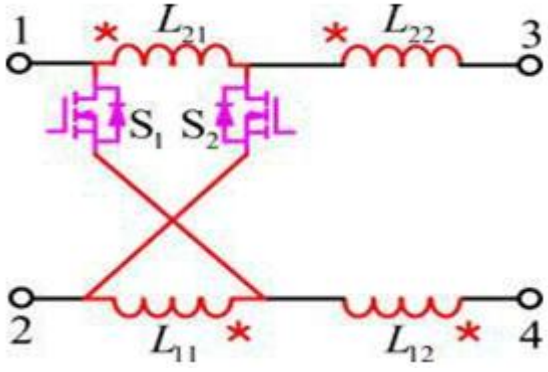

Fig.1. The active coupled-inductor network (ACLN).

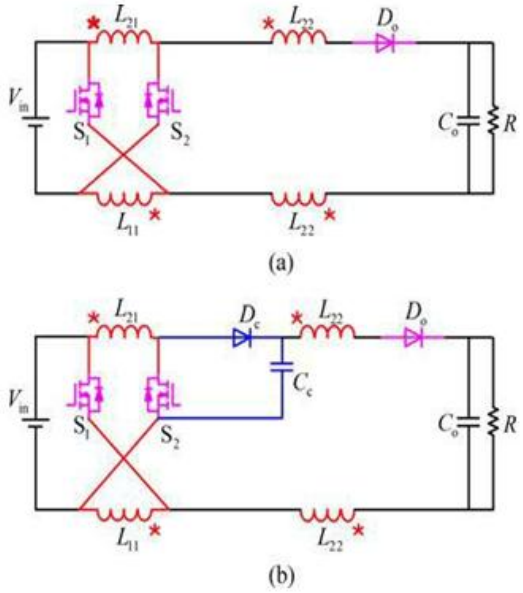

Fig.2. Proposed high step-up ACLN dc–dc boost converter. (a) ACLNC. (b) ACLNC with a passive lossless clamped circuit.

ACLN with the traditional boost converter, the ACLN dc–dc boost converter (ACLNC) is obtained, as shown in Fig. 2(a), in which the output voltage is greatly enhanced. The proposed high step-up converter is constructed by two coupled inductors made up of four windings L11, L12 ,L21, and L22, two switches S1 and S2 , one output diode Do , and one output capacitor Co. The leakage inductance is inevitable in the proposed ACLNC, which results in high voltage spikes, large switching losses, and severe EMI problems. In general, the dissipated RCD circuit can be used for absorbing the leakage inductance, but the losses Induced by the RCD circuit are significant and the efficiency is degraded. Therefore, passive lossless clamped circuits are applied here to recycle the leakage energy and to suppress the voltage spikes as shown in Fig. 2(b) [6].

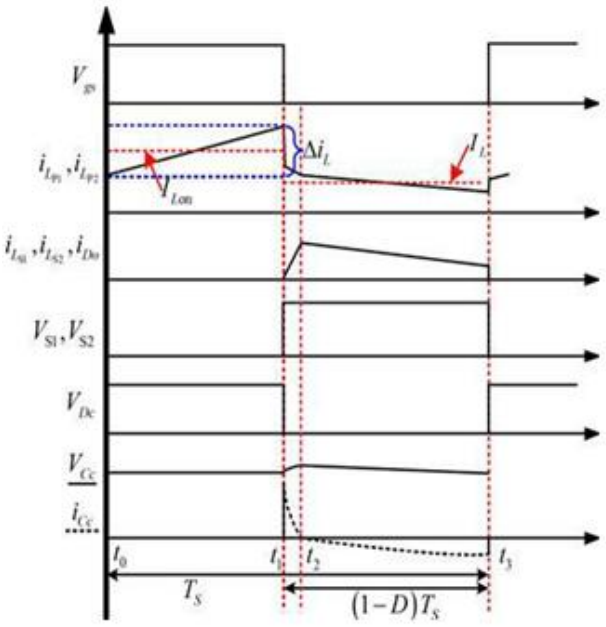

Fig.3. Some typical waveforms of the proposed ACLNC

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III. BASIC OPERATING PRINCIPLE

Fig3 briefly illustrates the key waveforms of the proposed ACLNC. Only the operating principle in continuous- conduction mode (CCM) is discussed in this letter. The transient states in operating principle will not be discussed here because the parasitic resistance and the parasitic capacitance of the two active switches and diodes are neglected. Fig. 4(b)–(d) shows the equivalent circuits of the proposed ACLNC under the following assumptions:

1) The capacitors Cc and Co are large enough so that the voltages on them are considered to be constant. 2) The switches and diodes are ideal. In order to clearly show the current flows, the ideal switches take the place of MOSFETs in ON state or OFF state, as shown in Fig. 4(a). 3) The equivalent circuit model of the coupled inductor includes two ideal coupled inductors LPiand LSiand two leakage inductors Lki(i = 1, 2). 4) To make the following derivation simple, define K as LP i/ (LP i +Lki) and the turns ratio of LP1 to LS1 and LP2 to LS2 is 1 :N (N >1). LP1, LP2 and LS1, LS2 share the same inductance, respectively.

A. CCM Operation

The three steady operating modes are described as follows. Mode I [t0 ,t1]: During this time interval, the switches S1 and S2 are turned ON. Diodes Dc and Do are reverse biased.

The current-flow path is shown in Fig. 4. The primary sides of both coupled inductors are in parallel charged. The currents inductor iLP 1 and iLP2 are increased linearly. Output capacitor Co provides its energy to the load R. When the switches S1 and S2 are turned OFF at t1 , this operating mode ends. Thus, according to the KVL, the voltage equation across coupled inductors is expressed as follows:

$$V_L^I = 2(NK+1)V_{\text{in}}. \quad (1)$$

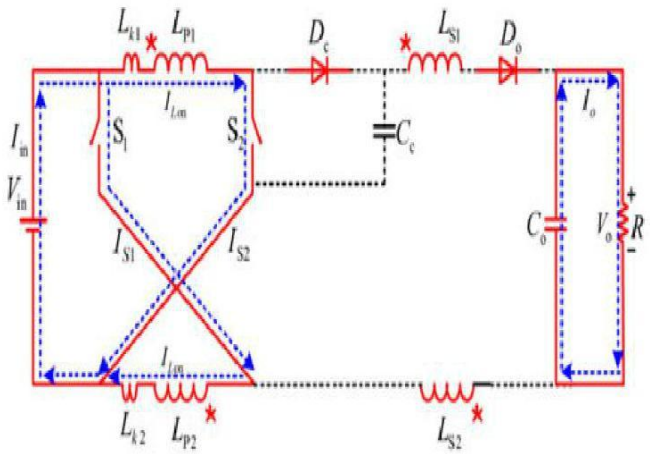

Fig.4.

Mode II [t1, t2]: During this time interval, the switches S1 and S2 are turned OFF. Diodes Dc and Do are forward biased. The leakage energy flows into the clamped capacitor Cc. Meanwhile, the dc source Vin and the energies stored in the coupled inductors are transferred to output capacitor Co and the load R. This operating mode is ended when the charging current of clamped capacitor iCcis equal to zero, as shown in Fig. 5. The voltage across both coupled inductors can be expressed as

$$V_L^{II} = V_{in} - V_o. \quad (2)$$

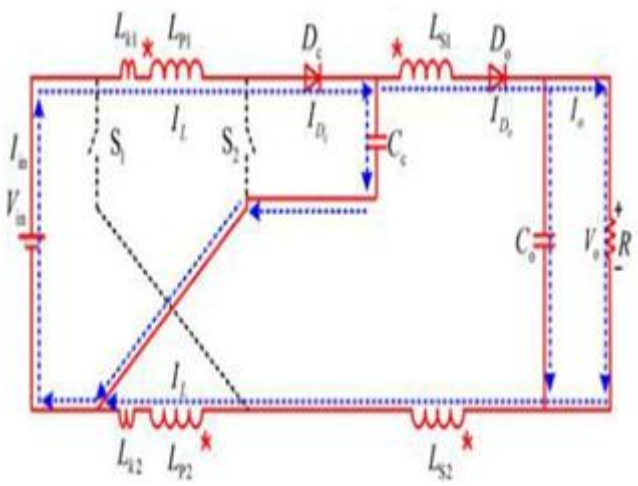

Fig.5.

Mode III [t2 ,t3]: During this time interval, the switches S1 and S2 remain OFF. Diodes Dc and Do are still forward biased. The current-flow path is shown in Fig.6. The clamped capacitor Cc is discharging. Concurrently, the dc source Vin and the energies stored in the coupled inductors are transferred to output capacitor Co and the load R. This operating mode is ended when the switches S1 and S2 are turned ON at t3. The voltage across both coupled inductors can be written as.

$$V_L^{III} = V_{in} - V_o. \quad (3)$$

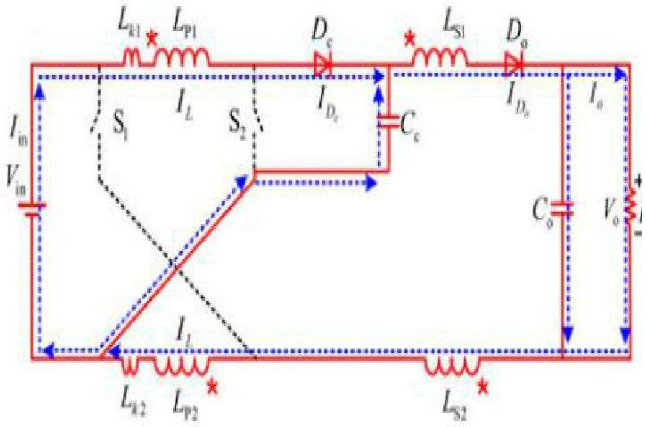

Fig.6. Equivalent circuits of the proposed ACLNC

IV. CIRCUIT PERFORMANCE ANALYSIS

A. Steady-State Analysis

By applying the volt–second balance principle on coupled inductors, the following equation is formed:

$$\int_{t_0}^{t_1} V_L^I dt + \int_{t_1}^{t_2} V_L^{II} dt + \int_{t_2}^{t_3} V_L^{III} dt = 0. \quad (4)$$

Substituting (1)–(3) into (4) and collecting terms, the voltage gain is obtained as

$$M_{CCM} = (D(2NK + 1) + 1)/(1 - D). \quad (5)$$

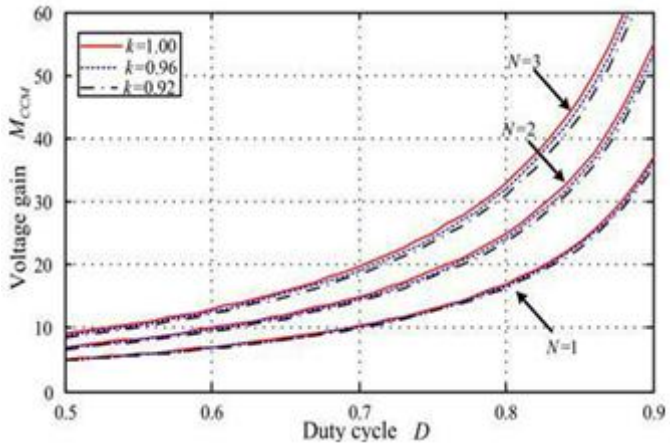

Fig. 7.Effect of leakage inductance and turns ratio on voltage gain

By employing the clamp circuits, the voltage strikes caused by the leakage inductance are suppressed and the energy stored in the leakage inductance is recycled to the load. Especially, the reverse-recovery problem of the diodes Do is solved. However, the leakage inductance causes the duty ratio losses. The schematic of the voltage gain versus the duty ratio under various leakage inductanceLk1 and various turns ratio of the coupled inductors is shown in Fig.

As the turns ratio increases, the voltage gain of this converter increases. On the contrary, as the leakage inductance increases, the voltage gain of this converter decreases. In order to further clearly show the effect of the leakage inductance, Table I shows the effect of the leakage inductance and the turns ratio on the voltage conversion gain when the converter operate under D=0.6. Therefore, some Consideration should be made when the leakage inductance is big during the design. When leakage inductance is zero, the ideal voltage gain can be written as

$$M_{CCM} = (D\,(2N+1) + 1)\,/(1 - D). \quad (6)$$ **B.**

Voltage Stresses and Current Stresses on Power Devices

The voltage ripples on the capacitors and the leakage inductances are ignored to simplify the voltage stresses analysis on the components of the proposed converter. The voltage stresses of the main switch S1, S2 and clamped capacitor Cc are given by

$$V_{S1} = V_{S2} = V_{C_c} = V_{in}/(1 - D). \quad (7)$$

The voltage stresses on diodes Do and Dc related to the turns ratio and the input voltage can be derived as

$$V_{D_o} = V_{in}\,(2N + 1)\,/(1 - D)$$
$$V_{D_c} = V_{in}/(1 - D). \quad (8)$$

The on-state average currents of the output diode Do and clamped diode Dc are calculated as

$$I_{D_o} = I_{D_c} = I_o/(1 - D). \quad (9)$$

The root-mean-square (RMS) currents through the switches can be obtained by assuming the inductor current ripples of primary sides of coupled inductors as iL= KL

ILon,

$$I_{S1-RMS} = I_{S2-RMS} = \frac{(1+N)\sqrt{D}}{1-D} \cdot \frac{P_o}{V_o}\sqrt{\frac{K_L^2}{12}+1} \quad \textbf{(10)}$$

C. Comparison with Other Converters

Due to the dual-switch structure, the current ripple is minimized to reduce the conduction loss, the passive component size is reduced, and the power level is increased. In order to clearly demonstrate the circuit advantages of the proposed converter, a detailed comparison is made among the conventional boost converters, boost converter with switching coupled-inductor [Boost-SCL] in [20], ultra large gain step-up switched-capacitor dc–dc converter with coupled inductor [USC-CL] in [21], a coupled inductor SEPIC converter [CL-SEPIC] in [22], passive clamp-mode coupled-inductor boost converters with coupled inductor [CM-Boost-CL] in [6], and the proposed ACLNC are highlighted in Table II.

TABLE II: Performance Comparison Among Different Converters

Topology	Boost	Boost-SCL	USC-CL	CL-SEPIC	CM-Boost-CL	ACLNC
Active switches	1	1	1	1	1	2
Diodes	1	2	4	2	2	2
Magnetic cores	1	1	1	2	1	1
Voltage gain	$\frac{1}{1-D}$	$\frac{1+N\,D}{1-D}$	$\frac{C3}{1-D}$	$\frac{(1+N)D}{1-D}$	$\frac{N\,D+1}{1-D}$	$\frac{C6}{1-D}$
Voltage stress of active switch	$\frac{V_{in}}{1-D}$	$V_{in}\frac{1+N\,D}{1-D}$	$\frac{V_{in}}{1-D}$	$V_{in}\frac{1+N\,D}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$
Current stress of active switch	$\frac{I_O}{1-D}$	$\frac{I_O(N+1)}{1-D}$	$\frac{I_O N(D+1)}{D(1-D)}$	$\frac{I_O(D+N)}{1-D}$	$\frac{I_O(N+1)}{1-D}$	$\frac{I_O(N+1)}{1-D}$
Voltage stress of output diode	$\frac{V_{in}}{1-D}$	$V_{in}\frac{1+N\,D}{1-D}$	$\frac{N\,V_{in}}{1-D}$	$V_{in}\frac{1+N\,D}{1-D}$	$\frac{N\,V_{in}}{1-D}$	$\frac{(1+2N)V_{in}}{1-D}$
Cost	small	medium	medium	medium	small	medium
Voltage gain with parasitic resistance	$\frac{A1}{B1}$	$\frac{A2}{B2}$	$\frac{A3}{B3}$	$\frac{A4}{B4}$	$\frac{A5}{B5}$	$\frac{A6}{B6}$
Efficiency with parasitic resistance	$\frac{A1(1-D)}{B1}$	$\frac{A2(1-D)}{B2(1+N\,D)}$	$\frac{A3(1-D)}{B3C3}$	$\frac{A4(1-D)}{B4C4}$	$\frac{A5(1-D)}{B5(N\,D+1)}$	$\frac{A6(1-D)}{B6C6}$

$$A1 = 1 - V_D\,(1-D)\,/V_{in}$$
$$B1 = 1 - D\,(r_L + D r_{DS} + (1-D) r_D)\,/\,((1-D)R)$$
$$A2 = ND + 1 - V_D\,(1-D)\,/V_{in}$$
$$B2 = 1 - D + \frac{(N+1)r_L + r_D}{R} + \frac{D(N+1)^2(r_L + r_{DS})}{(1-D)R}$$
$$A3 = 1 + N\,(D+1) - 4V_D\ \ (1-D)\,/V_{in}$$
$$B3 = 1 - D + N\,(r_L + r_D)\,/2R + (N r_L + r_D)\,(1+D)\,/DR + N\left(1 + D + D^2\right)(r_L + r_{DS})\,/D^2\,(1-D)\,R$$
$$C3 = 1 + N\,(D+1)\,,\ A4 = D\,(N+1) - V_D(1-D)/V_{in}$$
$$B4 = 1 - D + r_{DS} D(N+1)^2/(1-D)R + (N_L + r_D)/R + \left(1 - 2D + 2D^2 + DN^2 - 2D^3 - 2D^2N^2\right) r_L/(1-D)\,R,$$

$$
\begin{aligned}
C4 &= D(N+1) \\
A5 &= ND+1-2V_{\mathrm{D}}(1-D)/V_{\mathrm{in}} \\
B5 &= 1-D+\frac{(2r_{\mathrm{D}}+r_L(N+1))}{R} \\
&\quad +\frac{(r_L+r_{\mathrm{DS}})D(N+1)^2}{(1-D)R} \\
A6 &= D(2N+1)+1-2V_{\mathrm{D}}(1-D)/V_{\mathrm{in}} \\
C6 &= (2N+1)D+1 \\
B6 &= 1-D+\frac{2(r_L+Nr_L+r_d)}{R} \\
&\quad +\frac{2D(N+1)^2(r_L+r_{\mathrm{DS}})}{R(1-D)}.
\end{aligned}
\tag{11}
$$

Some specific variable symbols of all parasitic components are assumed as follows: VD is the forward voltage drop of diodes; rLis the ESR of inductors; rDS is the on-state resistance of the switch; rD represents the forward resistance of diode; and R represents the load. According to the previous work [23], [24], the theoretical dc gain and efficiency influenced by the parasitic parameters and duty cycle are also obtained in Table II. Although the different voltage stresses and current stresses of the power switches make different models of power switch available in different converters, here we assume that all the parasitic parameters are same. In order to show how different output power influences the efficiency, some parameters are assumed as follows: VD = 1 V, rL=0.05 Ω, rDS=0.085 Ω, rD=0.02 Ω, Vin = 20V, Vo=200V, N =2. Fig. 8 shows the calculated efficiency under different load. One can see that the efficiency of the boost converter and the CL-SEPIC converter is higher than the proposed converter in the case of light load, only the efficiency of the CL-SEPIC converter is higher than the proposed converter in the case of overloading. So, although the numbers of components in the proposed converter compared with the boost converter are increased, the efficiency cannot be degraded.

On the contrary, because of decreasing voltage stress and current stress, it is easy to achieve decent efficiency in high step-up applications. Fig. 9 calculates the voltage gain under different duty cycle. When the duty cycle is lower than about 0.65, only the voltage gain of USC-CL is higher than the gain of the proposed converter. When the duty cycle is lower than about 0.55, the parasitic parameters have little impact on the voltage gain of the converters, except USC-CL converter. As the duty cycle increases, the ideal voltage gain of the proposed converter is beyond the ideal voltage gain of the USC-CL converter. Meanwhile, parasitic parameters make the practical voltage gain lower than the ideal voltage gain in all converters. But, the practical voltage gain of the proposed converter is still higher than the practical voltage gain of other converters, except USC-CL converter. Compared with the boost converter, both the ideal voltage gain and the practical voltage gain of the ACLNC are higher. Also, the voltage stresses and the current stresses of the switches in the ACLNC are dramatically reduced. Although the numbers of part in the ACLNC are more than those of the boost converter.

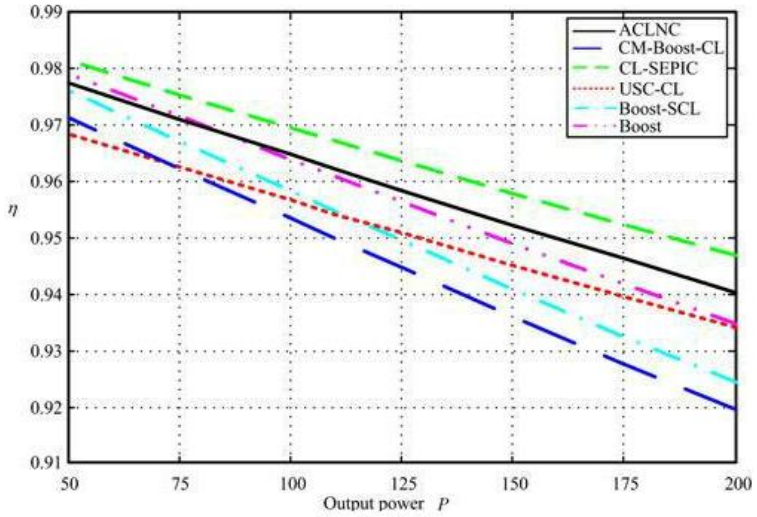

Fig.8. Efficiency curves of different converters hich is influenced by parasitic parameters and duty cycle under different output power

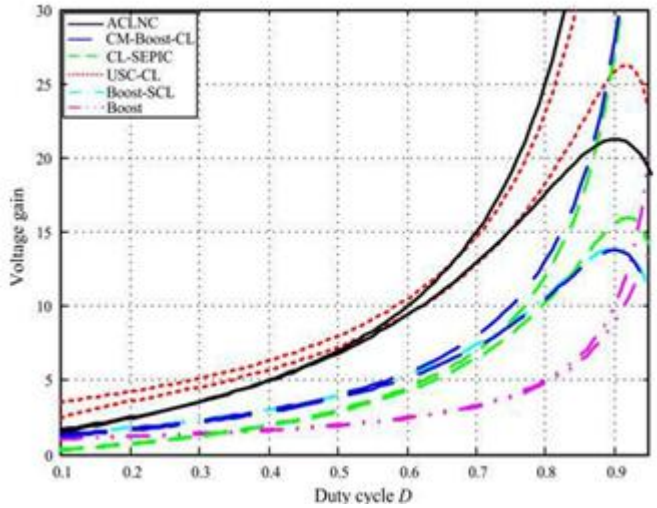

Fig.9. Comparison of the voltage gain among different converters (solid line: ideal voltage gain, dashed line: voltage gain influenced by parasitic parameters).

TABLE III: System Specification of the Proposed Converter

System parameters	Specifications
Input voltage V_{in}	20 V
Output voltage V_o	200 V
Rated power P_o	200 W
Switching frequency f_s	50 kHz

TABLE IV: System Specification of the Proposed Converter

Components	Specifications
Switches S_1 , S_2	IRFP250
Diodes D_o , D_c	VS-EPU6006-N3
Output capacitor C_o	470 μF/450 V
Clamped capacitor C_c	22 μF/100 V
Coupled inductors	Core-NPS306060
	$N_P : N_S = 1 : 2$
	$L_{P1} = 232\,\mu H, L_{S1} = 942\,\mu H$
	$L_{P2} = 212\,\mu H, L_{S2} = 922\,\mu H$

The efficiency of the ACLNC is superior to the boost converter gain of USC-CL is higher than the gain of the proposed converter. When the duty cycle is lower than about 0.55, the parasitic parameters have little impact on the voltage gain of the converters, except USC-CL converter. As the duty cycle increases, the ideal voltage gain of the proposed converter is beyond the ideal voltage gain of the USC-CL converter. Meanwhile, parasitic parameters make the practical voltage gain lower than the ideal voltage gain in all converters. But, the practical voltage gain of the proposed converter is still higher than the practical voltage gain of other converters, except USC-CL converter. Compared with the boost converter, both the ideal voltage gain and the practical voltage gain of the ACLNC are higher. Also, the voltage stresses and the current stresses of the switches in the ACLNC are dramatically reduced. Although the numbers of part in the ACLNC are more than those of the boost converter, Compared with the Boost-SCL, both the ideal voltage gain and the practical voltage gain of the ACLNC are higher. The voltage stresses of the switches in the ACLNC are reduced, the low on-resistance switch can be used. Meanwhile, the current stresses of the main switches are also reduced.

V. SIMULATION RESULT

Below fig.10 shows the overall simulation circuit of without PI Controller. Input voltage is 20V and output voltage is 200V as shown in Fig.11.

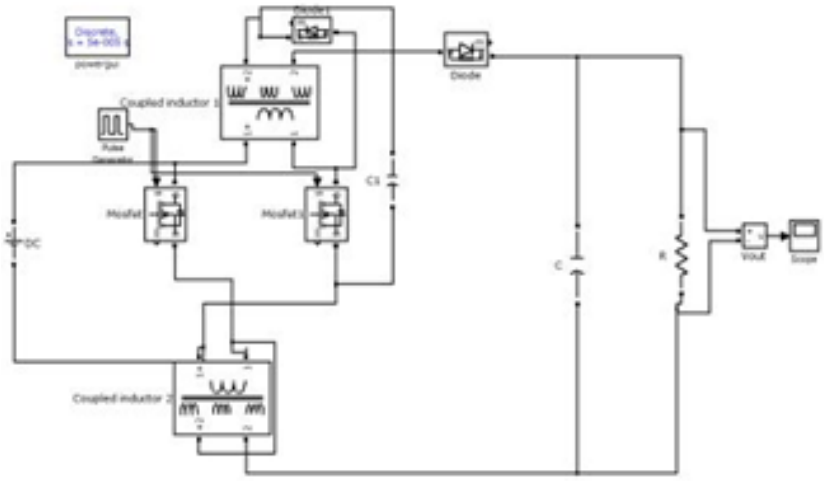

Fig.10.Existing system block diagram.

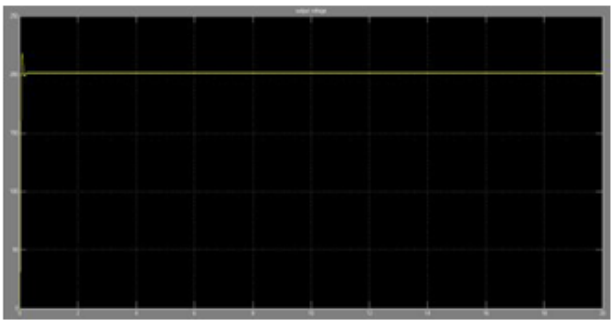

Fig.11. the output voltage wave form (200V).

The pulse generation of the circuit shown in below Fig.12.

Fig.12.The pulse generation of the circuit.

The black diagram of extension system with PI Controller shown in below Fig.13.

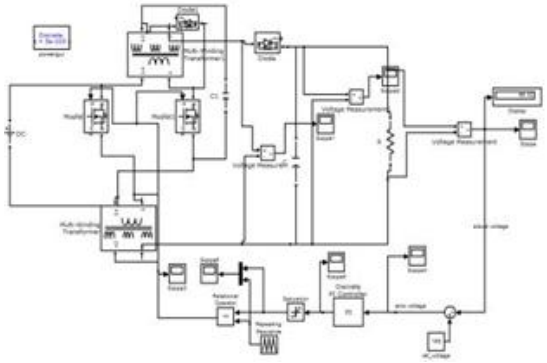

Fig.13. Extension system block diagram.

Pulse Width Modulation wave form shown in below Fig.14.

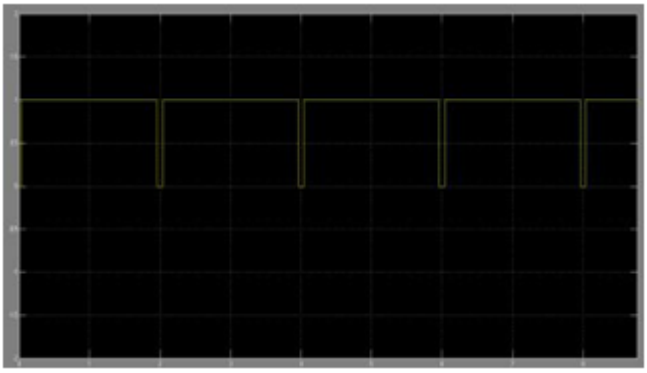

Fig.14.Pulse Width Modulation waveform.

The input voltage shown in given below Fig.14.

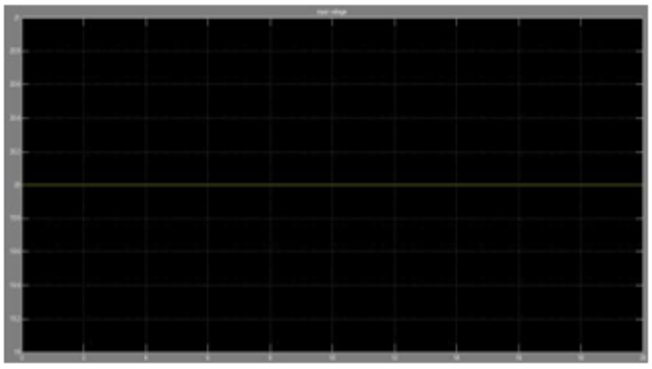

Fig.15.extension system input voltage waveform.

The output voltages 100v,150v and 200v wave forms are shown below Figs.15 to 18.

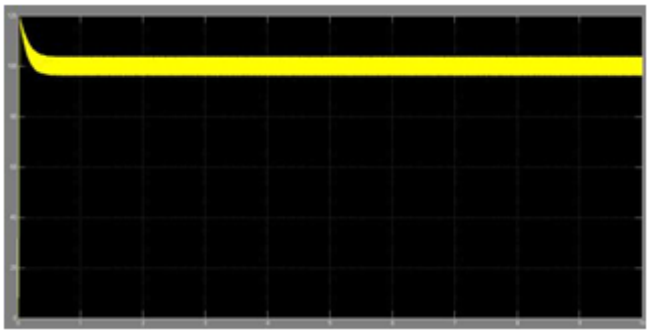

Fig.16.extension system output voltage (100v) waveform

Fig.17.extension system output voltage(150v) waveform.

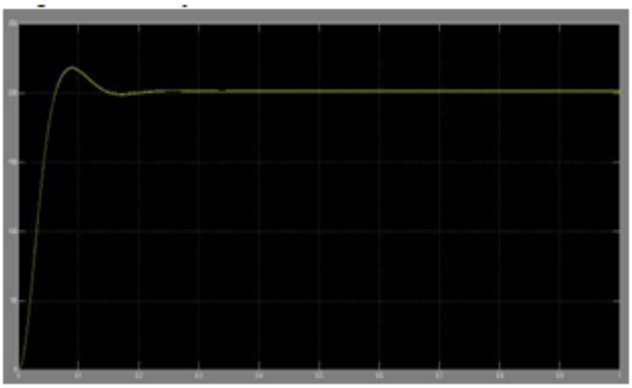

Fig.18 extension system output voltage (200v) wave form.

VI. CONCLUSION

In this paper few conclusions are made. By using PI controller we can get dynamic response and fixed switching frequency. We also can reduce hormonics.instead of using PI controllers we also can use other types of controllers.

ACLNC topology with high voltage ratio is proposed and the steady-state analysis is given. A passive lossless clamped circuit is introduced to suppress the voltage spike across the switches. Compared to the traditional high stepup dc/dc converter, it has the following advantages: high voltage gain can be achieved with the reduced magnetic size lower part count contributes not only to the lower cost but also to higher power conversion efficiency; low voltage power switches can be selected, which can help to reduce the on-state resistance of the switch and the loss. But in closed loop system output voltage need to set. Depends on set voltage system will give the output voltage. Simulations results are taken for varies voltages like 100V, 150V, 200V and are studied. PI controller is used for design the closed loop system.

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