International Journal of Advanced Technology in Engineering and Science
Vol. No.5, Issue No. 07, July 2017
www.ijates.com
ijates
ISSN 2348 - 7550

TRANSISTOR RESIZING APPROACH FOR FULL ADDER CELLS TO REDUCE THE LEAKAGE POWER

M. Chandra Sekhar[1] , K.Soumya[2]

Assistant Professor[1,] Assistant Professor[2]

[1,2]Dhruva Institute of Engineering & Technology , Near Ramoji Film City

Yadadri District, Telangana, (India)

ABSTRACT

Power dissipation has become a major issue it has made the way to consider the performance and area so that low power is achieved. Low power is the major requirement for portable multimedia devices employing various signal processing algorithms and architectures. Any computational circuit is incomplete without the utilization of an Adder. Addition is one of the primary operations in arithmetic circuits. We presented a new transistor resizing approach for 1bit full adder cells to regulate the optimal sleep transistor size which reduce the leakage power. In this paper, we propose approximate four bit full adder to reduce the leakage power. These four bit adders are implemented using 1 bit adder as reference. We have performed simulations using micro wind in different nano meter technologies with standard CMOS technology.

Keywords: Sleep transistor,4-Bit Full Adder Cell, Conventional Mirror Adder (CMA), Microwind and DSCH Tools.

I. INTRODUCTION

In current day's electronics industry, one of the main challenges faced is to attain low power designs for the several applications. As power dissipation has become a major issue it has made the way to consider the performance and area so that low power is achieved. The trend for considering low power designs began with a remarkable growth in the areas of personal computing like portable desktops, multimedia devices etc., that particularly aim in high speed computations and complex functionality with reduced power consumption.

The approximate computing has specification for selecting the hardware for DSP blocks. DIGITAL SIGNAL Processing (DSP) blocks form the backbone of various portable multimedia applications. Most of these DSP blocks implement image and video processing algorithms, where the ultimate output is either an image or a video for human consumption. Human beings have less perceptual abilities when interpreting an image or a video. This allows the outputs of these algorithms to be numerically approximate rather than accurate.

Adders are heart of computational and many complex arithmetic circuits are based on the addition. The main use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In current day technologies, several variants of different logic styles have been proposed to implement 1-bit full adder cells. These full adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30xincrease in gate leakage. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity.

The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further peak of ground bounce noise is possible with proposed novel technique with improved staggered phase damping technique.

II. CONVENTIONAL MIRROR ADDER

Power dissipation has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power dissipation. Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous when we implement by the pass transistor logic. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability.

The following figure shows the conventional CMOS 28 transistor adder. This is considered as a Base case throughout this paper. All comparisons are done with Base case. The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs.

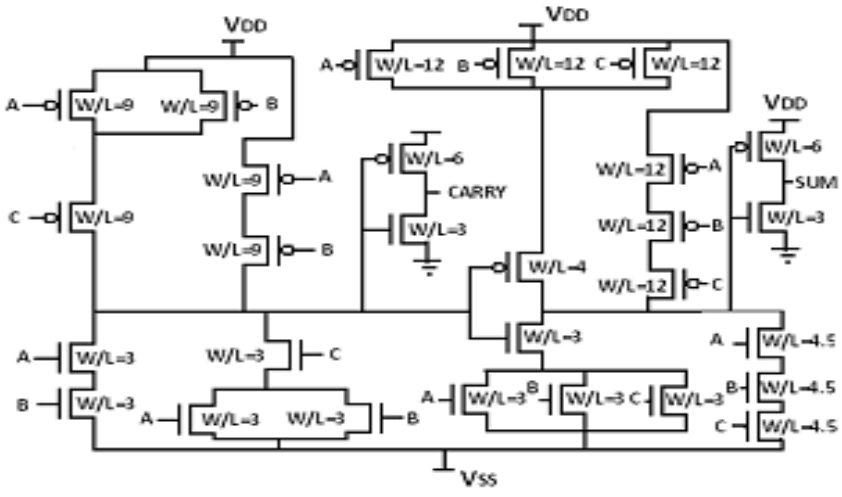

Fig:1 Conventional Mirror Adder

Since this implementation is not based on complementary CMOS logic, it provides a good opportunity to design an approximate version with removal of selected transistors.

III. SLEEP TRANSISTOR

To reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Modified sizing are shown in following figures respectively.

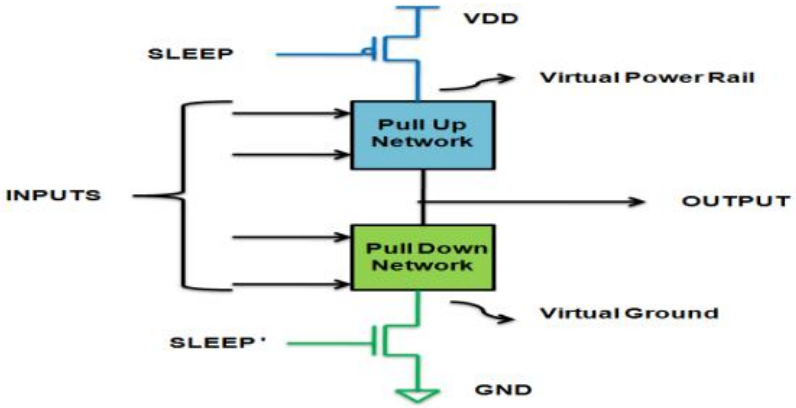

Fig 2: Sleep transistor design

The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and gives W/L ratio of 1.2. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which are 3.1 times that of NMOS in fig2. The sizing of each block is based on the following assumption each block has been treated as an equivalent inverter. The same inverter ratio is maintained on each block. These sizing will reduce the standby leakage current greatly because sub threshold current is directly proportional to the Width/Length ratio of transistor. On the other hand, these reduced sizes will reduce the area occupied by the circuit. This will reduce the silicon chip area and obviously there will be a reduction in the cost. Modified adder circuit i.e. fig 4.3 shown, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an equivalent inverter. The goal of this design is to reduce the standby leakage power.

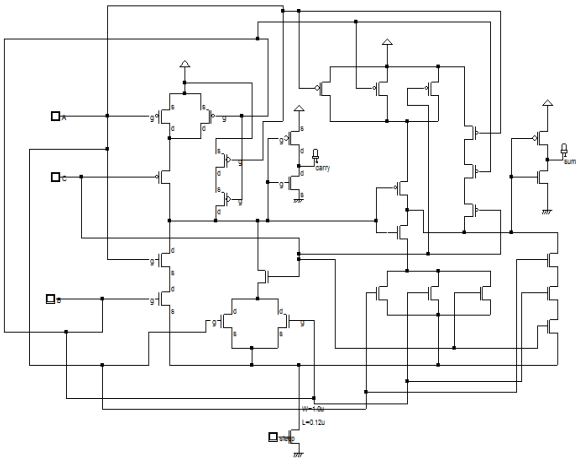

Fig3 Conventional Mirror Adder with sleep transistor

IV. APPROXIMATE FULL ADDER CELLS

In this section, we discuss different methodologies for designing approximate adders. Since the MA is one of the widely used economical implementations of an FA, we use it as our basis forproposing different approximations of an FA cell with sleep transistor.

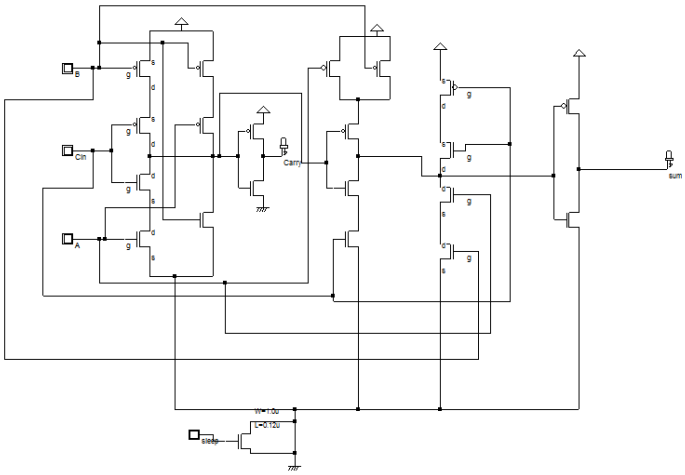

Fig 3: approximation1with sleep transistor

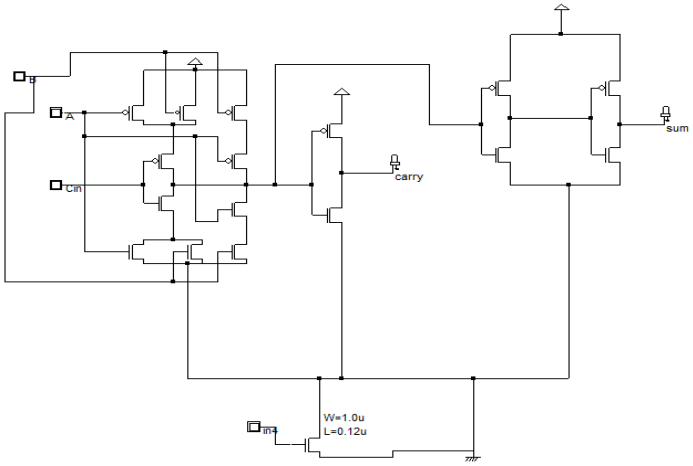

Fig 4: approximation 2 with sleep transistor

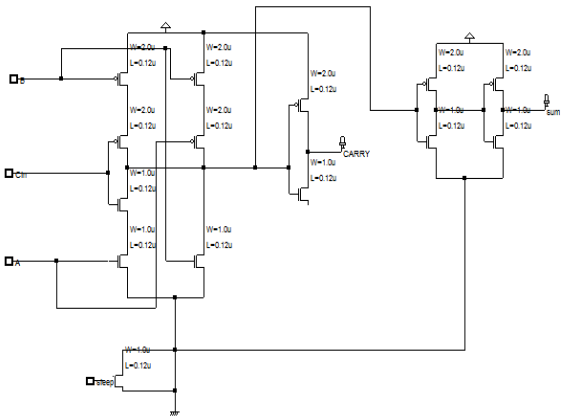

Fig 5: approximation 3 with sleep transistor

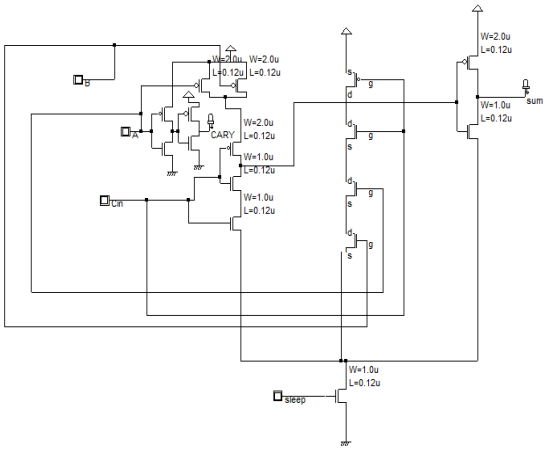

Fig 6: approximation 4 with sleep transistor

A. Approximation Strategies for the MA

In this section, we explain step-by-step procedures for various approximate MA cells with fewertransistors. Removal of some series connected transistors will facilitate faster charging/discharging of node capacitances.

Approximation 1:

To get an approximate MA with fewer transistors, we start to remove transistors from the conventional schematic one by one. However, we cannot do this in an arbitrary fashion. We have to make sure that any input combination of A,B and C_{in} won't result in short circuits or open circuits in the simplified schematic. Other important is that the resulting simplification should introduce minimal errors in the Full Adder truth table.

A goods election of transistors to be removed (ensuring no open or short circuits) results in a schematic shown in Fig. 3, which we call approximation 1. Clearly, this schematic has eight fewer transistors compared to the conventional MA schematic. In this case, there is one error in C_{out} and two errors in Sum, as shown in Table I.

In this case, there is one error in C_{out} and two errors in Sum, as shown in Table I. A tick mark denotes a match with the corresponding accurate output and a cross denotes an error.

Approximation 2:

The truth table of an FA shows that Sum= Cout1for six out of eight cases, except for the input combinations A = 0,B = 0,Cin= 0 and A = 1,B = 1,Cin= 1.Now, in the conventional MA, Cout is computed in the first stage. Thus, an easy way to get a simplified schematic is to set Sum= Cout.

In this approximation2, Sum has only two errors, while Cout is correct for all cases, as shown in Table I.

Approximation 3:

Next simplification can be obtainedby combining both approximations 1 and 2. Here one error in Coutand three errors in Sum, as shown inTable I. The corresponding simplified schematic is shown inFig. 10.

Approximation 4:

In this approximation 4 it introduces two errors in Cout and three errors in Sum, as shown in Table I. The corresponding simplified schematic is shown in Fig. 11.In all these approximations, Cout is calculated by using an inverter with Cout as input.

These all approximations are using sleep transistor corresponding figures are shown above. Therefore a new transistor resizing approach for 1-bit full adder cells to determine the optimal sleep transistor size which reduces the leakage power.

V. PROPOSED 4 BIT FULL ADDER DESIGN

The four bit Conventional mirror adder and approximation full adder cells are designed with help of 1 bit adder cells. The main important is that the resulting simplification should introduce minimal errors in the Full Adder truth table. The all four bit[4] approximations are satisfying the resulting minimal errors in the table I.

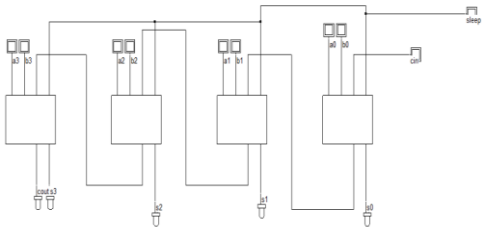

Fig 7: four bit Conventional mirror adder

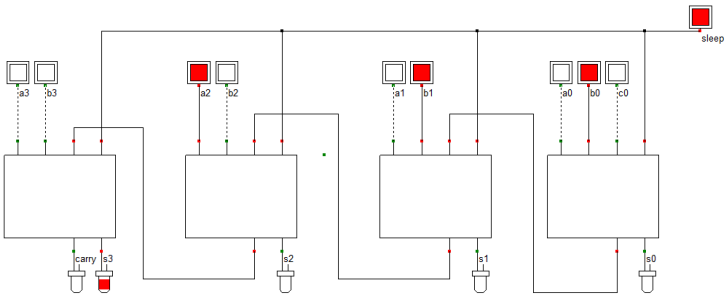

Fig 8:four bit approximation 1 adder

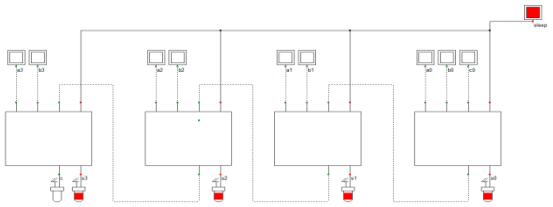

Fig 9: four bit approximation 2 adder

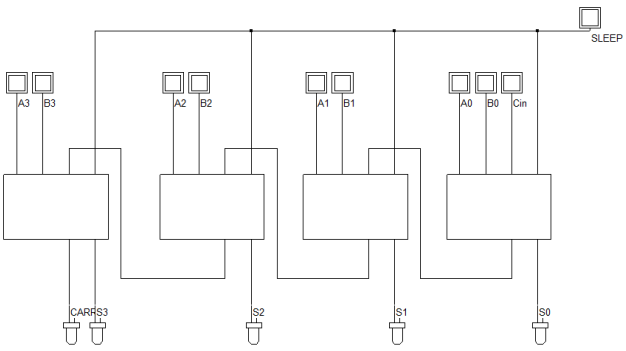

Fig 10:four bit approximation 3 adder

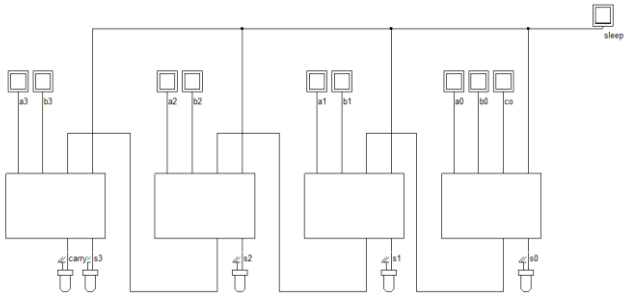

Fig 11:four bit approximation 4 adder

TABLE I

TRUTH TABLE FOR CONVENTIONAL FA AND APPROXIMATIONS 1–4

Inputs			Accurate Outputs		Approximate Outputs							
A	B	C_{in}	Sum	C_{out}	Sum_1	C_{out1}	Sum_2	C_{out2}	Sum_3	C_{out3}	Sum_4	C_{out4}
0	0	0	0	0	0✓	0✓	1 x	0✓	1 x	0✓	0✓	0✓
0	0	1	1	0	1✓	0✓	1✓	0✓	1✓	0✓	1✓	0✓
0	1	0	1	0	0 x	1 x	1✓	0✓	0 x	1 x	0 x	0✓
0	1	1	0	1	0✓	1✓	0✓	1✓	0✓	1✓	1 x	0 x
1	0	0	1	0	0 x	0✓	1✓	0✓	1✓	0✓	0 x	1 x
1	0	1	0	1	0✓	1✓	0✓	1✓	0✓	1✓	0✓	1✓
1	1	0	0	1	0✓	1✓	0✓	1✓	0✓	1✓	0✓	1✓
1	1	1	1	1	1✓	1✓	0 x	1✓	0 x	1✓	1✓	1✓

Table1: Truth Table for Conventional FA & Approximations 1-4 both 1-bit and 4-bit.

V. SIMULATION RESULTS

The proposed 4-bit Conventional full adder Approximations 1-4 simulation results are shown in below

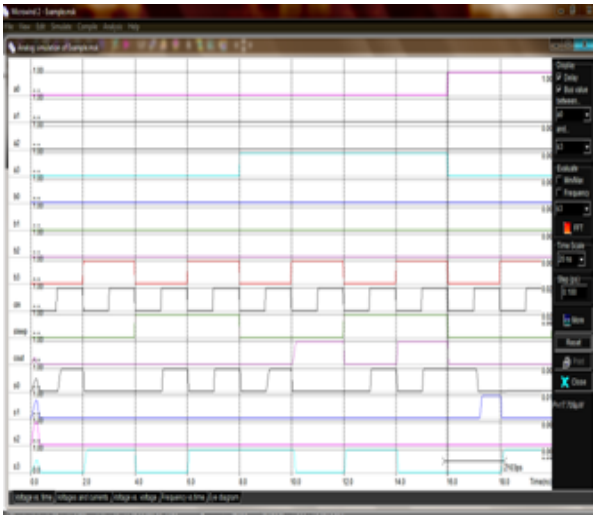

Fig12: Conventional FA

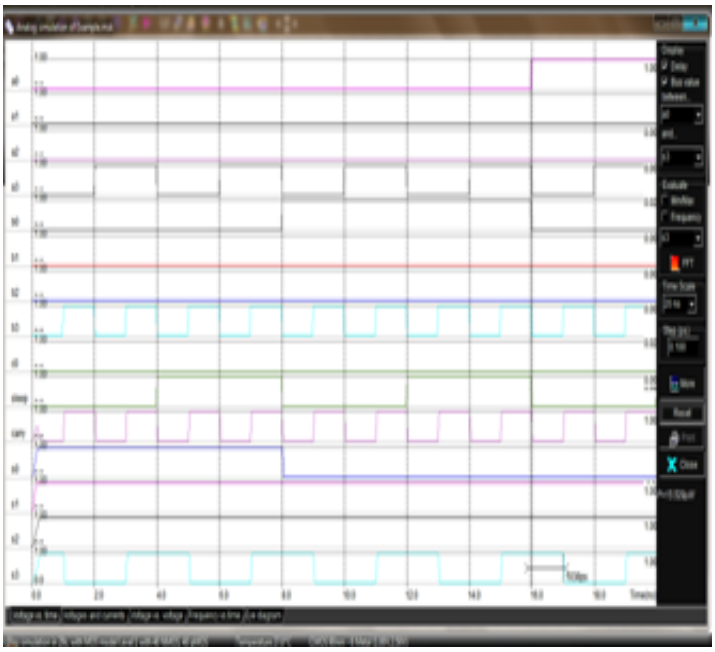

Fig13: Approximation 1

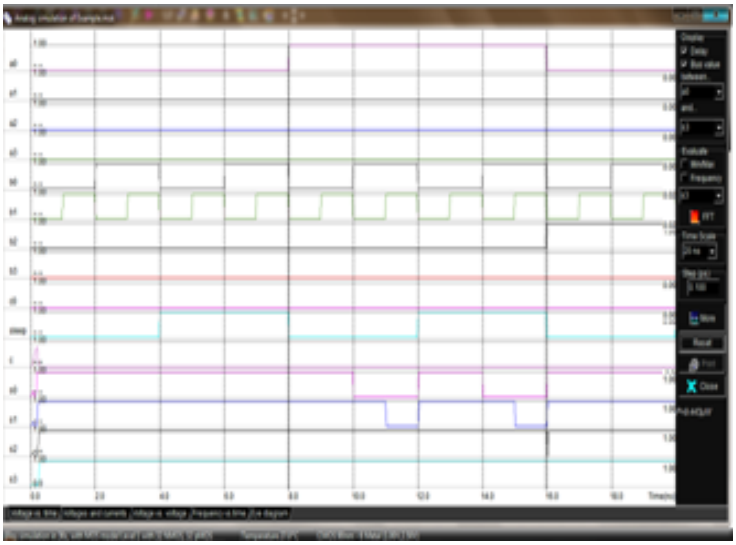

Fig14: Approximation 2

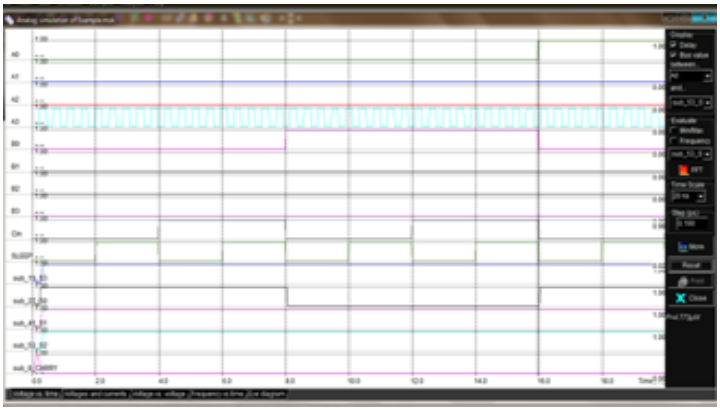

Fig15: Approximation 3

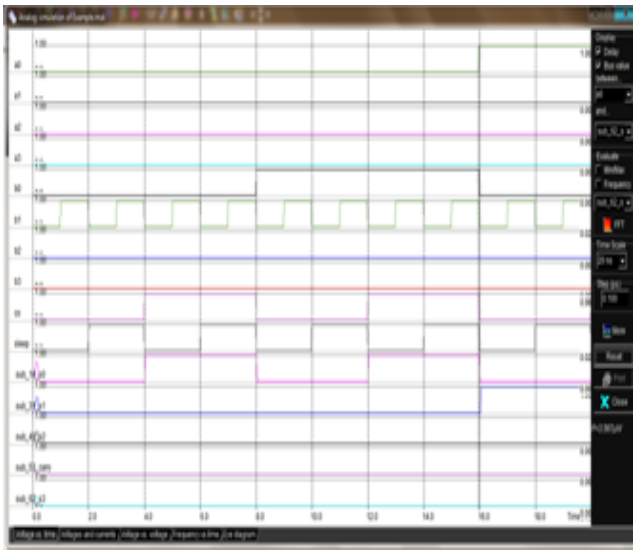

Fig16: Approximation 4

The Conventional FA and Approximations produces different power analysis shown in Table 2.

Table2: Power analysis

METHODS	TECHNOLOGIES			
		120nm	90nm	70nμm
CONVENTIONAL MIRROR ADDER	1-bit	27.240μW	22.297μW	16.901μW
	4-bit	28.307μW	17.709μW	16.878μW
APPROXIMATION 1	1-bit	20.599μW	18.305μW	6.694μW
	4-bit	20.073μW	15.529μW	8.395μW
APPROXIMATION 2	1-bit	12.971μW	9.783μW	4.338μW
	4-bit	12.330μW	9.443μW	4.298μW
APPROXIMATION 3	1-bit	15.270μW	13.133μW	5.504μW
	4-bit	5.857μW	4.773μW	3.134μW
APPROXIMATION 4	1-bit	10.995μW	8.063μW	3.875μW
	4-bit	4.415μW	3.567μW	2.188μW

VI. CONCLUSION

In this paper, our approach aimed to simplify the complexity of a conventional MA cell by reducing the number of transistors and also proposing approximate four bit full adder cells for aimed to reduce leakage power and power consumption by using of sleep transistor. These four bit adders are implemented using 1 bit adder as

reference .We have performed simulations using microwind tool [6] in different Nano meter technologies with standard CMOS technology.

REFERENCES

[1]"Low-Power Digital Signal Processing Using Approximate Adders",IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 32, NO. 1, JANUARY 2013, Vaibhav Gupta, Debabrata Mohapatra, Anand Raghunathan, Fellow, IEEE, and Kaushik Roy, Fellow, IEEE

[2] "Design Of Low-Power Approximate Adders For Signal Processing Applications" R.Sabitha1, K.Sharmila2, M.Sindhuja3,T.Suganya4 VSB Engineering College/Dept of ECE, Karur, Tamilnadu, India.International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 4, April – 2013 ISSN: 2278-0181

[3] 1.V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, "IMPACT: Imprecise adders for low-power approximate computing," in Proc. IEEE/ACM Int. Symp. Low-Power Electron. Design, Aug. 2011, pp. 409–414.

[4] Four-Bit Cmos Full Adder Design in Submicron Technology with Low Leakage Power and Ground Bounce Noise Reduction Using Dual Sleep Approach Y Jagadeesh, T Krishnamurthy.,M.Tech, Dept. of ECE, Assistant Professor, Dept of ECE, SVEC, Tirupathi SVEC, Tirupathi

[5] Design and realisation of Low leakage 1-bit CMOS based Full Adder Cells for Mobile Applications Padma sai .Y1, Rajesh.K2 1working as professor at vnrvjiet, Hyderabad 2Pursuing Mtech at vnrvjiet, Hyderabad IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 3, Issue 6 (Nov. – Dec. 2013), PP 51-57 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197

[6] Microwind and Dsch v3.0 – Lite User's Manual