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RELIABILITY ENSURED TEMPERATURE INSTABILITY SENSOR FOR SRAM MEMORIES

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ABSTRACT

In a Very Large Scale Integrated (VLSI) circuit, memory design and development is the predominant domain. Static Random Access Memory (SRAM) is used as a discrete component in earlier stages of the system design, and now it is used as an Embedded SRAM for System on Chip (SOC) designs. Designing and developing of memory in each manufacturing technology node is continuous challenge and it is the first priority of the evaluation of manufacturing technology. Reliability of a product describes the ability of a system or component to perform its required functions under stated conditions for a specific period of time. Quality of product is decided based on reliability of the chip. For an Integrated Circuit (IC), as a critical product specification under today's aggressive technology scaling, to achieve reliability in leading-edge technology has always been very difficult and costly to measure. In this project, highly reliable NBTI and PBTI sensors based SRAM memory circuits have been designed. The Bias temperature instability (BTI) is known as one serious reliability concern in nanoscale technologies. BTI gradually increases the absolute value of threshold voltage (Vth) of MOS transistors. The main consequence of Vth shift of the SRAM cell transistors is the static noise margin (SNM) degradation. This paper proposes a sensor called write current-based BTI sensor (WCBS) to assess the BTI-aging state of SRAM cells. The WCBS measures BTI-induced SNM degradation of SRAM cells by monitoring the maximum write current shifts due to BTI.

Keywords: SRAM, Static Random Access Memory, Reliability, Bias Temperature Instability (BTI), NBTI, PBTI, Signal to Noise Margin (SNM)

I. INTRODUCTION

The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System-On-Chip and high performance VLSI circuits. Due to the need of battery operated device, the scaling in CMOS technology continues. Nanoscale CMOS SRAM memory design faces several challenges like reducing noise margins and increasing variability, due to the continuous technology scaling. In SRAM the data is lost when the memory is not electrically powered. Advances in chip design using CMOS technology have made possible the design of chips for higher integration, faster performance, and lower power consumption.

To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to smaller dimensions over the last few years. Power consumption of SRAMs account for a significant portion of the overall chip power consumption and due to high density, low power operation is a feature that has become a necessity in today's microprocessors.

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The basic architecture of a static RAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations. Additional support circuitry used to implement special features, such as burst operation, may also be present on the chip

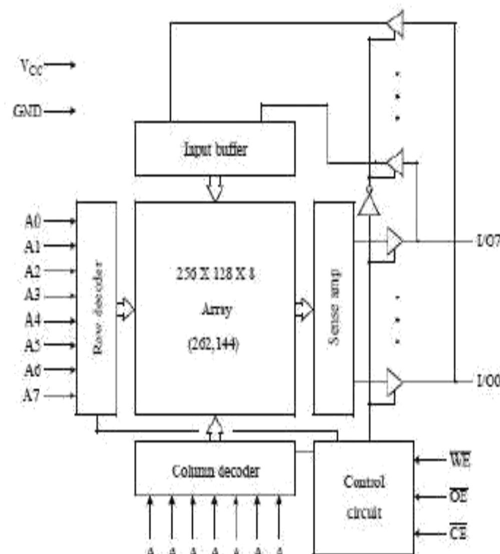

Fig 1 SRAM Block diagram

1.1 CONVENTIONAL 6T SRAM CELL

An SRAM memory cell is a bi-stable flip-flop made up of four to six transistors. The flip-flop may be in either of two states that can be interpreted by the support circuitry to be a 1 or a 0. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices (as opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of poly-silicon, allowing for very high-resistance pull-up resistors.

The principal drawback of using 4T SRAM is increased static power due to the constant current flow through one of the pull-down transistors. This is sometimes used to implement more than one (read and/or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry. Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing silicon wafer is relatively fixed, using smaller cells. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically

provided in order to improve noise margins.

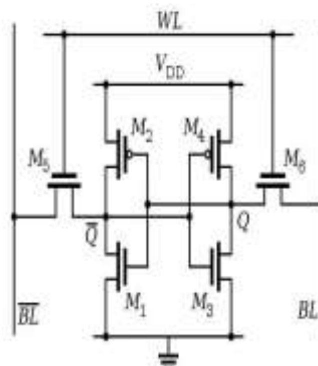

Fig.2 Conventional 6T SRAM cell

READ AND WRITE OPERATIONS

To select a cell, the two access transistors must be "on" so the elementary cell (the flip-flop) can be connected to the internal SRAM circuitry. These two access transistors of a cell are connected to the word line (also called row or X address). The selected row will be set at VCC. The two flip-flop sides are thus connected to a pair of lines, B and B. The bit lines are also called columns or Y addresses. During a read operation these two bit lines are connected to the sense amplifier that recognizes if a logic data "1" or "0" is stored in the selected elementary cell. This sense amplifier then transfers the logic state to the output buffer which is connected to the output pad. There are as many sense amplifiers as there are output pads. During a write operation, data comes from the input pad. It then moves to the write circuitry. Since the write circuitry drivers are stronger than the cell flip-flop transistors, the data will be forced onto the cell. When the read/write operation is completed, the word line (row) is set to 0V, the cell (flip-flop) either keeps its original data for a read cycle or stores the new data which was loaded during the write cycle.

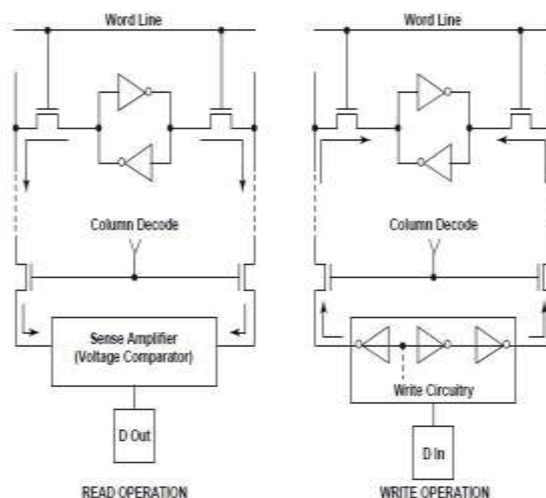

Fig3 Read Write Operation of SRAM

PROBLEMS IN 6T SRAM CELL

The potential stability problem of this design arises during read and writes operation, where the cell is most vulnerable towards noise and thus the stability of the cell is affected. If the cell structure is not designed properly, it may change its state during read and write operation. There are two types of noise margin which affects the Cell stability that are discussed shortly. During the read operation, a stored "0" can be overwritten by a "1" when the voltage at node V1 reaches the Vth of nMOS N1 to pull node V2 down to "0" and in turn pull node V1 up even further to "1" due to the mechanism of positive feedback. This results in wrong data being read or a destructive read when the cell changes state. Conventional 6T SRAM suffers severe stability degradation due to access disturbance at low–power mode.

II. BIAS TEMPERATURE INSTABILITY

One major effect of technology scaling to the nanometer scales is reliability challenges. Among different reliability issues, bias temperature instability (BTI) is the most serious concern. The BTI gradually increase the absolute value of transistors threshold voltage (Vth)and decreases the mobility (μ) of the charge carriers as well. High electric field on the gate insulator, at the elevated temperature, accelerates BTI phenomenon. When a transistor is in linear or saturation state, electric field on gate insulator that reaches to the millions of volts per meter breaks the Si–H bonds, which had been established at the fabrication time to passivate incomplete bonds between Si and SiO2. Interface traps that are generated due to this dissociation slow-down the movement of charge carriers. On the other hand, the generated Si ions, due to Si–H bonds break, push the transistor channel away and increase the absolute value of Vth, forming the stress phase of BTI. On the contrary, when the electric field is removed, some of the broken Si–H bonds will be formed again and put the transistor in the recovery phase. In this way, the previous Vth degradation is partially compensated in the recovery phase. The total effect of BTI is a gradual increase of Vth overtime. The amount of Vth degradation is strongly proportional to the duty cycle (the ratio of stress to recovery time), the supply voltage, and the operating temperature. The effect of BTI on p-type and n-type transistors is called NBTI and PBTI, respectively. In the previous fabrication technology sizes, the NBTI has been far more severe than PBTI; however, nowadays by the development of high-k materials, the PBTI has become a major concern as well. The main effect of BTI on combinational circuits can be observed as propagation delay increase and the delay variation can be accurately monitored using timing violation sensors. But, BTI effect on SRAM cells, which occupy up to 90% of processors die area [14], leads to static noise margin (SNM) degradation. The SNM is the minimum noise voltage that can flip the state of the SRAM cell. However, tiny shift in SNM can hardly be monitor reusing built-in sensors and the sensor precision steps down due to process variation and other environmental parameters change.

III. PROPOSED AGING SENSOR

BTI monitoring is a suitable method to provide a warning signal to prevent system from catastrophic failure due to aging. In this paper, we propose a low area/power overhead NBTI/PBTI sensor to determine aging state of SRAM cells in a memory block. Six transistor SRAM cell structure consists of two cross coupled inverters connected as a positive feedback. During SRAM cell lifetime, two of the four transistors of the cross coupled

inverters are under stress, regardless of the stored value. Holding a constant value, asymmetrically ages SRAM cell and accelerates aging rate. Regarding the fact that a large portion of many kinds of SRAM-based memories store a constant value for a long period of time, due to data dependence, narrow-width values, and special data and instruction patterns, these memories are hardly vulnerable to BTI. This is while the combinational parts experience more relaxation phases due to higher signal activity in average. On the other hand, the effect of BTI on combinational parts is propagation delay shift, which can be accurately assessed using nanoscale CMOS-compatible circuits. However, the major effect of BTI on SRAM cells is SNM shift, which is not measurable as straight forward as delay shift. Also, SRAM aging sensors should monitor all of the cells to be able to report overall aging condition of SRAM block. Hence presenting a method that can monitor BTI in SRAM cells is more challenging.

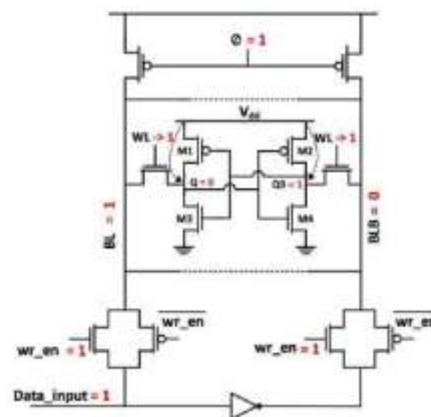

Fig 4. Current flow during SRAM cell Write operation

There can be two situations during the write operation: 1) to write the same value stored in the cell previously and 2) to write different values of the cell. During the first condition, no current is flowed and the effect of Vth shift on the SRAM aging state cannot be observed. Therefore, we evaluate current consumption of the cell during the write operation at the second condition. During the write operation of SRAM cells, Ivdd flows through M1 and M2 which is shown in Fig. 4. Input data is given at data-input line and write enable signal is set to “1.”As Fig. 4 shows, when access transistors turn ON, the current will be drawn from VDD which is exactly equal to p-type transistors currents of SRAM cell. Hence, despite of bit lines currents, Ivdd strongly depends on the p-type transistors currents. Actually, during the write operation, Ivdd is equal to the total of p-type transistors currents of the SRAM cells

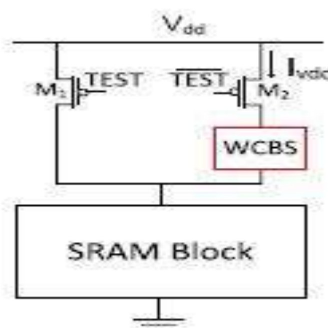

Fig 5. NBTI Sensor based SRAM Memory

The WCBS can be connected to the SRAM block with almost no effect on its normal operation condition. Fig. 5 shows this connection. In the test phase, the test signal is triggered high, which turns ON *M*2. In this case, by writing on the SRAM block, *I*vdd flows into the SRAM block through the WCBS to measure SRAM cells NBTI aging state. This is while during the normal SRAM block operation, *M*1 is ON and the WCBS is not in the path of *I*vdd flow. As the same way, the connection of WCBS to the SRAM block, to monitor the maximum of *I*gnd, in order to measure PBTI aging state, is shown in Fig. 6. It should be mentioned that the supply voltage of the SRAM block should be separated from the logic block of the SRAM cell, which normally is and *I*vdd/*I*gnd, which is shown in Figure purely drives SRAM cells. In the test phase, the test signal becomes "1," thus M2 turns ON and the write current is given to the sensor for measuring BTI-aging condition. However, during the normal operation of the SRAM block, when the test signal is "0," M2 turns OFF and the power of the other parts of the sensor is gated (not shown in the figure for simplicity).

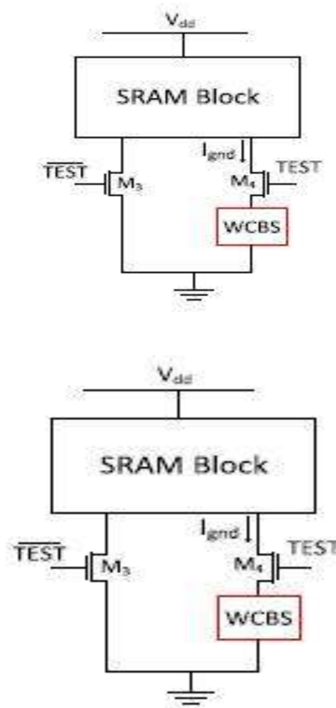

Fig 6. PBTI sensor based SRAM memory

This is the idle time of the sensor. Because aging is a gradual process [9], [10], the test procedure will be done infrequently within long intervals, which can be once a week or month. Hence, the idle time of the sensor is much more than the working time and the sensor components are usually inactive. Therefore, the BTI effect on the sensor itself is quite negligible. The peak of the overall current, which is drawn from VDD during the write operation, is equal to the total of the write current (dynamic current) and the leakage current of SRAM cells. However, the differences of the peak write current between the fresh and the aged conditions reveal the

aging states, not the absolute values of the write current. Hence, the leakage currents existing in two conditions will be eliminated to a large extent and the write current differential variations show the aging states of the SRAM cells.

IV.EXPERIMENTAL EVALUATION

The proposed aging sensor netlist is implemented and was analyzed using Synopsys HSPICE with 65-nm predictive technology model. In our simulations, the cell and pull-up ratios, providing the desirable stability for read/write operation, are 1.2 and 0.5, respectively. Cell ratio is the ratio between the sizes of the driver transistor to the access transistor, defined for the proper read operation. Pull-up ratio is the ratio of the size of the load transistor multiplied by the mobility of holes to the access transistor multiplied by the mobility of electrons defined for the proper write operation and compares the amount of current consumption change between the initial point (non aged condition with Vth shift of 0 mV) and the aged point during the write operation.

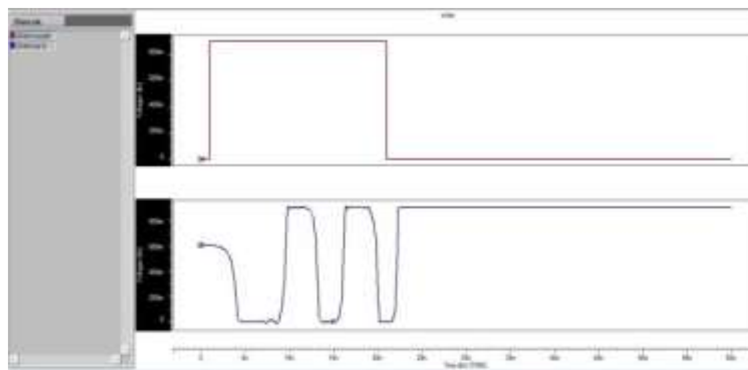

Fig 7. Simulation Results of WCBS

To measure the SNM of the SRAM cells, utilized two noise voltage sources between storage nodes of the cross coupled inverters to determine the least noise voltage that flips the stored value [34]. Simulations are done for the SRAM Block with 32 bit each row, and Vth shifts are applied to the transistors of the SRAM cells in a row to mimic the BTI effect.

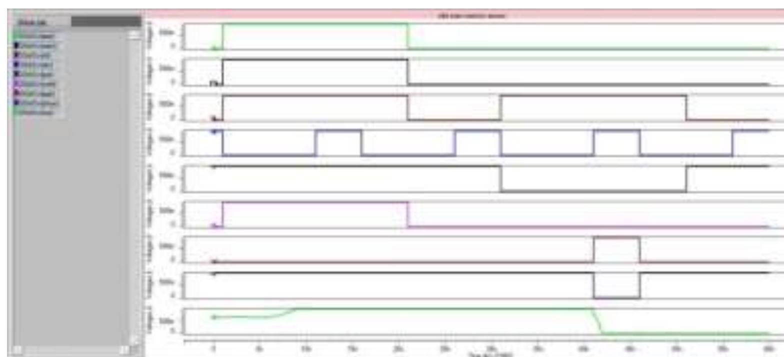

Fig 8. NBTI SRAM memory sensor simulation Results

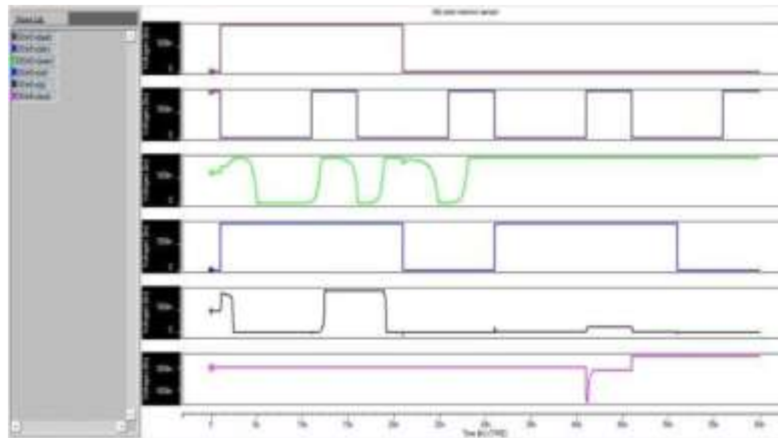

Fig 9. PBTI SRAM memory sensor simulation Results

Cell and pull-up ratios are set such that the strength of pull-down/pull-up transistors be larger/smaller than the access transistors of the SRAM cell, to make a valid read/write operation. Our sensor detects aging state of SRAM cells in a differential manner. This means that it obtains fresh and aged peak write current of target SRAM cell/cells (which are then translated into the corresponding frequencies). The proposed sensor (WCBS) investigate the effect of temperature on the write current, we simulated the peak write current under different aging conditions between 0 and 100 mV of Vth degradations, for the temperatures between 0 °C and 100 °C in Fig. 9. Shows that different temperatures are effective on the write current consumption change by about 2%.On the other hand, in different temperatures, the rate of current consumption reduction between each two points remains the same. The constant current consumption reduction makes the results predictable and accurate for different conditions.

V. CONCLUSION

The BTI is one of the worst challenging reliability concerns in nanoscale technology sizes, which leads to Vth shift of transistors. Vth shift in the transistors of SRAMs results in the SNM degradation over time. Our aim in this paper was to propose a sensor to accurately measure BTI degradation in SRAM cells to monitor the SRAM cells aging status. For this purpose, the peak of Ivdd/Ignd of the SRAM block is monitored during write operation as an indicator of SRAM cells NBTI/PBTI-aging. This current is captured and converted to corresponding voltage by theCCVS. Peak of this voltage controls the oscillation frequency of the VCO. The oscillation frequency shift in comparison with referenced frequency of a fresh cell shows the amount of the BTI effect. By special values written on the SRAM cells, the BTI state of one row down to one cell can be measured. The precision of the sensor is about 1.25 mV & 3.2% error and the area overhead is less than 1%.

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