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FAST BINARY COUNTERS BASED ON SYMMETRIC STACKING

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Abstract—in this paper one new binary counter is proposed which is very fast when compared to other usual parallel counters. First, we are designing binary counter using solely full adders and after with new symmetric stacking method. We are evaluating these two techniques and displaying how the symmetric stacking method is decreasing the x-or gate delays in the essential route of the binary counter. This kind of our proposed counter is very useful in the existing counter based totally Wallace tree multiplier design. With this new symmetry stacking counter we are lowering delay and increasing the performance of multipliers in VLSI circuits. we are designing and simulating our proposed quick binary counter using Xilinx ISE layout suite 14.5.

Keywords- binary counter, full adder, symmetry stacking, 6:3 architecture, wallace tree multiplier, Xilinx 14.5

I. INTRODUCTION

To sketch a first-rate computational unit in VLSI circuits we need quick and environment friendly multipliers and adder units. Especially in multipliers after generating the partial merchandise including of these partial merchandise play an important function to determine the efficiency of the total computational unit. To velocity up the addition of partial merchandise in multiplier graph we are the use of 1/2 adders, full adders as proven in figure1.One full adder makes 3 input operands into two output operands. we are designing these full adders by the usage of x-or gates. But these XOR gates take a lot of time to compute the data. We can also add partial merchandise using specific full adders which are designed with two 2:1 MUX and one XOR gate. So that we can reduce the extend by way of the use of this one of a kind adder two

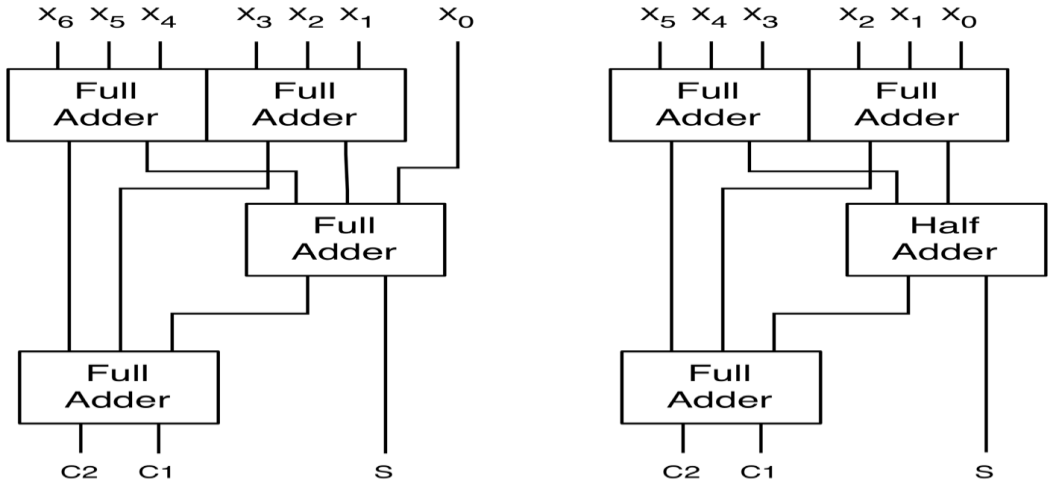

Fig1.binarycounter using full adders

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The velocity of multipliers is a crucial difficulty in identifying the overall performance of microprocessors. Microprocessors use multipliers inside their arithmetic common sense units. the DSP systems require fast multipliers in such as convolution and filtering applications. The demand for high-speed multipliers is always growing

The Fast Multiplication Process

The quickly multiplication process consists of three steps:

• Partial product generation,

• Partial product discount and

• Final lift propagating addition.

Various recoding schemes are used to limit the wide variety of partial products. Compressors have been broadly used for discount method which generally contributes the most to the delay, power and region of the multiplier. To reap a better performance, the use of greater order compressors alternatively of conventional compressors, e.g. 3:2 compressors, have been considered. The reduction procedure subsequently outcomes in a 2-row matrix, and then a high-speed adder is used to get the ultimate result from the two rows. Several kinds of implementation primarily based on the conventional 6:3 structure proposed to be used for quickly multiplication or a couple of addition applications.

In this we are the use of the binary counter which is designed with bit stacking technique to add the partial products in a multiplier. First we present a counting method that makes use of bit stacking circuits accompanied by way of a novel technique of combining two small stacks to shape larger stacks. A 6:3 counter built using this technique makes use of no XOR gates or multiplexers on its necessary path. VLSI simulation effects show that our 6:3 counter is at least 30% quicker than existing counter designs whilst additionally the use of less power. The

identical counter-based Wallace multiplier layout was once used for every simulation, while the interior counter was once varied.Use of the proposed counter improves multiplier effectivity for giant circuits, yielding 64- and 128-bit multipliers that are every faster and consume a whole lot less energy than exceptional counter based totally Wallace (CBW) designs.

II. Three -Bit Stacking Circuit

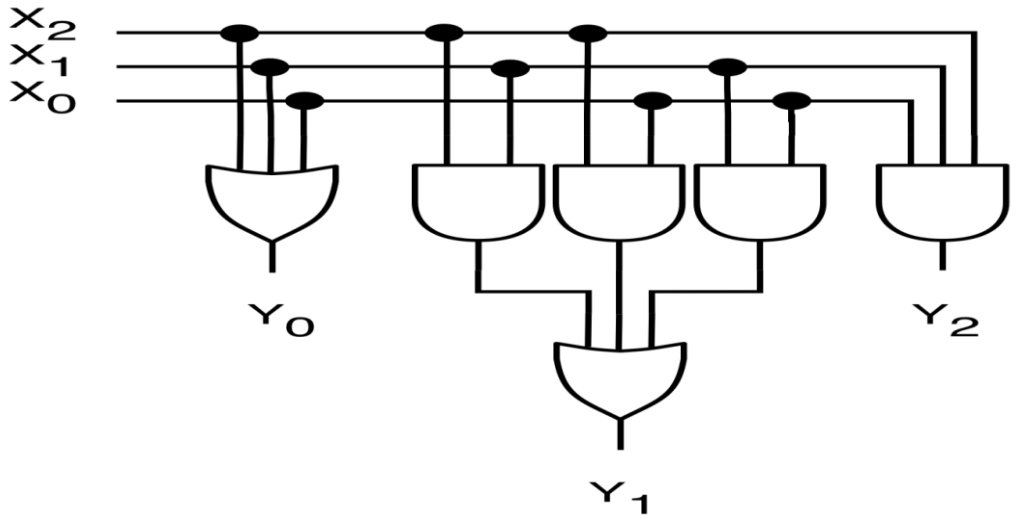


Fig2:three-bit stacking circuit

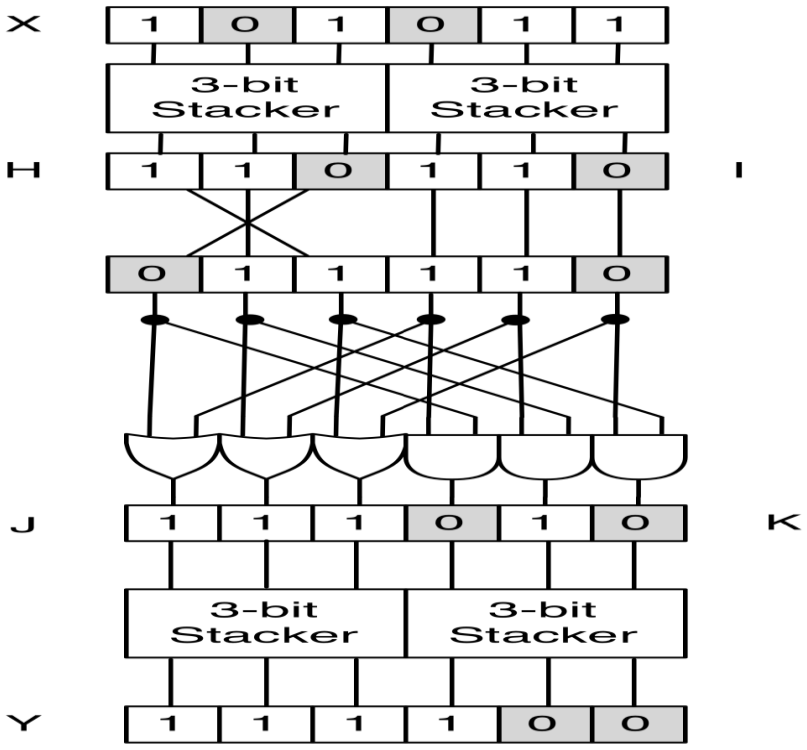
Given inputs and outputs of stack is given as follows*X*0, *X*1, and *X*2
Y0, Y1, and Y2
we are getting outputs as follows

- *Y0 = X0 or X1 or X2*
- *Y1 = X0X1 + X0X2 + X1X2*
- *Y2 = X0X1X2.*

Namely, the first output will be "1" if any of the inputs is one, the second output will be "1" if any two of the inputs are one, and the last output will be 1.. The 3-bit stacking circuit is shown in Fig

IIIMerging 3 Bit Stacks into 6 Bit stack

fig3: symmetric stacking counter example



In the above instance first we are the use of 2 three bit stacks at first level. In the output of first stage stacks we are getting two sequences of 1's and two zeros. it is not appropriate stack alignment. So now we are interchanging the bits of one stack then we are getting one team of 1's surrounded by means of two zeros as shown in figure3..it is additionally no longer perfect two stack alignment .so this time we are the utilization of two another couple of 3- bit stacks. Now we are getting our required stack alignment all 1'right-hand aspect and all 0's are on left-hand side

IV. CONVERTING BIT STACK TO BINARY NUMBER

In order to plan 6 bit counter we have to convert above 6-bit stack into a binary number. for higher appreciation two we are the usage of intermediate values H ,I,K and labeling inputs as x0.x1,x2,x3,x4,x5 and outputs as S,C1,C2.

We can calculate S by using the formula

S = He ⊕Ie.

Where ***He=*** Even parity which occurs if zero or two "1" bits appear in *X*0, *X*1, and *X*2.

Ie= Even parity which occurs if zero or two "1" bits appear in *X*3, *X*4, and *X*5

To design S we are using one x-or gate.But it is not on the critical path

C1=1 when the count is 2 or 3 or 6

$C1 = (H1 + I1 + H0\ I0)(K0 + \overline{K}1 + K2) + H2\ I2.$

Here *(H*1 + *I*1 + *H*0 *I*0*) indicates* at least two inputs we need to see stacks of length two from either top-level

Stacker, or two stacks of length one,

$(K0 + \overline{K}1 + K2)$ indicates we tend to don't have quite 3 inputs set, we tend to merely got to check that that none of the K bits is about because the K vectors solely set once quite 3 inputs square measure "1,"

H2 I2 indicates if we've got all six inputs as "1." {wecan|wewill|we square measure able to} check this by checking that every one 3 of each the H and that i bits are

Set. As these square measure bit stacks, we tend to merely check the right bit within the stack for this case

we will simply calculate C2 because it ought to be set whenever we've got

At least 4-bit set

We can calculate c2 as

$C2 = K0 + K1 + K2.$

C2=1 if atleast 4bits are 1

By using the above we can design one 6:3 counter except using x-or gate in the necessary path. In this the major drawback is wiring complexity. When in contrast to typical binary counter with the full adder in this we are using greater wires

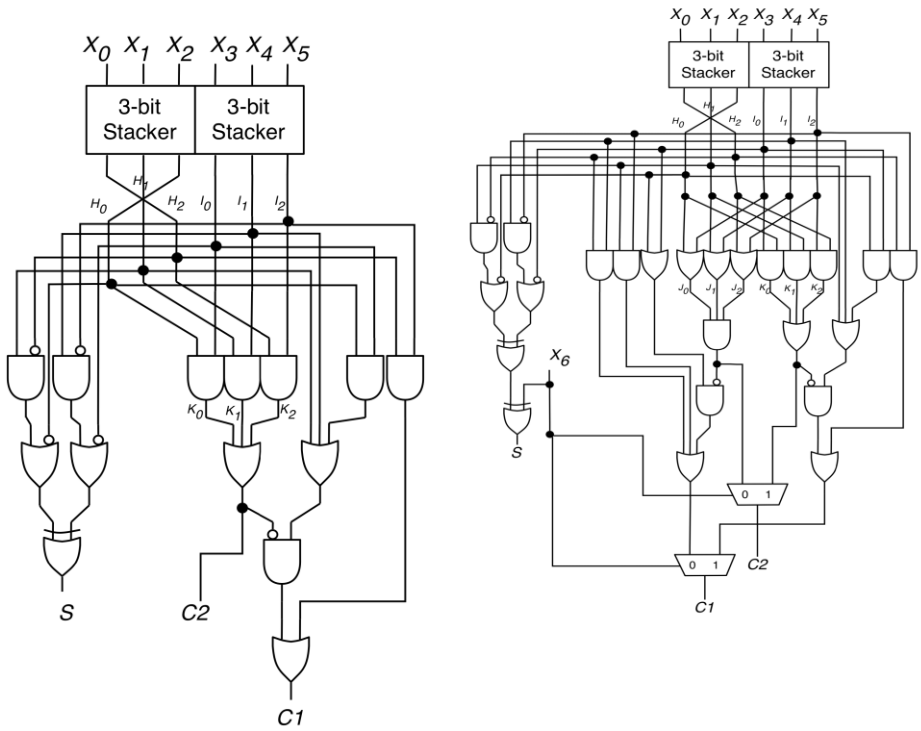


fig4: 6:3 counter and 7:3 counter using symmetric stacking

V.6:3 COUNTER SIMULATIONS

The designed 6:3 symmetric counter is first simulated the use of specter, using the ON semiconductor C5 0.5-µm system (formerly AMI06), and in contrast with traditional counters. When we simulate parallel counter it has given crucial path extend of 3_xor+ 2basicgates.the MUX based totally counter has given the prolong of 1_xor + 3_mux.And our proposed symmetric counter extend is less when compared last counters due to the fact there is no single XOR gate in integral path. it operates almost 30% quicker than all other counter designs. Thus this novel method of counting. The simulated result is in the table1.

Design	Latency (ns)	Avg. Power (µW)	Transistors
CMOS full adders	2.9	124	102
Parallel Counter [4]	2.2	181	158
Mux-Based [6]	1.8	158	112
Proposed	1.4	146	124

Table1: 6:3 Counter Simulation Results

VI. 7:3 COUNTER DESIGN

To get higher compression ratio we are designing 7:3 counter by using symmetric stacking approach.In this we are calculating S by using one extra XOR gate and we are calculating C1 and C2 by assuming X6=0 and X6=1

If X6 = 1, then C1 = one if the count of X0, to, X5 is a minimum of one however but three or five, which may be computed as

C1 = (H0 + I0) J0J‾1 J2 + H2 I1 + H1 I2.

Also, C2 = one if the count of X0, X5 is a minimum of three

C2 = J0 J1 J2.

Both versions of C1 and C2 area unit computed and a MUX is employed to pick the right version supported X6. Note that

This style thus has MUX on the vital path.

Design	Latency (ns)	Avg. Power (μW)	Transistors
CMOS full adders	3.0	222	112
Parallel Counter [4]	2.3	266	178
Mux-Based [6]	2.1	278	120
Proposed	1.8	282	194

.table2:7:3 counter simulation result

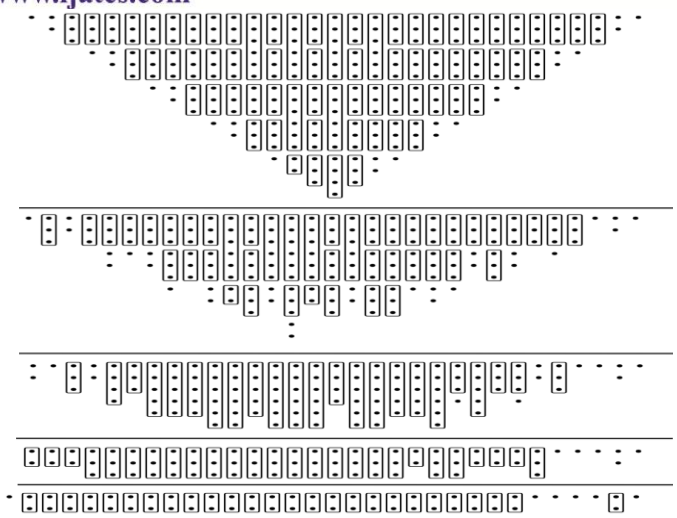


Fig. 5. CBW multiplier reduction tree using up to 6:3 counters

	Latency (ns)				Avg. Power (mW)				Area (Transistors)			
Size	Wallace	[5]	[6]	Stack	Wallace	[5]	[6]	Stack	Wallace	[5]	[6]	Stack
8	5.6	5.8	4.5	5.9	6.0	5.1	5.5	5.3	1.3k	1.3k	1.2k	1.2k
16	10.9	11.4	10.8	11.1	21.5	24.3	24.8	24.3	5.1k	5.9k	5.0k	5.2k
32	11.8	12.9	12.6	11.2	86.9	102	111	94.9	20k	24k	19k	21k
64	14.7	14.4	13.8	12.9	326	423	453	383	76k	99k	73k	86k
128	19.7	19.1	17.7	15.3	1253	1719	1826	1541	305k	400k	301k	344k

Table2: multiplier simulation result

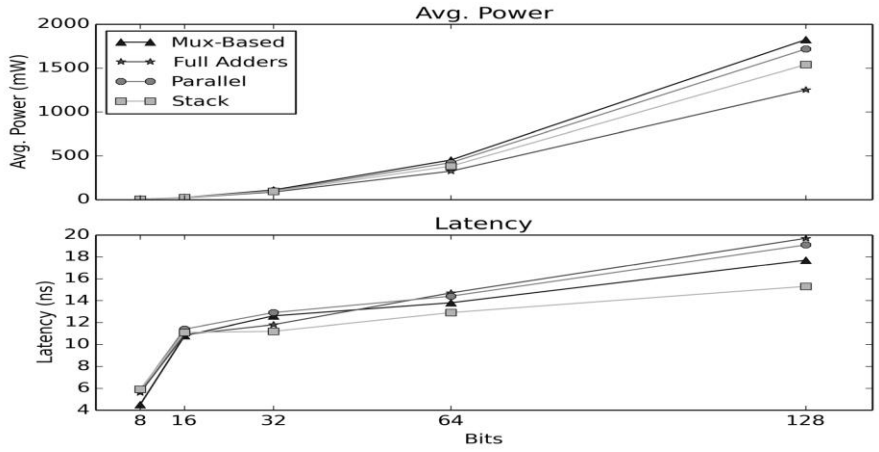


Fig. 6. Power and latency for CBW multipliers with different counters

VI. CONCLUSION

In this we have designed 6:3 binary counter using symmetric stacking approach, and in contrast the parameters such as extend and region of two the proposed counter with usual counters like the parallel counter ,MUX primarily based counter and full adder based totally counters. We run all the types of counters using Xilinx ISE suit14.5 and presented the results. We validated that 6:3 counters carried out with this bit stacking technique achieve higher speed than different greater order counter designs while reducing strength consumption. This is due to the lack of XOR gates and multiplexers on the necessary path. The 64-bit and 128-bit counter based Wallace tree multipliers built using the proposed 6:3 counters .

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