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Design and Analysis of Hybrid Full Adder using 90nm CMOS Technology

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ABSTRACT - This Paper Presents the result and analysis of 1 bit hybrid full adder by deploying transmission gate logic & CMOS gate logic using Cadence Virtuoso with the help of 90nm technology. In this work we have modified the Hybrid Full Adder, using XOR-XNOR Technique in GPDK 90nm Technology, which resulted in reduction of PDP and Noise Margin whereas the transistors were optimally sized to provide improved Voltage Swing. Hence the proposed design gives a remarkable improvement in optimizing the power and delay simultaneously which may be suitable for building block of VLSI Circuit.

***Key Words*:** *XOR-XNOR Technique, GPDK 90 nm, PDP.*

I. INTRODUCTION

The increasing prominence of portable systems and the need to limit power consumption in very high density ULSI chips have led to rapid and innovative development in low-power design in recent years. The need for low-power design is also becoming a major issue in high-performance digital systems, such as microprocessors, digital signal processors (DSPs) another application. Increasing chip density and higher operating speed lead to design of very complex chips with high clock frequency. Full adders are designed using binary adders, by improving 1-bit full adder. Performance plays an important role in VLSI Design and Technologies, which are reported in [1-4] and they unremarkably aim at increasing speed and reducing power dissipation. To improve the performance of adder there we have two methods. One is 'System level viewpoint' method and second method is 'Critical Style View point'. In system level viewpoint it consists of finding the longest path in the ripple adders and reduce the trail so as to

scale back the full signal path delay. The longest signal path is where the carry out bit of the most significant bit has to be calculated in most of the things. The second method is 'Circuit Style Viewpoint' in transistor level, that is, semiconductor device level design skills are supported by designing of high- performance full adder. An optimized design is required to prevent any decrease in signal magnitude, provide small delays consume less

power in critical paths and even at low supply voltage maintain consistency, while moving ahead for smaller designs such as nanometre range.

In previous work, [5-7] – It was aimed to achieve higher speed but keeping power dissipation low, and hence targeting low PDP. Along with the complexity multi-fold reduction in PDP was also achieved. But in all these designs, there was a disadvantage, as it was not able to improve the Noise Margin. In the proposed design "Transistor Sizing" for CMOS circuits was done to balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section. It maximizes the noise margins and provides symmetrical characteristics.

II. BINARY ADDER CIRCUIT

Adder circuit is combinational digital circuit it is kind of calculator is use to add two binary number this one is an important circuit that can be integrated with many other circuits for the wide application, they are also use to calculate address, table indices and other similar operation Half adder, Ful adder and Ripple carry adder is a type of adder, an electronic circuit that can perform the addition of numbers. A fast and energy efficient adder play an important role in electronic industry. In modern VLSI circuit low power and high speed are two important factors. Today increasing number of portable devices that require small area low power.

XOR/XNOR circuits are basic building blocks in Adders, designing efficient reliable XOR/XNOR gates is an important challenge in the area of high-performance computers.

Conventionally, a logical circuit can be realized by canonical CMOS transistors. As usual, the direct conversion from logical gates needs many more transistors. A conversion based on gate level, not on transistor level, will create too much redundancy in the circuit. With the transmission gate theory, the high impendence state is available, the less transistors can be used on the transistor level. XOR and XNOR functions are implemented by transmission gate logic. It gives improved performance in terms of power and delay.

III. PROPOSED HYBRID ADDER

Different logic styles tend to favour one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS), dynamic CMOS logic, complementary pass-transistor logic (CPL) and Transmission Gate full adder (TGA) are the most important logic design styles in the conventional domain.

The proposed Hybrid Adder Circuit architecture is designed as hybrid topology, which is a combination of Static CMOS and Swing Restoring Pass Transistor Logic along with sizing of Transistors, resulting in improved performance of existing XOR/XNOR technique. As shown in Block Diagram below, our proposed hybrid FA is designed by combining CMOS and pass transistor logic styles. This design can be divided in three modules: Inverter, XOR/XNOR and Multiplexer.

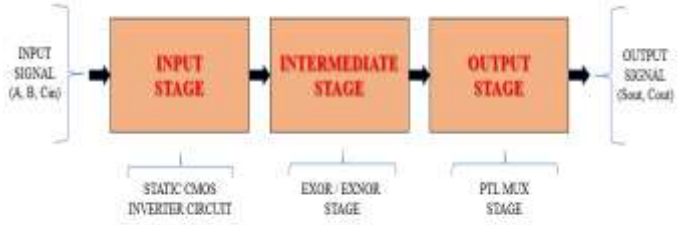

Figure 1 BLOCK DIAGRAM OF PROPOSED MODEL

The output stage of multiplexer module (based on pass transistor logic style) includes two transmission gate-based multiplexers to generate signals Sout and Cout. This topology of Hybrid Adder Circuit consumes less power. Also the transistors were sized with reference inverter $(W/L)_{PUN}$ 3 times as that of $(W/L)_{PDN}$. It can be observed that output signals Sout and Cout can be given by expression as following:

$$\begin{aligned}
&\text{Sum} = A \oplus B \oplus C \\
&\quad = A \oplus X \qquad (\text{where } X = B \oplus C = B'C + BC') \\
&\text{And} \\
&\text{Carry} = ABC + A'BC + AB'C + ABC' \\
&\quad = (A + A').BC + AB'C + ABC' \\
&\quad = BC + AB'C + ABC' \\
&\quad = (BB' + BC + C'B' + C'C).B + AB'C + ABC' \\
&\quad = ((B'C + BC')'.B + A.(B'C + BC') \\
&\quad = X'B + XA \qquad (\text{where } X = B \oplus C = B'C + BC')
\end{aligned}$$

IV. FIGURES AND TABLES

SCHEMATIC DESIGN

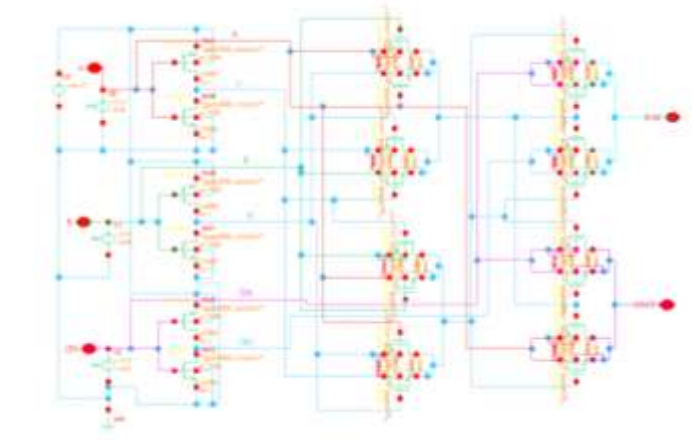

Figure 2 SCHEMATIC DIAGRAM OF PROPOSED HYBRID MODEL

TEST BENCH OUTPUT

The test bench is analysed for 100 MHz square wave input signal with peak voltage of 1V.

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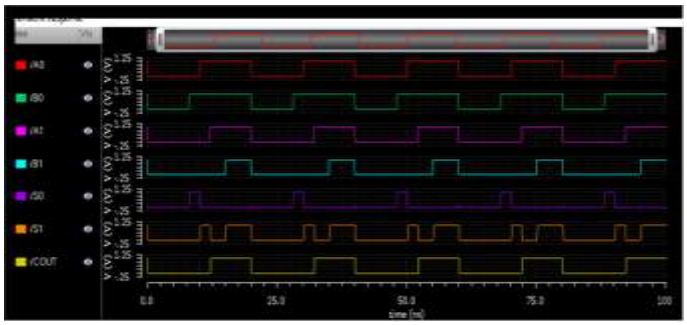

Figure 3 TEST BENCH OUTPUT

POWER DISSIPATION

In order to compute the power consumption, we have to take into account how often the device is switched. If the gate is switched on and off $f_{0\to1}$ time per second, the power consumption equals $P_{dyn} = C_L V_{DD}^2 f_{0\to1,}$ where $f_{0\to1}$ represents the frequency of energy-consuming transitions, this is 0 → 1 transition for static CMOS.

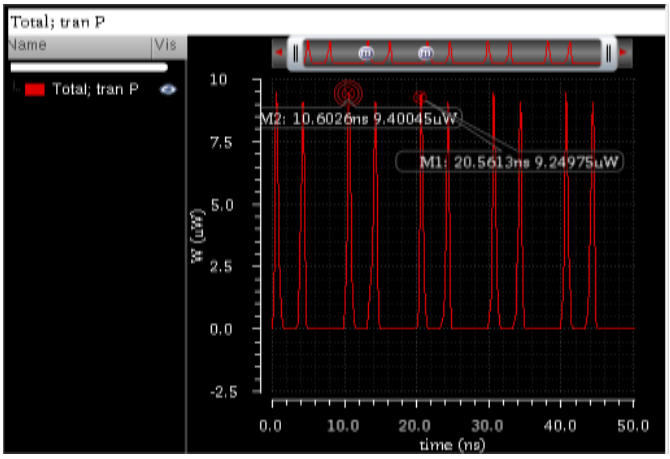

Figure 4 TOTAL POWER DISSIPATION OUTPUT

DELAY CALCULATION

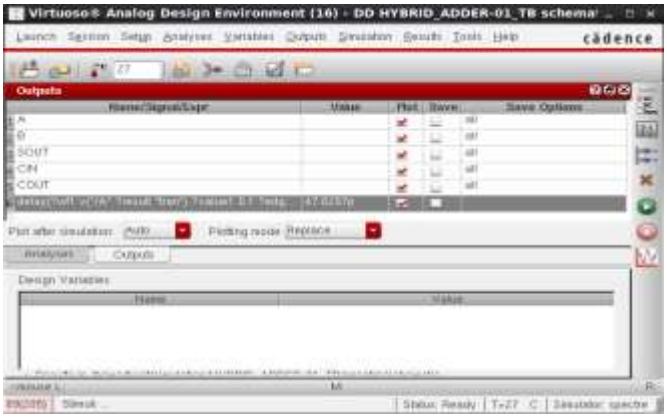

Figure 4 CALCULATED DELAY OUTPUT

COMPARISON TABLE

We have designed Hybrid Adder circuit, which is in order of increasing abstraction, i.e. the device, circuit, gate and the functional module in Cadence Virtuoso Tool. Test bench for each module were created and results have been obtained for power consumption, delay and power delay product.

TABLE I: POWER & DELAY OF EACH DESIGN MODULE

S. No	Design Block	No of Transistors	Average Power (µW)	Delay (ps)	PDP (fJ)
1	INVERTER	2	0.65	121	0.07865
2	NAND GATE	4	2.26	257	0.58082
3	NOR GATE	4	3.53	289	1.02017
4	HALF ADDER	18	9.18	425	3.9015
5	FULL ADDER	42	18.21	760	13.8396
6	2-BIT ADDER	60	37.85	1290	48.8265
7	PROPOSED HYBRID DESIGN	22	9.41	47.1	0.44274

TABLE II: COMPARISON TABLE

S. No.	FULL ADDER DESIGN	Average Power (µW)	Delay (ns)	PDP (fJ)
1	28T MIRROR ADDER	15.91	0.216	3.08
2	HYBRID CMOS 1	18.02	0.159	2.04
3	NEW HPSC	18.58	0.217	3.11
4	TFA	18.07	0.188	2.10
5	TG CMOS	14.98	0.174	1.59
6	FULL ADDER (16T)	28.59	11.512	329.13
7	FULL ADDER (27T)	25.50	6.482	165.33
8	PROPOSED HYBRID DESIGN	9.41	0.047	0.44

V. CONCLUSIONS

In this paper, a full-fledged design for low power hybrid adder is proposed using Cadence Virtuoso with GPDK 90nm Technology by different techniques such as Pass Transistor Logic & Complementary CMOS Technique using 22 transistors.

These designs have been tested in analog design environment. All the Power Consumption calculations have been carried out at 100MHz and 1V power supply. Simulation results prove that Proposed Hybrid Design for Full Adder circuit has lowest Power dissipation of 9.4 µW and PDP 0.44 fJ.

VI. ACKNOWLEDGEMENT

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