International Journal of Advanced Technology in Engineering and Science
Vol. No. 10, Issue No. 06, June 2022
www.ijates.com
ijates
ISSN 2348 - 7550

MODIFIED BORROW SELECT SUBTRACTOR FOR LOW POWER AND AREA EFFICIENCY

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ABSTRACT

Power is one of the most significant designs bound after speed, in integrated circuit. One of the basic essential components in such circuit is adder and subtractor. In order to optimize such circuits, there is need of designing proficient and low power fundamental blocks. This paper presents two architectures of modified borrow select subtractor that consume less power with increased area efficiency. The modifications carried out in the logical flow of subtraction process by using blocks with lower number of logic gates lead to a smaller number of gates, thus resulting in less device count, lower area and lower power dissipation. The synthesis and simulation results are carried out using Xilinx ISE 14.7.

Keywords: *Borrow Select Subtractor, Low Power Subtractor, BSLS, Adder-Subtractor.*

INTRODUCTION

The role of arithmetic circuits in all the signal processing units is of paramount importance and in which Adder-Subtractor circuit is indispensable. Adders, subtractors and multipliers are the essential building blocks of processors. Normally, subtraction is done using adder-subtractor module, which can practically result in slowing down arithmetic operation, since the same hardware has to be used for both addition and subtraction processes using additional control signals. The commonly used Ripple Borrow Subtractor (RBS) used for subtraction of unsigned numbers possesses a simple architecture. However, performance of RBS is limited by borrow propagation time incurred from Least Significant Bit (LSB) to Most Significant Bit (MSB). In other words, the delay of RBS depends on binary word length. Borrow Select Subtractor (BSLS) architecture is proposed here to overcome the limitations of existing RBS with multiple RBS circuits. This method generates partial difference and borrow using multiplexers (MUX) and the final difference and borrow is selected. As the BSLS utilizes multiple RBS circuits in it, it is proved normally area inefficient.

The primary focus is on reducing area and power consumption, which is achieved by using logic blocks with fewer gates occupying less area even while aiming for same logic functionality.

LITERATURE REVIEW

In 2010, Emam [4] proposes two novel designs of Adder/Subtractor using reversible logic gates. The first design is an implementation of two's complement Adder/Subtractor suitable for signed/unsigned numbers. The other design proposes a novel reversible gate that can work singly as a reversible Full Adder/Subtractor unit. The proposed Full Adder/Subtractor is then applied to design a reversible 4-bit ripple Adder/Subtractor.

In 2015, T. F. Tay and C. Chang [5] proposes that efficient modular adders and subtractors for arbitrary moduli are key booster of computational speed for high-cardinality Residue Number Systems as they rely on arbitrary moduli set to expand the dynamic range. This paper proposes a new unified modular adder/subtractor that possesses regular structure for any modulus. Compared to the latest modular adder/subtractor, which works for modulus in the forms of $2^n \pm k$, the proposed design is faster and consumes lower power for n range from 4 to 8.

In 2018, Shabeerkhan [6], proposed Power is one of the most significant designs bound after speed, in integrated circuit. One of the basic essential components in such circuit is adder and subtractor. In order to optimize such circuits, there is need of designing proficient and low power fundamental blocks. we present a new design of the full subtractor based on difference based borrow calculation. The proposed full subtractor is optimized in terms of delay, cost and power. The proposed reversible full subtractor is shown to be better than the existing design. The proposed subtractors proposed in this work will be useful in a number of digital signal processing applications.

EXISTING METHOD

The subtractor circuit analyzes the data with the help of reference signal and allows the signal to the concerned operation without changing its originality. The subtractor circuit is very useful device in signal/data processing, fast multiplier and propagating signals. Low-power IC design has become an especially vibrant area of research and development, resulting in advances in low-power fabrication processes and circuit techniques, dynamically programmable power supplies and power efficient microprocessors.

The difference between the subtrahend and the minuend is in 2's complement form when the subtrahend is greater than minuend. To convert the two's complement form into signed magnitude form, additional blocks are required. When borrow output from unsigned BSLS is 0, the result is positive. Hence, the output doesn't necessitate the conversion to signed magnitude form. Similarly, as borrow output is 1, the result is negative. Then, the output of borrow-out is complemented and 2's complement is performed on entire result in signed magnitude form. Fig. 5 depicts the signed borrow select subtractor. The 16-bit BSLS for unsigned numbers consists of five logic groups. Each group computes the difference and borrow for different number of bits. Each functional group except first group has 2 n-bit RBS, n-bit BEC and a (2n+2):(n+1) multiplexer.

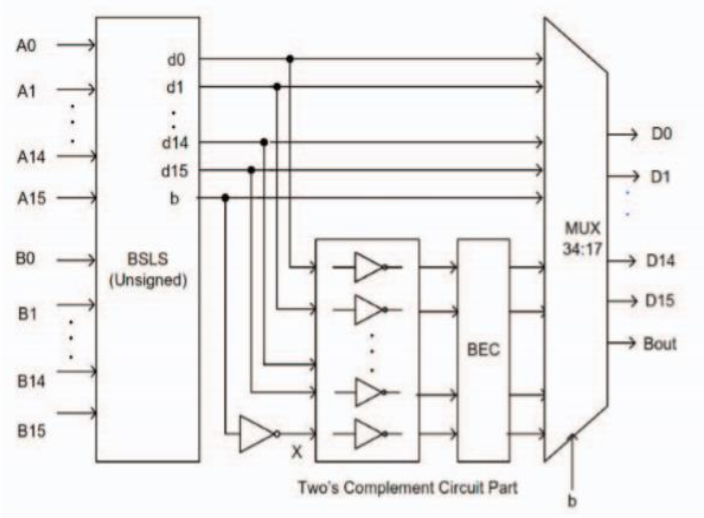

Fig.1. Signed Borrow Select Subtractor

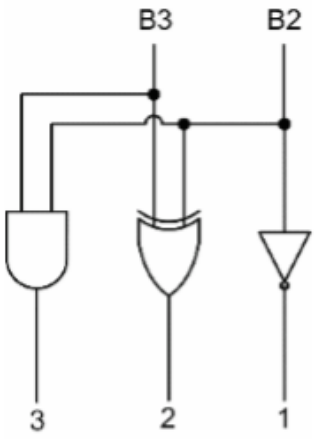

Fig.2. 2-Bit BEC

PROPOSED METHOD

BSLS-BLO: The First proposed architecture replaces the second n-bit RBS and BEC-1 of BSLS using (n+1)-bit Binary-Less-One (BLO) logic in all groups. It uses Binary-Less-One (BLO) logic as shown in Fig.3. for 3-bit BLO logic. The proposed Binary-Less-One (BLO) logic accomplishes the same operation of generating the difference and borrow assuming that the Bin from the previous stage is 1. Fig.4 shows the architecture of the modified Borrow Select Subtractor circuit configured using Binary-Less-One logic (BSLS-BLO). The Binary-Less-One logic is employed in all groups except the group 1 to compute difference and borrow bits.

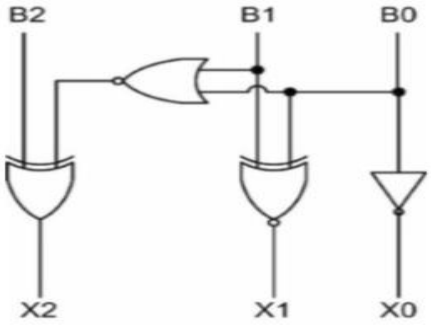

Fig.3. 3-bit Binary-Less-One (BLO)

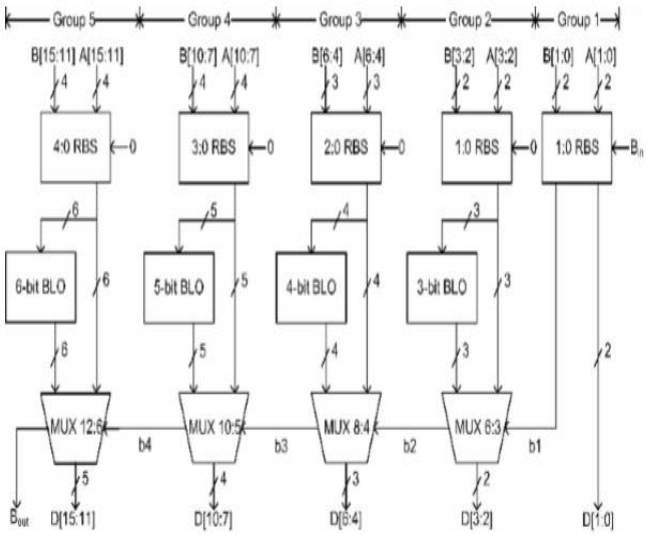

Fig.4. Modified Borrow Select Subtractor using Binary-Less-One Logic

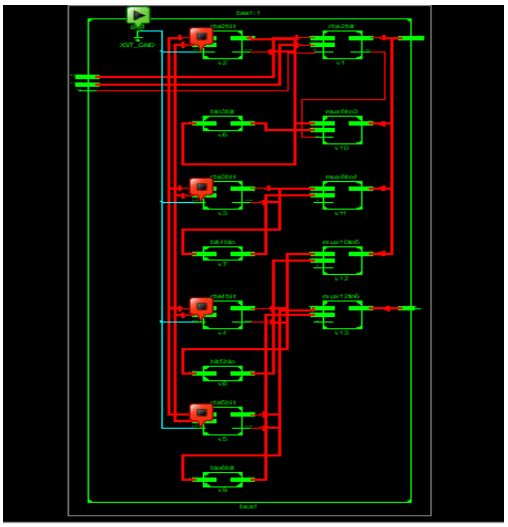

Fig.5. RTL Schematic of BSLS-BLO

BSLS-RBHS: A second variant of the BSLS has been proposed in this Section, which replaces the second n-bit RBS and BEC-1 of BSLS or the n-bit BLO in BSLS-BLO using n-bit ripple borrow half subtractor (RBHS) in all groups. It employs Ripple Borrow Half Subtractor (RBHS) as shown in Fig.6, as depicted for a 3-bit ripple borrow half subtractor (RBHS In this architecture, the (2n+2):(n+1) multiplexer in each group has been replaced with a OR gate. This results in reduction of number of gates. Each functional group except first group has one n-bit RBS, n-bit RBHS and an OR gate. The first group has only one two-bit RBS.Based on the borrow bit Bin generated from the previous group, the difference and borrow bit values have been computed.

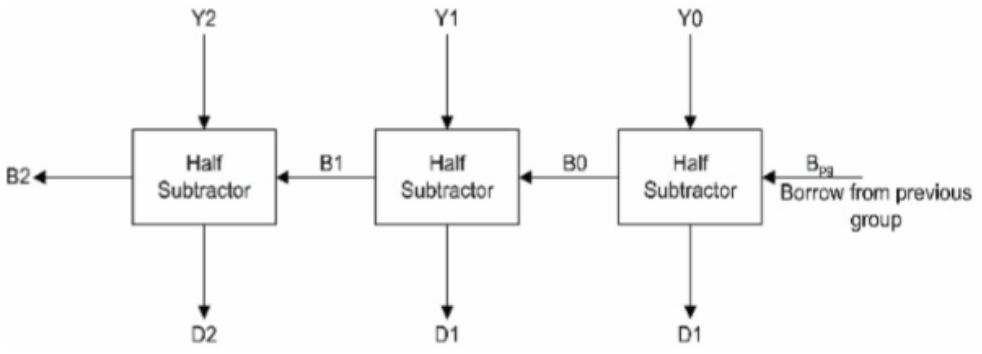

Fig. 6. 3-bit Ripple Borrow Half Subtractor (RBHS)

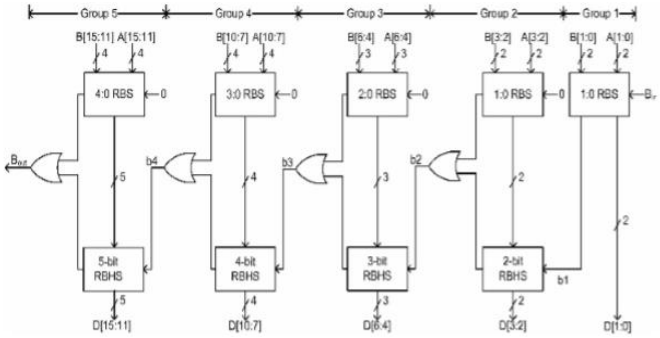

Fig.7. Modified Borrow Select Subtractor using Ripple Borrow Half Subtractor

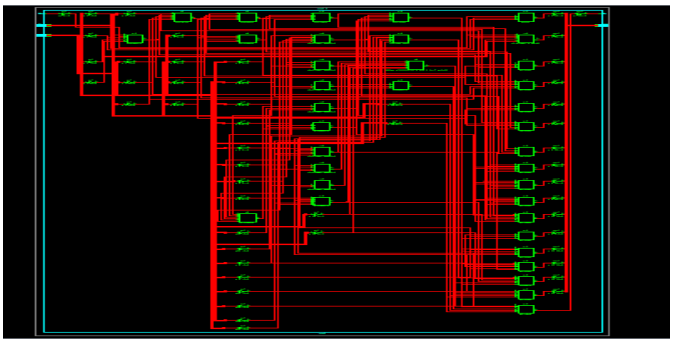

Fig.8. RTL Schematic of BSLS-RBHS

METHODS OR TECHNIQUES USED

Xilinx Tools is a suite of software tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD). The CAD tools enable you to design combinational and sequential circuits starting with Verilog HDL design specifications. Digital designs can be entered in various ways using the above CAD tools: using a schematic entry tool, using a hardware description language (HDL) – Verilog or VHDL or a combination of both. In this lab we will only use the design flow that involves the use of Verilog HDL.

RESULT

The proposed architectures have been designed under the design environment for comparing the results justifiably. The two architectures have been simulated and the area, delay and power reports obtained. These reports were compared with the expected area (by device count), delay and power and tabulated.

International Journal of Advanced Technology in Engineering and Science
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www.ijates.com
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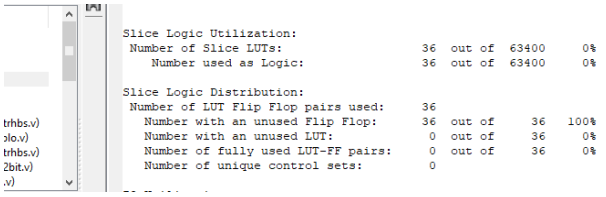
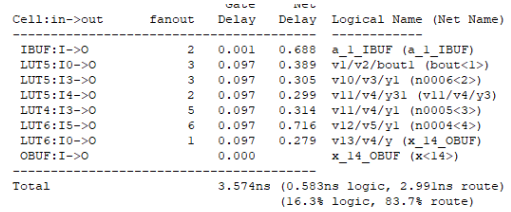


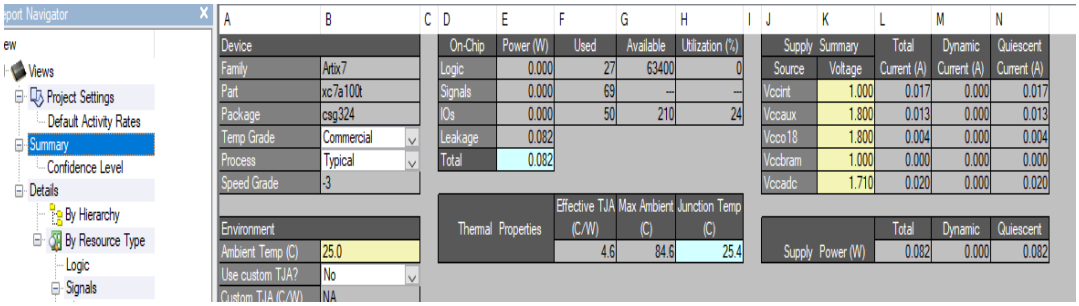
```
Slice Logic Utilization:
 Number of Slice LUTs:                  36  out of  63400     0%
    Number used as Logic:               36  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    36
   Number with an unused Flip Flop:     36  out of     36   100%
   Number with an unused LUT:            0  out of     36     0%
   Number of fully used LUT-FF pairs:    0  out of     36     0%
   Number of unique control sets:        0
```

Fig.9. BSLS-BLO Area



```
Cell:in->out      fanout   Gate Delay   Net Delay   Logical Name (Net Name)
----------------------------------------------------------------------------
 IBUF:I->O             2       0.001       0.688   a_1_IBUF (a_1_IBUF)
 LUT5:I0->O            3       0.097       0.389   v1/v2/bout1 (bout<1>)
 LUT5:I3->O            3       0.097       0.305   v10/v3/y1 (n0006<2>)
 LUT5:I4->O            2       0.097       0.299   v11/v4/y31 (v11/v4/y3)
 LUT4:I3->O            5       0.097       0.314   v11/v4/y1 (n0005<3>)
 LUT6:I5->O            6       0.097       0.716   v12/v5/y1 (n0004<4>)
 LUT6:I0->O            1       0.097       0.279   v13/v4/y (x_14_OBUF)
 OBUF:I->O                     0.000               x_14_OBUF (x<14>)
----------------------------------------
Total                          3.574ns (0.583ns logic, 2.991ns route)
                                       (16.3% logic, 83.7% route)
```

Fig.10. BSLS-BLO Delay



Report Navigator
View
Views
Project Settings
Default Activity Rates
Summary
Confidence Level
Details
By Hierarchy
By Resource Type
Logic
Signals

Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

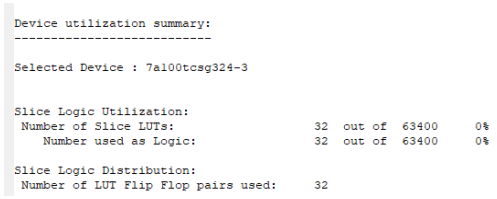
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	27	63400	0
Signals	0.000	69	---	---
IOs	0.000	50	210	24
Leakage	0.082			
Total	0.082			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

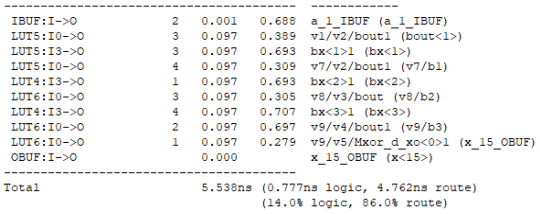
Supply Summary	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Source / Voltage			
Vccint 1.000	0.017	0.000	0.017
Vccaux 1.800	0.013	0.000	0.013
Vcco18 1.800	0.004	0.000	0.004
Vccbram 1.000	0.000	0.000	0.000
Vccadc 1.710	0.020	0.000	0.020
Supply Power (W)	0.082	0.000	0.082

Fig.11. BSLS-BLO Power



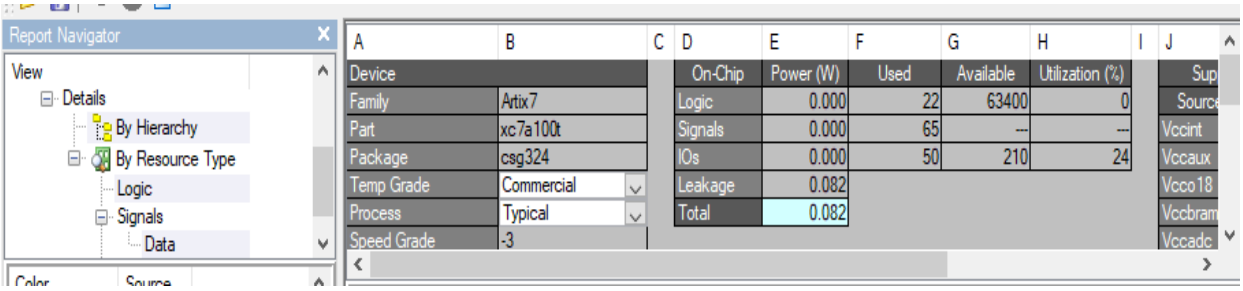
```
Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                  32  out of  63400     0%
    Number used as Logic:               32  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    32
```

Fig.12. BSLS-RBHS Area



```
----------------------------------------  ------------
 IBUF:I->O             2   0.001   0.688  a_1_IBUF (a_1_IBUF)
 LUT5:I0->O            3   0.097   0.389  v1/v2/bout1 (bout<1>)
 LUT5:I3->O            3   0.097   0.693  bx<1>1 (bx<1>)
 LUT5:I0->O            4   0.097   0.309  v7/v2/bout1 (v7/b1)
 LUT4:I3->O            1   0.097   0.693  bx<2>1 (bx<2>)
 LUT6:I0->O            3   0.097   0.305  v8/v3/bout (v8/b2)
 LUT4:I3->O            4   0.097   0.707  bx<3>1 (bx<3>)
 LUT6:I0->O            2   0.097   0.697  v9/v4/bout1 (v9/b3)
 LUT6:I0->O            1   0.097   0.279  v9/v5/Mxor_d_xo<0>1 (x_15_OBUF)
 OBUF:I->O                 0.000          x_15_OBUF (x<15>)
----------------------------------------
Total                      5.538ns (0.777ns logic, 4.762ns route)
                                   (14.0% logic, 86.0% route)
```

Fig.13. BSLS-RBHS Delay



Report Navigator
View
Details
By Hierarchy
By Resource Type
Logic
Signals
Data

Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	22	63400	0
Signals	0.000	65	---	---
IOs	0.000	50	210	24
Leakage	0.082			
Total	0.082			

Fig.14. BSLS-RBHS Power

Table.1: COMPARISION TABLE

ARCHITECTURE	DEVICE COUNT	DELAY	POWER
BSLS	282	5.674ns	210mW
BSLS-BLO (Proposed)	**202**	**3.57ns**	**82mW**
BSLS-RBHS (Proposed)	**142**	**5.53ns**	**82mW**

CONCLUSION

This paper presents modified borrow select subtractor using Borrow Less One and modified borrow select subtractor using Ripple Borrow Half Subtractor. The number of gates employed is less in both proposed architectures compared to existing architecture. On comparing these structures there is 28.36% and 49.64% reduction in device count respectively for Borrow Less One and Ripple Borrow Half Subtractor. This design approach also leads to reduced number of transistors utilized, lower area and reduced power consumption.

Since Mostly adders and subtractors are used in DSP applications which are error tolerant. By applying the concept of approximation, we can achieve better results in terms of area, power and delay.

The future research activities may include integration
of the proposed DFF in complex digital systems,
combining sequential and combinatorial logic.

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