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Performance Evaluation of CAM Using Adiabatic Logic

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Abstract

A design of power efficient content addressable memory is a highly efficient VLSI (Very Large-Scale Integration) based content addressable memory for storage applications. By using energy recycling principle of Binary CAM and ternary CAM adiabatic logic. Basically, CAM (Content-Addressable Memory) is a specialized type of high-speed memory that searches its entire contents in a single clock cycle. In this generalized CAM structure is designed for storage applications which will perform match operation in addition to read and write operation. CAM provides high performances based on content rather than address unlike RAM (Random Access Memory). Hence, this gives effective result compared to other systems. The circuits are designedusing 90nm CMOS technology with power supply of 2.5v using Tanner tools.

Keywords – CAM, Adiabatic Logic, BCAM, TCAM.

I. INTRODUCTION

A Content Addressable Memory (CAM) is a storage device like normal RAM device but in addition to that, this does the search or compare operation [1]. It serves two functionalities: Bit Storage and Bit Comparison [2]. Unlike RAM cell, it takes data as input and gives address as output in one clock period. Search operation is performed in parallel among all memory cells and gives the matched location for the given input data. And this parallel processing of data for search operation due to high switching activity leads to very high-power consumption [3]-[4]. Several Low Power techniques are available. Out of them Adiabatic logic principle works well in energy recycling process and in the depletion of power dissipation.

Various Adiabatic logics have been reported over the past for the low power CAM architectures [3]-[4]. CAMs are widely used in Applications wherever fast parallel search operations are required. These types of applications include translation lookaside buffers, branch prediction buffers, cache tags, database search engines, packet processing in network routers, Internet protocol (IP) address filtering and data compression.

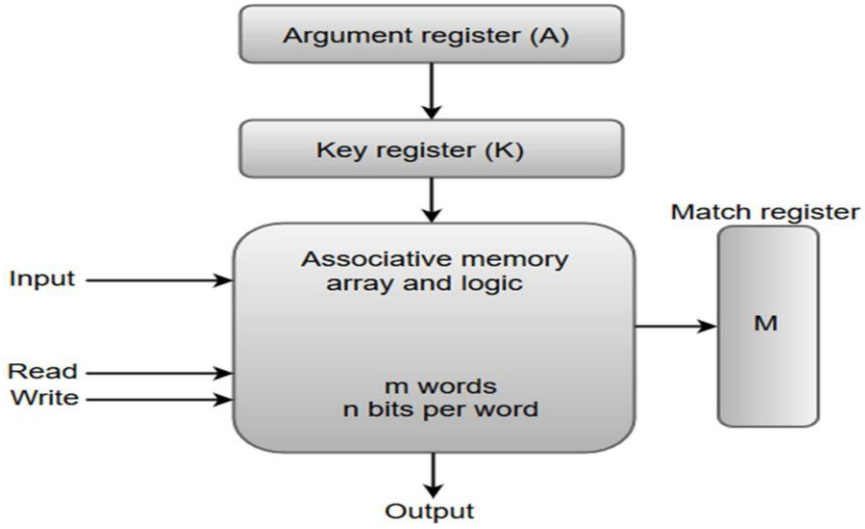

Fig 1. Block Diagram of CAM

Content Addressable Memory is used in very high-speed applications. The CAMs are used extensively in computer networking, Network routers, artificial neural networks and many more [5]. CAM perform search operation through content and provides the address of that particular content, whereas in RAM the search operation is done to obtain the stored data in the address of the memory by giving address [7]. CAM is divided into two categories: (i) Binary CAM (BCAM) (ii) Ternary CAM (TCAM) [8]. Binary Cam is preferred where exact matching is required in terms of 0's and 1's, where as in TCAM, wild bit 'X' (don't care) is used along with 0'sand 1's [9].

In TCAM, the search operation is done by masking globally and locally. Search key is provided to perform global masking and local masking. By providing through the search key masking can be done globally and by providing through the table entries or by storage cells masking can be done locally [10],[11]. CAM perform both write and read operations similar to RAM but perform search operation very faster compared to conventional RAM as CAM searches the entire memory to check whether the CAM memory has the stored data and then a listof address will be returned where the data was found. RAM reads and compares the entries for every request thereby increasing the search time. CAMs are used mainly for high-speed network routers and catching.

II. BINARY CONTENT ADDRESSABLE MEMORY

Content addressable memory consists of SRAM cell built by using 6 transistors along with the matching circuit [9]. 6T SRAM consists of two inverters which are used for storing the data and two extra transistors to actsas access transistors. In addition to this, matching circuit is used to perform search operation. Based on designerand implementation, matching circuit is built either by using XOR or XNOR. BCAM schematic [3] shown in theFig. 2. It is built by using one 6T SRAM cell along with XNOR matching circuit.

The write and read operations are performed as in SRAM. The search operation is carried out by placing the data to be matched on search line and then it is compared with the data stored in SRAM cell. The write operation is carried out by writing the data bit to be written on the bit lines (BLs) and then by enabling the wordline (WL).

This activates the access transistors which in turn store the data bits which are on the bit lines at Vx and Vy. In order to write 1 at Vx, we make BL1=1 and BL1C=0 and then enable WL and activate access transistors which causes the BL currents to flow.

The search operation is performed by precharging ML, the match line to Vdd and bit lines to ground. Then the data bits which are to be searched placed on search lines and compared with the data stored at Vx and Vy. If the data matches then ML, activates to high level. In case mismatch occurs, then the match line takes the value to ground [12]. The bit lines are pre charged to high state to perform read operation and then enabling the word line WL. Between the bit lines, small voltage difference is developed due to the current flowing through thetransistor. This makes the cell not to write anything during the read operation.

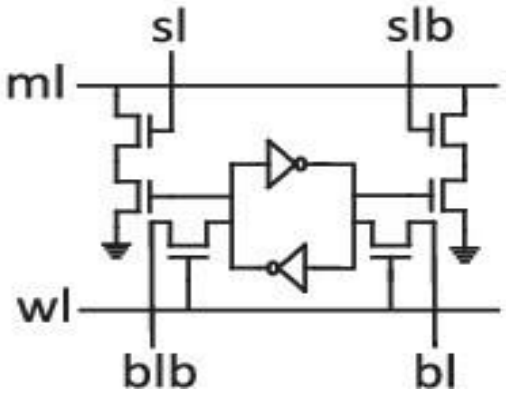

Fig 2. Simple BCAM circuit

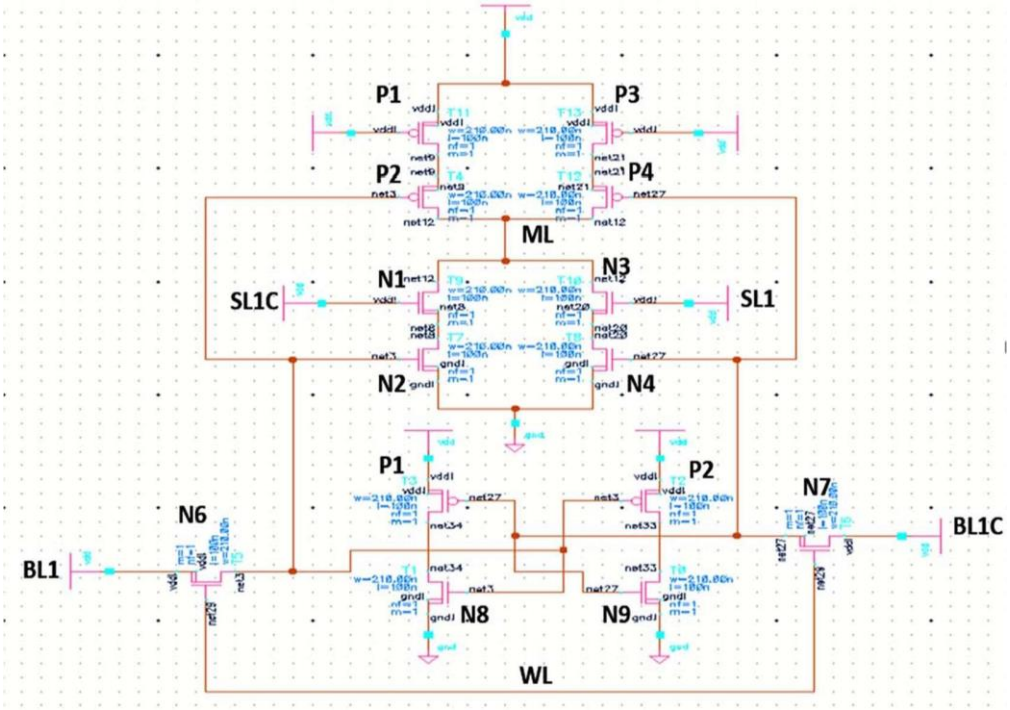

Fig 3. Schematic of BCAM

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III. TENARY CONTENT ADDRESSABLE MEMORY

The schematic of TCAM [3] shown in the Fig. 4. It is similar to BCAM but TCAM consists of 6T two SRAM cell along with the matching circuit which allows the ternary data. Therefore, the memory operations are performed similar to BCAM.

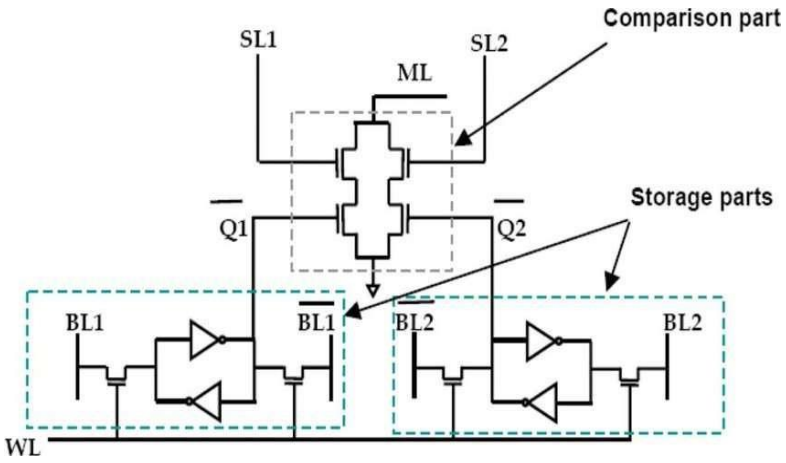

Fig 4. Simple TCAM Circuit

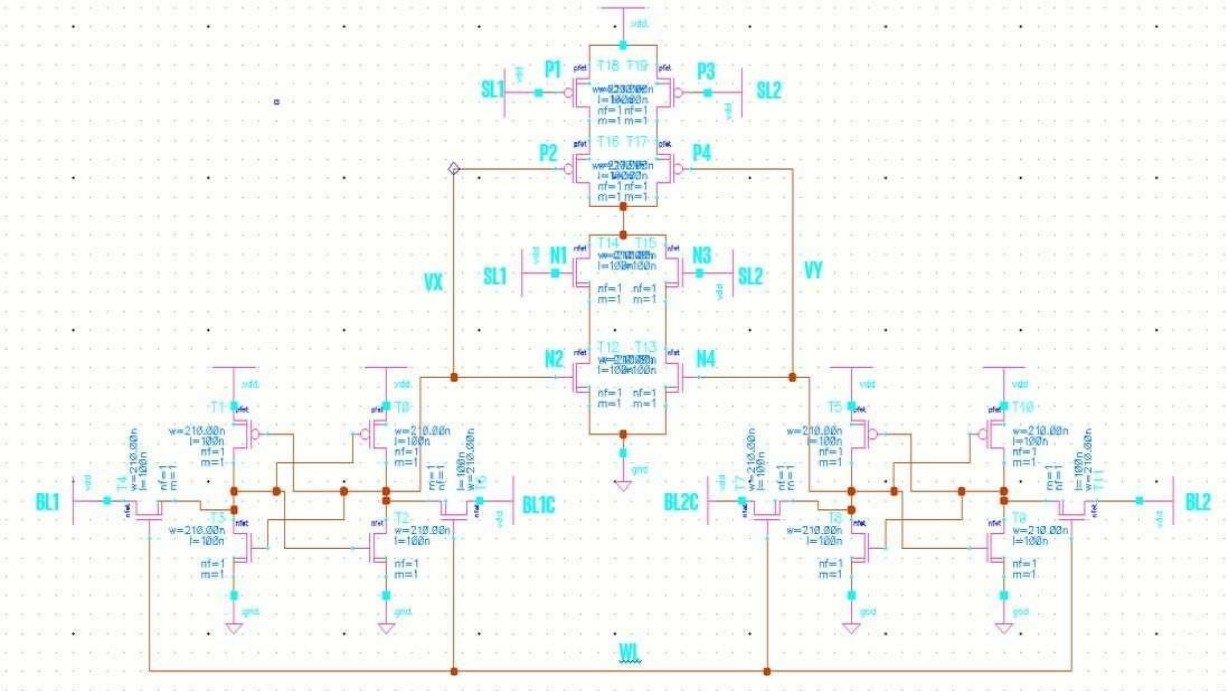

Fig 5. Schematic of TCAM cell

IV. B-TCAM

The Combination of both BCAM and TCAM can be implemented in single circuit as shown in fig.
5. The below figure shows the block diagram of proposed system. Initially, input data is generated from thedata generator and address is allotted to that data using address bus. The address bus is divided into two typesthey are row address and column address [13]. Instruction register is given to the address to perform row andcolumn operation based on instruction command. Both row and column address will transfer data to CMA memory access block to save the data. From this CAM memory access block read and write operations are performed. All these data will be saved in the FPGA memory and it is implemented in Xilinx ISE software tool.

Content-addressable memory (CAM) is a special type of computer memory used in certain very- high-speed searching applications [14]. It is also known as associative memory or associative storage and compares input search data against a table of stored data, and returns the address of matching data.

CAM is frequently used in networking devices where it speeds up forwarding information device and routing table operations. This kind of associative memory is also used in cache memory. In associative cache memory, both address and content are stored side by side. When the address matches the corresponding content is fetched from cache memory using Adiabatic Logic.

Performance improvement of an application through accelerators is achieved by first choosing or detecting demanding computation to be accelerated. Some approaches rely on forms of High-Level Synthesis (HLS), i.e., offline stages involving manual source code analysis or use of tools to identify candidate functions. A translation of high-level code is performed, to automatically generate Hardware Description Language (HDL) code, followed by standard logic synthesis.

This may require modifying source code to allow compatibility with HLS tools, or later modification to allow for integration with the accelerator hardware. In contrast, the approaches addressed throughout this chapter rely on binary information. Approaches of this kind analyses the compiled application, and provide a transparent use of custom hardware for the application programmer. Binary acceleration focuses on exploring Instruction Level Parallelism (ILP).

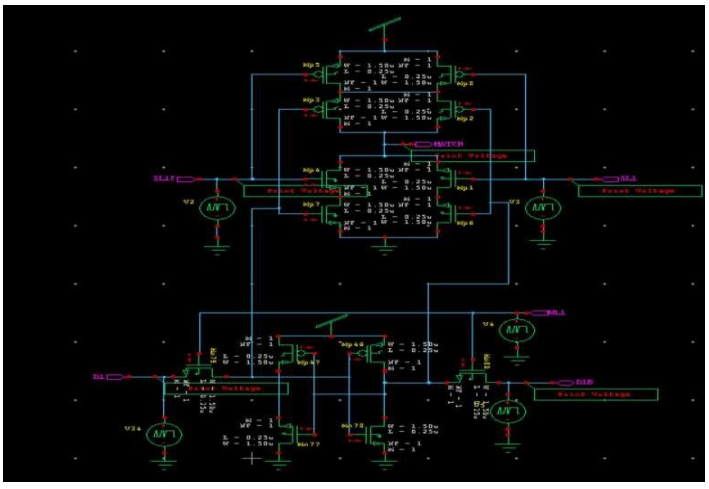

Fig 6. Schematic of B-TCAM

The address generation unit used to produce the address. This address is given as the input to LUT component. The address generation circuit is generally used in conjunction with the control circuit which is usedto produce the control signals s0 and s1 [15],[16]. The control signals are used in the subsequent for the multiplication of any binary word of size L, with a fixed coefficient A, instead of storing all the 2L possible values of C=A*X, only (2L /2) words corresponding to the odd multiples of A may be stored in the LUT [17], while allthe even multiples of A could be derived by left-shift operations of one of those odd multiples [18].

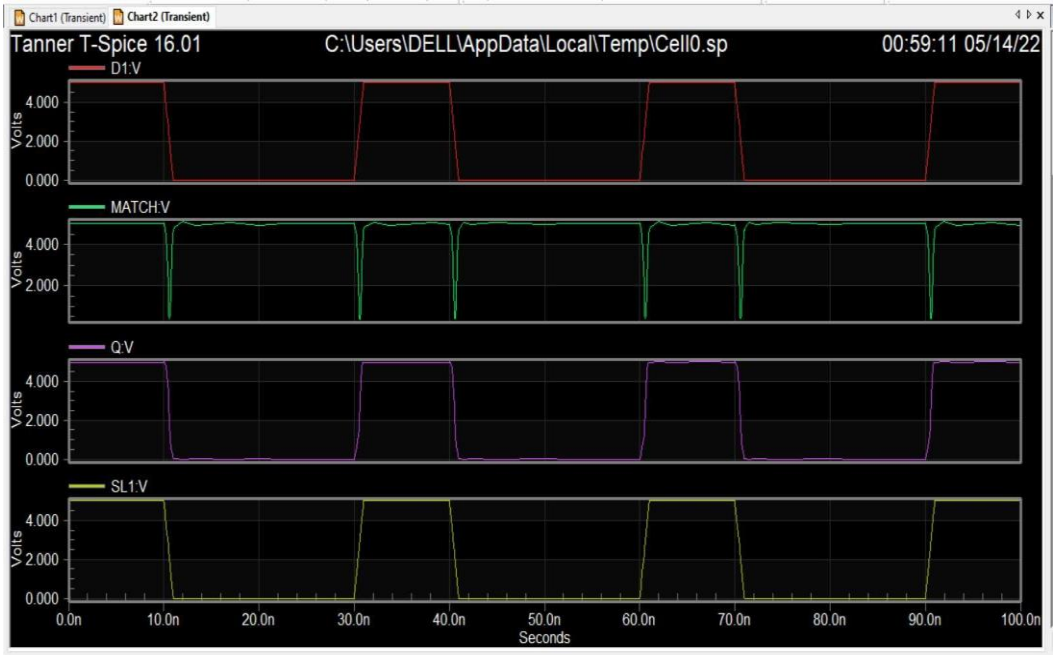

Fig 7. Simulation result of BCAM and TCAM

The simulation can be shown in Fig 7. In this waveform write Data (D1) is given as 100 and its complement can be considered as D1B as 011. Read Data is same as write Data (Q)i.e., 100. Search data (SL) as
100. If write data and the search data is same then we get the Match line as logic 1 otherwise logic 0.

V. CONCLUSION

A Content Addressable Memory (CAM) is a hardware search engine used for high-speed searching/accessing. The utilization of CAM is still constrained in some applications by large power dissipation. Especially, the search approach contributes more power in overall power dissipation. This methodology proposes a CAM cell using split-controlled single ended storage technique to achieve energy-efficient hardware search engine. By using Tanner tools, the design of BCAM and TCAM are implemented in efficient way. The design ofCAM using SRAM and XNOR as the matching circuit. Then the technologies for performing search operation inboth BCAM and TCAM are investigated to obtain better performance. The performance of BCAM and TCAM is analyzed in by using of Tanner tools. Power consumption of BCAM and TCAM Adiabatic logic are adequatelyreduced with power saving of 40% can be analyzed.

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