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DESIGN AND SIMULATION OF A FULL ON CHIP LOW DROP-OUT VOLTAGE REGULATOR AT TRANSISTOR LEVEL FOR CONVENTIONAL SUBMICRON PROCESS

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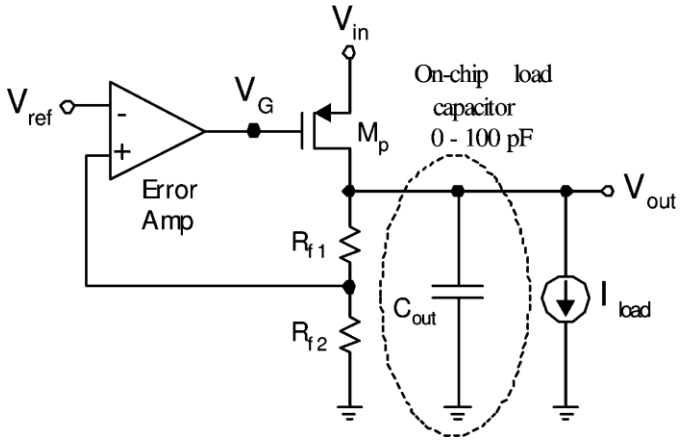
ABSTRACT

This paper will enable the user to understand the operation of Low Drop-Out Voltage Regulators. The most commonly used Regulator used in power management systems be covered. LDO regulators are an essential part of the power management system that provides constant voltage supply rails.Most of the conventional LDO performances are greatly affected whenthe external capacitor is reduced by several orders of magnitude so this study is based onsimulation of chip LDO with variation of output load.

I. INTRODUCTION

Industry is pushing towards complete system-on-chip (SoC) design solutions that include power management. The study of power management techniqueshas increased spectacularly within the last few years corresponding to a vast increase in the use of portable, handheld battery operated devices. Power management seeks to improve the device's power efficiency resulting in prolonged battery life and operating time for the device. A power management system contains several subsystems including linear regulators, switching regulators, and control logic . The control logic changes the attributes of each subsystem; turning the outputs on and off as well as changing the output voltage levels, to optimize the power consumption of the device.

LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with improved power efficiency. Efficiency is improved over conventional linear regulators by replacing the common-drain pass element with a common-source pass element to reduce the minimum required voltage drop across the control device. Smaller voltage headroom in the pass element results in less power dissipation, making LDO regulators more suitable for low-voltage, on-chip,power management solutions.



The conventional LDO voltage regulator, for stability requirements, requires a relatively large output capacitor in the single microfarad range. Large microfarad capacitors cannot be realized in current design technologies, thus each LDO regulator needs an external pin for a board mounted output capacitor. This paper poses to remove the large external capacitor, while guaranteeing stability under all operating conditions. Removing the large off-chip output capacitor also reduces the board real estate and the overall cost of the design and makes it suitable for SoC designs.Removing the external capacitor requires a sound compensation scheme for both the transient response and the alternating current (ac) stability

II. BRIEF DESCRIPTION

2.1 Uncompensated Ldo

Most of the conventional LDO performances are greatly affected when the external capacitor is reduced by several orders of magnitude. The absence of a large external output capacitor presents several design challenges both for ac stability and load transient response. Conventional LDO regulators use a large external capacitor to create the dominant pole and to provide an instantaneous charge source during fast load transients Thus, a capacitorless LDO requires an in- ternal fast transient path to compensate for the absence of the large external capacitor. To realize the task at hand, the basic capacitorless LDO regulator, shown in Fig. 1, is revisited in the following section.

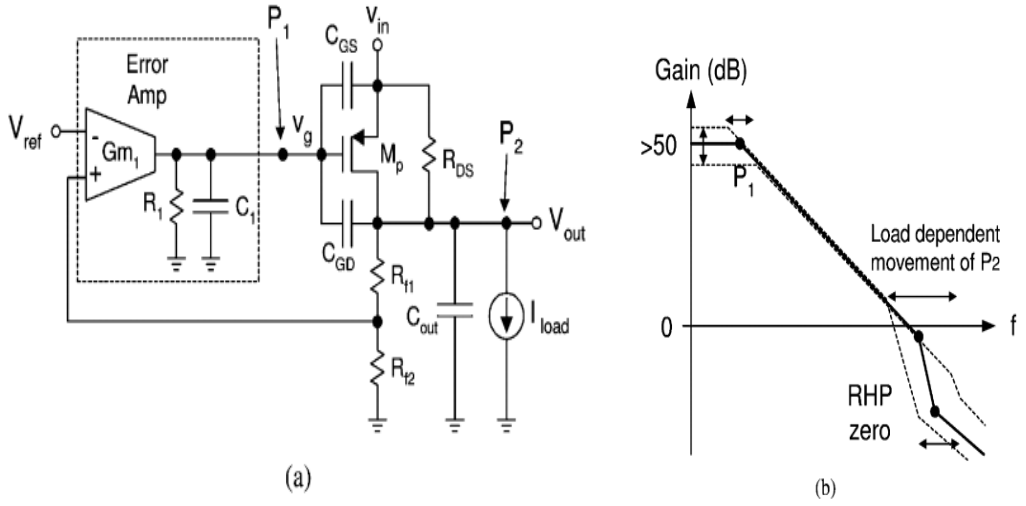


Fig.2.(a) Equivalent circuit of LDO voltage regulator and (b) pole locations for uncompensated capacitor less LDO voltage regulator; C around 100pF

A. Uncompensated AC Response

One of the most significant side effects in LDOs is stability degradation due to the several poles embedded in the loop. As shown in Fig. 2(a), the uncompensated capacitorless LDO has two major poles: the error amplifier output pole P_1 and the load dependent output pole P_2. If the loop is opened, the location of P_1 at the gate of M_p is given by

$$\text{P1} = \frac{1}{R_1 \ (C_1 + C_{GS} + A_{\text{pass}} C_{GD})} \quad (1)$$

.The second pole P_2 is located at the LDO's output

$$P_2 \cong \frac{1}{\left(R_{DS} \| (R_{f1} + R_{f2}) \| R_{\text{out}} \| \left(\left(\frac{C_{GD}}{C_1 + C_{GS} + C_{GD}} \right) \frac{1}{\text{Gm}_P} \right) \right) C_{\text{out}}}$$

The pass transistor Gm_P and R_{DS} increases and decreases, respectively, for increasing load current making P_2 very sensitive to the LDO's load conditions. Large load currents push the output pole P_2 to higher frequencies well past P_1. At low currents, the effective load resistance increases significantly; P_2 is pushed to lower frequencies.Due to the unavoidable parasitic poles, loop stability cannot be guaranteed due to the decreased phase margin. Therefore, the uncompensated capacitorless LDO regulator may not be stable especially at the no-load condition. A side effect ofCgdis the generation of a right-hand plane (RHP) zero Z_1(≈Gmp/Cgd) that re duces loop phase margin; a simplified magnitude plot is shown 2(b)

Conventional LDO regulator analysis usually ignores the feedforward zero due to the pass transistor's C_{GD}.RHP zero Z_1 attracts complex poles to the right-hand side of the S-plane, degrading the loop's stability. The presented external capacitorless LDO regulator requires a gain-bandwidth product of around 500 kHz. At those frequencies, the feedforward zero has noticeable effects at low load currents.

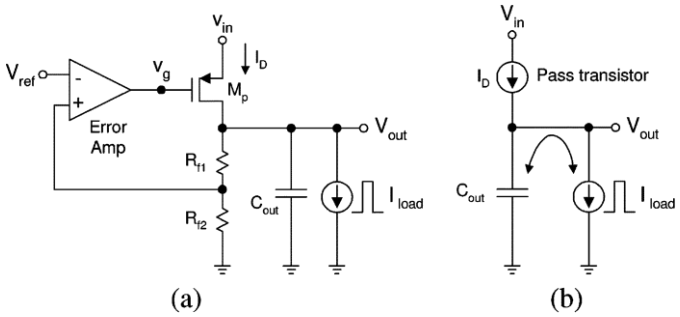


Fig. 3.Effects of limited loop bandwidth under fast load transients. (a) Basic linear regulator. (b) Equivalent circuit for fast load transients.

Uncompensated Transient Response

A large external capacitor is used on conventional LDO regulators and linear regulators in general to improve the transient load regulation. The output capacitor C_{out} in the range of nanofarad–microfarad in Fig. 3(a) stores potential energy proportional to the output voltage, and it can deliver the required instantaneous current giving some time for the regulating loop to react and provide the required output current through the pass transistor. For a pulsed output current of 0 to I_{MAX}, the transfer of charge from the capacitor to the load corresponds to a voltage drop delta(Vout) at the output node. If the LDO's loop is slower than the load transient, the pass transistor gate voltage can be assumed constant throughout the load transient. The circuit diagram of Fig. 3(b) models and its controlling circuitry as a constant current source. The maximum peaking occurs when the initial

V_{out}

current of M_p is 0, and the load current suddenly changes from 0 to I_{max}; for this case, the maximum output voltage variationis approximately determined by

$$\Delta V_{out} \cong \frac{I_{max} \cdot \Delta t}{C_{out}}.$$

In this expression, Δt is the time required by the loop to react.Thus, the changes in output voltage are inversely proportionalto C_{out}; the output voltage ripple for a given load transient is reduced by increasing the output capacitance. This side effect becomes more apparent when the load transients are much faster than the loop's gain-bandwidth product, which is usually the case resulting in peak voltages greater than 100 mV

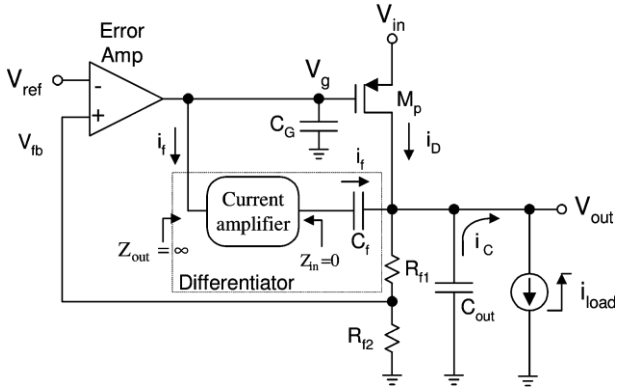
III. PROJECT DESIGN

3.1 Proposed Ldo Regulator Architecture

For the design of an external capacitorless LDO regulator, there are the following two major design considerations:

1) small over/under shoots during transients and 2) the regulator's stability.

To solve these issues, a compensating left-hand plane (LHP) zero is introduced.The properties of the Miller amplifier have been exploited for the stabilization of multistage amplifiers; the downside of that technique is the generation of an RHP zero . Some techniques reporting the elimination of that zero have been used for long time. One input of the differential amplifier monitors the fraction of the output determined by the resistor ratio of R1 and R2. The second input to the differential amplifier is from a stable voltage reference (bandgap reference). If the output voltage rises too high relative to the reference voltage, the drive to the Pass Element changes, to maintain a constant output voltage. This is a cumulative loop which monitors the output voltage continuously and varies the error voltage to make it stable.



Proposed LDO architecture

A. Transient Response Compensation

In the off-chip capacitorless LDO voltage regulator, the relatively small and load-dependant on-chip output capacitor C_{out} cannot be used to create the dominant pole since the output pole must reside at high frequency. Thus, the dominant pole must be placed within the error amplifier control loop, and transient control signal must propagate through an internal dominant pole be- fore or at the gate of the pass transistor. Overall transistor gate cap Cg=Cgs+ApassCgd+C1 and output resistance of the error amplifier R_1 act as a current-to-voltage converter, and thus, has an equivalent propagation delay proportional toR1Cg the larger the gate capacitance is, the larger the propagation delay will be. When a step output current occurs, the pass transistor can only supply the desired

current to the load when the gate voltagemoves close enough to its steady state after some time delay .

Since the error amplifier's parasitic poles are placed at high frequencies (time delay associated with these poles is small), the speed of the LDO voltage regulator is mainly determined by the pass transistor propagation delay t_p determined by gmerror/Cg. Since the ground current must be minimized in on-chip LDO voltage regulator, the value of gmerror is limited; therefore, a circuit is needed that improves the speed of charging the gate of the pass transistor.An auxiliary fast loop (differentiator), as shown, compensates for these issues and constitutes the core of the proposed LDO regulator. The differentiator forms the backbone of the architecture providing both a fast transient detector path as well as internal ac compensation.

B. The ac Stability

The topology's transfer function can be obtained as

$$\frac{v_{\text{out}}}{v_{fb}} = -\frac{(\text{Gm}_1 R_1)\cdot(\text{Gm}_P R_{\text{out}})\left(1 - s\frac{C_{gd}}{\text{Gm}_p}\right)}{\left[\begin{array}{c}(1+sR_1C_G)(1+sR_{\text{out}}C_{\text{out}}) \\ +(sR_ZC_f(\text{Gm}_f R_1 \text{Gm}_P R_{\text{out}}))\left(1 - s\frac{C_{gd}}{\text{Gm}_p}\right)\end{array}\right]}.$$

As expected, the differentiator splits the poles located at the input and output of the pass transistor, but it does not effect the location of the RHP zero. High-coupling network gainGmf*Rzensures sufficient distance between the two poles to yield stable LDO operation. . The ac compensated capacitorless LDO regulator has a Bode plot that resembles a first-order transfer function up to the complex conjugate pole pair; is the most critical case. The ac stability involves the following three essential requirements: 1) the complex pole pair does not cross into the RHP, 2) the magnitude peaking of the complex conjugate pair does not peak over the 0-dB threshold (adequate gainmargin), and 3) adequate phase margin.

IV. SCOPE AND CONSTRAINTS

The large external capacitor used in typical LDOs is removed allowing for greater power system integration for system-on-chip (SoC) applications. Typical issues are the load transient and ac stability issues

V. TOOLS USED

Main Designing and simulating tool for circuits will be Cadence Virtuoso.

VI. PERFORMANCE MEASUREMENTS

1) Power supply Ripple Rejection
2) Area
3) Loop gain
4) Vdrop
5) Settling time
6) Output noise
7) Phase margin
8) Load regulation
9) Quiescent current

VII. Testing Methodology

LDO Voltage Regulator will be designed at transistor level and simulated using submicron technology particular device models. The simulation outputs are compared to the required performance parameters.

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